Product Change Notification - SYST-22DAQX971

Date:

26 Feb 2019

Product Category:

8-bit Microcontrollers

Affected CPNs:

Notification subject:

ERRATA - PIC16(L)F18325/18345 Family Silicon Errata and Data Sheet Clarification

Notification text:

SYST-22DAQX971

Microchip has released a new DeviceDoc for the PIC16(L)F18325/18345 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at PIC16(L)F18325/18345 Family Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change:

1) Updated Table 2. Fixed links.
2) Updated section 6.2 in Module 6: Master Synchronous Serial Port (MSSP)
3) Added section 7.3 in Module 7: Electrical Specifications.
4) Other minor corrections.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 26 Feb 2019

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

PIC16(L)F18325/18345 Family Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

PIC16F18325-E/7NVAO
PIC16F18325-E/JQ
PIC16F18325-E/P
PIC16F18325-E/SL
PIC16F18325-E/SLVAO
PIC16F18325-E/ST
PIC16F18325-I/JQ
PIC16F18325-I/P
PIC16F18325-I/SL
PIC16F18325-I/ST
PIC16F18325-I/STVAO
PIC16F18325T-E/7NVAO
PIC16F18325T-E/SLV04
PIC16F18325T-E/SLVAO
PIC16F18325T-E/ST
PIC16F18325T-E/STV06
PIC16F18325T-E/STVAO
PIC16F18325T-I/JQ
PIC16F18325T-I/SL
PIC16F18325T-I/SLV05
PIC16F18325T-I/ST
PIC16F18325T-I/STVAO
PIC16F18345-E/6NVAO
PIC16F18345-E/GZ
PIC16F18345-E/P
PIC16F18345-E/SO
PIC16F18345-E/SS
PIC16F18345-H/SS
PIC16F18345-I/GZ
PIC16F18345-I/P
PIC16F18345-I/PREL
PIC16F18345-I/SO
PIC16F18345-I/SS
PIC16F18345T-E/6NVAO
PIC16F18345T-E/SS
PIC16F18345T-E/SSV03
PIC16F18345T-E/SSVAO
PIC16F18345T-H/SS
PIC16F18345T-H/SSVAO
PIC16F18345T-I/GZ
PIC16F18345T-I/SO
PIC16F18345T-I/SS
PIC16F18345T-I/SSVAO
PIC16LF18325-E/JQ
PIC16LF18325-E/JQVAO
PIC16LF18325-E/P

PIC16LF18325-E/SL
PIC16LF18325-E/ST
PIC16LF18325-I/JQ
PIC16LF18325-I/P
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PIC16LF18325-I/ST
PIC16LF18325T-E/JQVAO
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PIC16LF18325T-I/SL
PIC16LF18325T-I/ST
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PIC16LF18345-E/GZVAO
PIC16LF18345-E/P
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PIC16LF18345T-E/GZV02
PIC16LF18345T-E/GZVAO
PIC16LF18345T-I/GZ
PIC16LF18345T-I/SO
PIC16LF18345T-I/SS
PIC16LF18345T-I/SSVAO

PIC16(L)F18325/18345

PIC16(L)F18325/18345 Family
Silicon Errata and Data Sheet Clarification

The PIC16(L)F18325/18345 family devices that you have received conform functionally to the current Device Data Sheet (DS40001795**H**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F18325/18345 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A8**).

Data Sheet clarifications and corrections start on page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F18325/18345 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)			
		A4	A5	A7	A8
PIC16F18325	303Eh	2044h	2045h	2047h	2048h
PIC16LF18325	3040h	2044h	2045h	2047h	2048h
PIC16F18345	303Fh	2044h	2045h	2047h	2048h
PIC16LF18345	3041h	2044h	2045h	2047h	2048h

Note 1: The Device IDs (DEVID and DEVREV) are located at addresses 8006h and 8005h, respectively. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC16(L)F183XX Memory Programming Specification"* (DS40001738) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)			
				A4	A5	A7	A8
Oscillators	Fail-Safe Clock Monitor (FSCM)	1.1	The FSCM may fail to trigger.	X	X	X	
Power-Saving Operation Modes	Sleep	2.1	Immediate wake-up after Sleep command may cause unstable code execution.	X	X		
Peripheral Pin Select (PPS)	PPSLOCK Unlock Sequence	3.1	PPS unlock sequence does not function while in DOZE.	X	X		
Nonvolatile Memory (NVM) Control	NVMREG Access	4.1	Self-writes on LF devices below 2.2V at -40°C or less may not work.	X	X	X	
	WRERR Bit	4.2	Write Error (WRERR) bit is incorrectly set.	X	X	X	X
Device Configuration	Revision ID	5.1	Bit 6 of the Revision ID is incorrectly set.	X	X	X	X
Master Synchronous Serial Port (MSSP)	SPI Slave Mode	6.1	SSPBUF transmit shift register may be corrupted under certain conditions.	X	X	X	
	I^2C Communi-cation	6.2	Acknowledge failure on LF devices only.	X	X	X	
Electrical Specifications	SMBus 2.0	7.1	The maximum V_{IL} level changes when V_{DD} is below 4.0V at 125°C.	X	X	X	
	Fixed Voltage Reference (FVR) Accuracy	7.2	FVR output tolerance may be higher than specified at temperatures below -20°C.	X	X	X	X
	NVM Access	7.3	NVM access on LF devices may not work at all specified voltage and temperature ranges.	X	X	X	X
ADC Auto-Conversion Trigger	Auto-Conver-sion Trigger	8.1	Auto-trigger event does not begin a conversion while in Sleep.	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A8**).

1. Module: Oscillators

1.1 Fail-Safe Clock Monitor (FSCM)

The Fail-Safe Clock Monitor may fail to trigger with the loss of the external clock signal when the 4x PLL is enabled. This includes all external clock modes, LP, XT, HS, ECL, ECM and ECH.

Work around

None.

Affected Silicon Revisions

A4	A5	A7	A8				
X	X	X					

2. Module: Power-Saving Operation Modes

2.1 Sleep Mode

When using the HFINTOSC as the system clock and the Sleep command is executed and the device immediately wakes up, the CPU will begin code execution at an unknown oscillator frequency until the oscillator stabilizes.

Work around

Method 1:

Use a peripheral that utilizes the HFINTOSC as a clock source or input to the peripheral. When a peripheral uses the HFINTOSC, the HFINTOSC will remain active during Sleep.

Method 2:

Before executing the Sleep command, switch the oscillator source to either the LFINTOSC or an external clocking source. Once the device wakes from Sleep, the HFINTOSC can be re-enabled as the primary oscillator source.

Method 3:

Enable the HFOEN bit in the OSCEN register. Setting this bit manually enables the HFINTOSC, and is unaffected by Sleep.

Affected Silicon Revisions

A4	A5	A7	A8				
X	X						

3. Module: Peripheral Pin Select (PPS)

3.1 PPS Unlock Sequence

When using the Peripheral Pin Select Unlock sequence while in DOZE mode, the unlock sequence is incorrectly executed, causing the sequence to fail and the PPS registers to remain locked.

Work around

The unlock sequence should not be performed while the device is in DOZE mode.

Affected Silicon Revisions

A4	A5	A7	A8				
X	X						

4. Module: Nonvolatile Memory (NVM) Control

4.1 NVMREG Access

When performing self-writes through NVMREG access on PIC16LF18325/45 devices with V_{DD} below 2.2V and a temperature of -40°C, the write operation may not work. This applies to both Program Flash Memory and EEPROM writes.

Work around

None.

Affected Silicon Revisions

A4	A5	A7	A8				
X	X	X					

4.2 NVM WRERR

If a Reset occurs while a self-write operation is in progress, the Write Error (WRERR) bit is set. If the user clears the WRERR bit and another Reset occurs even though no self-write is in progress, the WRERR bit will be incorrectly set again since the internal write latch has not been cleared.

Work around

A successful write operation will clear the WRERR condition.

Affected Silicon Revisions

A4	A5	A7	A8				
X	X	X	X				

5. Module: Device Configuration

5.1 Revision ID

When reading the Revision ID, bit 6 of the Revision ID register is incorrectly set, causing the Revision ID to read 204x (x = revision number) rather than 200x.

Work around

None.

Affected Silicon Revisions

A4	A5	A7	A8				
X	X	X	X				

6. Module: Master Synchronous Serial Port (MSSP)

6.1 MSSP SPI Slave Mode

When operating in SPI Slave mode, if the incoming SCK clock signal arrives during any of the conditions below, the SSPBUF transmit shift register may become corrupted. The transmitted slave byte cannot be assured to be correct, and the state of the WCOL bit may or may not indicate a write collision.

These conditions include:

- A write to an SFR
- A write to RAM following an SFR read
- A write to RAM prior to an SFR read.

Work around

Method 1 (Interrupt-based using SS):

Connect the $\overline{SS}$ line to both the $\overline{SS}$ input and either an INT or IOC input pin.

1. Enable INT or IOC interrupts (interrupt on falling edge if available, otherwise check that $\overline{SS}$==0 when the interrupt occurs).
2. Load SSPBUF with the data to be transmitted.
3. Continue program execution.
4. When the Interrupt Service Routine (ISR) is invoked, do either of the following:
   a) Add a delay that ensures the first SCK clock will be complete, or
   b) Poll SSPSTAT.BF (while(BF==0)), and wait for the transmission/reception to complete.

Once one of these two methods are complete, it is safe to return to program execution.

Method 2 (Bit polling-based using SS):

1. Load SSPBUF with the data to be transmitted.
2. Poll the $\overline{SS}$ line and wait for the $\overline{SS}$ to go active (while(!PORTx.$\overline{SS}$==0)).
3. When $\overline{SS}$ is active (SS==0), do either of the following:
   a) Add a delay that ensures the first SCK clock will be complete, or
   b) Poll SSPSTAT.BF (while(BF==0)), and wait for the transmission/reception to complete.

Once one of these two methods are complete, it is safe to return to program execution.

Method 3 (SS not available):

1. Load SSPBUF with the data to be transmitted.
2. Poll SSPSTAT.BF (while(BF==0)), and wait for the transmission/reception to complete.

Affected Silicon Revisions

A4	A5	A7	A8				
X	X	X					

6.2 I²C Communication

When using the MSSP on LF devices to perform I²C communication, and the VDD voltage is above 3.0V, the Acknowledge (ACK) sequence does not always occur.

In 10-bit Slave mode, the MSSP may not generate the ACK sequence following reception of the second address byte (the lower address bits A7-A0). This issue occurs most commonly in 10-bit Slave mode. In 7-bit Slave mode, the MSSP may not generate the ACK sequence following the reception of the byte immediately following the 7-bit address (typically the first data byte).

In 10-bit Multi-Master mode, the MSSP may not generate the ACK sequence following the reception of the second address byte when acting as a slave. In 7-bit Multi-Master mode, the MSSP may not generate the ACK sequence following the reception of the first byte immediately following the 7-bit address when acting as a slave.

Work around

Do not exceed a VDD voltage of 3.0V when using an LF device for I²C communications.

Affected Silicon Revisions

A4	A5	A7	A8				
X	X	X					

7. Module: Electrical Specifications

7.1 SMBus 2.0 VIL Level

At 125°C, when the VDD voltage level supplied to the device is 4.0V and above, the maximum SMBus 2.0 voltage level for the VIL parameter is 0.8V. When VDD drops below 4.0V, the maximum SMBus voltage level for VIL drops to 0.7V. This issue applies to extended temperature devices only.

Work around

None.

A4	A5	A7	A8				
X	X	X					

7.2 Fixed Voltage Reference (FVR) Accuracy

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings, (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting) and FVR03 (4X gain setting).

Work around

At temperatures above -20°C, the stated tolerances in the data sheet remain in effect. Operate the FVR only at temperatures above -20°C.

Affected Silicon Revisions

A4	A5	A7	A8				
X	X	X	X				

7.3 Nonvolatile Memory

Nonvolatile memory (NVM) access on LF devices may not work when operating at temperatures between -40°C and +25°C and VDD levels below 2.0V.

Work around

None.

Affected Silicon Revisions

A3	A4	A7	A8				
X	X	X	X				

8. Module: ADC Auto-Conversion Trigger

8.1 ADC Auto-Conversion Trigger

When using ADC in Sleep mode, an auto-conversion trigger event will not cause the ADC to begin a conversion.

Work around

None.

Affected Silicon Revisions

A4	A5	A7	A8				
X	X	X	X				

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001795**H**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev K Document (02/2019)

Updated Table 2. Fixed links.

Updated section 6.2 in Module 6: Master Synchronous Serial Port (MSSP).

Added section 7.3 in Module 7: Electrical Specifications.

Other minor corrections.

Rev J Document (03/2018)

Updated Table 1 and Table 2.

Changes brought to Module 6: Master Synchronous Serial Port (MSSP).

Added Module 7: Electrical Specifications.

Added Module 8: ADC Auto-Conversion Trigger

Other minor corrections.

Rev H Document (07/2017)

Added Module 6 (Electrical Specifications); Updated Table 1 and 2; Other minor corrections.

Rev G Document (01/2017)

Silicon Errata issues:

Minor changes brought to Module 4: Nonvolatile Memory (NVM) Control, error temperature changed from 0° or less to -40°C.

Rev F Document (01/2017)

Data Sheet Clarifications:

Added Module 1: Comparator.

Rev E Document (10/2016)

Silicon Errata Issues:
Added Module 5: Device Configuration.

Rev D Document (09/2016)

Silicon Errata Issues:
Added Module 2: Power-Saving Operation Modes; Module 3: Peripheral Pin Select (PPS); Module 4: Nonvolatile Memory (NVM) Control.

Data Sheet Clarifications:
Removed Modules 1-5. Data sheet has been updated.

Rev C Document (11/2015)

Added silicon revision A5.

Rev B Document (09/2015)

Data Sheet Clarifications:

Revised Module 2: Oscillators (modified Register 6-6); Added Module 4: Power-Saving Operation (modified Register 8.1); Added Module 5: Electrical Specifications (modified Table 34-11).

Rev A Document (09/2015)

Initial release of this document.

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