Product Change Notification / SYST-18ENNV955

Date:

19-Jul-2022

Product Category:

CAN Controller

PCN Type:

Document Change

Notification Subject:

ERRATA - MCP2518FD Silicon Errata and Data Sheet Clarification

Affected CPNs:

SYST-18ENNV955_Affected_CPN_07192022.pdf
SYST-18ENNV955_Affected_CPN_07192022.csv

Notification Text:

SYST-18ENNV955

Microchip has released a new Errata for the MCP2518FD Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at MCP2518FD Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change: Corrections added to SPI Module.

Reason for Change: To improve Productivity

Impacts to Data Sheet: None

Change Implementation Status: Complete

Date Document Changes Effective: 19 Jul 2022

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices:: N/A

Attachments:

MCP2518FD Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

MCP2518FDT-H/SL
MCP2518FDT-H/SLVAO
MCP2518FDT-H/QBB
MCP2518FDT-H/QBBV01
MCP2518FDT-H/QBBV03
MCP2518FDT-H/QBBV04
MCP2518FDT-H/QBBVAO
MCP2518FDT-E/SL
MCP2518FDT-E/SLVAO
MCP2518FDT-E/QBB
MCP2518FDT-E/QBBV02
MCP2518FDT-E/QBBVAO

MCP2518FD
Silicon Errata and Data Sheet Clarification

The functionality of the MCP2518FD devices is described in the Device Data Sheet (DS20006027), except for the anomalies described below.

1. Module: SPI Module

Incorrect data for certain `READ/READ_CRC` commands:

There is a possibility that the transmitted data on a `READ/READ_CRC` is wrong when reading from the chip. A glitch on the SDO line shorter than 1 bit in length occurs and creates wrong data.

Fix/Work Around

Only use the `READ_CRC` command and if a CRC mismatch occurs, re-issue the `READ_CRC` command.

The following registers can be affected:

CiTXIF

CiRXIF

CiCON

CiTBC

CiINT

CiRXOVIF

CiTXATIF

CiTXREQ

CiTREC

CiBDIAG0

CiBDIAG1

CiTXQSTA

CiFIFOSTAm

The occurrence can be minimized by not using FIFOs 7/15/23/31.

Bit 31 of RAM reads can also be affected. This can be avoided by reading from a receive FIFO only after the message has been loaded into the FIFO, indicated by the receive flags. This is the recommended procedure independent of the issue described here.

2. Module: ECC Module

ECC Single Error Correction does not work in all cases:
Fix/Work Around:

Enable Single Error Correction (SEC) and Double Error Detection (DED) interrupts by setting SECIE and DEDIE. Handle SECIF as a detection interrupt and do not rely on the error correction. Instead, handle both interrupts as a notification that the RAM word at ERRADDR was corrupted.

3. Module: SPI Module

SFR address rollover does not work:

The SFR address rollover, from 0x3FF to 0x000 and from 0xFFF to 0xE00, does not work. Instead, the address changes from 0x3FF to 0x400 and from 0xFFF to 0x000.

The address rollover for the RAM works as described.

Fix/Work Around:

None.

4. Module: SPI/RAM Module

The SPI can write corrupted data to the RAM at fast SPI speeds:

Simultaneous activity on the CAN bus while writing data to RAM via the SPI interface, with high SCK frequency, can lead to corrupted data being written to RAM.

Fix/Work Around:

Ensure that FSCK is less than or equal to 0.85 * (FSYSCLK/2).

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5. Module: SPI/GPIO Module

Writing multiple bytes to the IOCON register using one SPI `WRITE` instruction may overwrite LAT0 and LAT1:

Writing Byte 2 and Byte 3 of the IOCON register using one SPI `WRITE` instruction clears LAT0 and LAT1.

Fix/Work Around:

When setting LAT0 or LAT1, do not use a multi-data byte SPI `WRITE` instruction.

Instead, write the bit fields in the IOCON register using single data byte SFR `WRITE` instructions.

Clarifications/Corrections to the Data Sheet:

In the MCP2518FD Data Sheet (DS20006027**B**), the following clarifications and corrections should be noted.

None.

APPENDIX A: REVISION HISTORY

Revision D (July 2022)

• Corrections added to **SPI Module**.

Revision C (October 2020)

• Corrections added to **SPI Module**.

Revision B (September 2020)

• Added **ECC Module**, **SPI Module**, **SPI/RAM Module** and **SPI/GPIO Module**.

Revision A (May 2018)

• Initial Release of this Document.

NOTES:

Note the following details of the code protection feature on Microchip products:

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