

Customer Information Notification

05-Feb-2020 Issue Date: Effective Date: 06-Feb-2020 Dear PCN NXP,

Please find below a Quality Notification that has been distributed by NXP.



201912015

Change Category

[] Wafer Fab Process

[] Wafer Fab Materials

[] Wafer Fab Location

[] Firmware

FS8400/FS8500, VR5500, FS5502 Power Management IC Data Sheet Updates

[] Assembly Process [] Assembly Materials [] Assembly Location [] Other	[] Product Marking	[] Test Location	[] Design
	[] Mechanical Specification	[]Test Process	[] Errata
	[] Packing/Shipping/Labeling	[] Test Equipment	[X] Electrical spec./Test coverage

Description

NXP Semiconductors announces data sheet updates for the FS8400/FS8500, VR5500 and FS5502 Power Management IC devices associated with this notification. The new data sheets provide updates related to new features, typo corrections, and clarifications. The revision history included in each updated document provides a detailed description of the changes. Changes are summarized below.

FS8400 / FS8500 Data Sheet Changes:

1. Automatic Pulse Skipping (APS) mode on Vpre can be enabled by OTP configuration

- 2. Buck1/2/3 soft-start ramp rate and time slot configurability by OTP
- 3. FS85 Mask revision in main register mapping: FMREV and MMREV are readable by SPI/I2C
- 4. Other typo and clarifications listed in Section 38: Revision history

The new FS84_FS85C v.5.0 data sheet can be found at:

https://www.nxp.com/webapp/sps/download/mod_download.jsp?colCode=FS84-FS85&appType=moderatedWithoutFAE

VR5500 Data Sheet Changes:

- 1. Automatic Pulse Skipping (APS) mode on Vpre can be enabled by OTP configuration
- 2. Buck1/3 soft-start ramp rate and time slot configurability by OTP
- 3. VR5500 Mask revision in main register mapping: FMREV and MMREV are readable by I2C
- 4. Other typo and clarifications listed in Section 36: Revision history

The new VR5500 v.6.0 data sheet is attached to this notice, and can be found at: <u>https://www.nxp.com/docs/en/data-sheet/VR5500.pdf</u>

FS5502 Data Sheet Changes:

- 1. Automatic Pulse Skipping (APS) mode on Vpre can be enabled by OTP configuration
- 2. Buck1/3 soft-start ramp rate and time slot configurability by OTP
- 3. FS5502 Mask revision in main register mapping: FMREV and MMREV are readable by I2C
- 4. Other typo and clarifications listed in Section 33: Revision history

The new FS5502 v.3.0 data sheet is attached to this notice, and can be found at: https://www.nxp.com/docs/en/data-sheet/FS5502.pdf

Corresponding ZVEI Delta Qualification Matrix ID: SEM-DS-02 and SEM-DS-03

Reason

The data sheet has been updated to correct errors, and provide additional technical clarification on some new device features in order to enable the full market launch.

Identification of Affected Products

Product identification does not change

Anticipated Impact on Form, Fit, Function, Reliability or Quality

There is no change to product form, fit, reliability or quality. Function is enhanced with new device features as described.

Data Sheet Revision

A new datasheet will be issued

Additional information

Affected products and sales history information: see attached file

Additional documents: view online

Contact and Support

For all inquiries regarding the ePCN tool application or access issues, please <u>contact NXP "Global Quality</u> <u>Support Team"</u>.

For all Quality Notification content inquiries, please contact your local NXP Sales Support team.

For specific questions on this notice or the products affected please contact our specialist directly: **Name** Olivier Culie

Position Applications Engineer

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Customer Focus, Passion to Win.

NXP Quality Management Team. About NXP Semiconductors

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