Product Change Notification - SYST-28VIVN630 (Printer Friendly)

Date:

30 Jun 2017

Product Category:

32-bit PIC Microcontrollers

Affected CPNs:

Notification subject:

Data Sheet - SAM L21 Datasheet

Notification text:

SYST-28VIVN630

Microchip has released a new DeviceDoc for the SAM L21 Datasheet of devices. If you are using one of these devices please read the document located at SAM L21 Datasheet.

Notification Status: Final

Description of Change:
1) Device variant for temperature range from -40°C to 105°C added.
2) Change of document style.
3) New Microchip document number. Previous version was Atmel document 42385 rev.J.
4) Added the temperature range: -40°C to 85°C and -40°C to 105°C to features
5) I/O Multiplexing and Considerations Table 7-5: No PB16, PB7 on SAM L21G
6) Editorial updates on PAC - Peripheral Access Controller , DSU - Device Service Unit , Clock System , GCLK - Generic Clock Controller, EIC – External Interrupt Controller, OSC32KCTRL – 32KHz Oscillators Controller , SUPC – Supply Controller, WDT – Watchdog Timer, TC – Timer/Counter, AES – Advanced Encryption Standard, CCL – Configurable Custom Logic and USB – Universal Serial Bus
7) For RTC – Real-Time Counter, Functional description of General Purpose registers added, Bit field position updated: CTRLB.ACTF, CTRLB.DEBF, SYNCBUSY.GPn. , Register RTC.PER is at offset 0x1C.
8) For DMAC – Direct Memory Access Controller, STEPSIZE factor in SRAM register BTCTRL is based on beat size in bytes.
9) Register OSCCTRL.DPLLCTRLB is not Enable-protected on OSCCTRL – Oscillators Controller
10) Register WDT.CONFIG is not Enable-protected and Register WDT.EWCTRL is not Enable-protected for WDT – Watchdog Timer
11) Notes added: PINCFG and PMUX registers are repeated per PORT group with offset 0x80 and Bit PORT.CTRL.SAMPLING is write-only for PORT - I/O Pin Controller
11) Bits ENABLE and SWRST in TC.CTRLA are not enable protected, Register TC.STATUS is read-synchronized, Register TC.INTENCLR: "Enable" in bit names replaced by "Disable", Registers TC.CCx are write- and read-synchronized for TC – Timer/Counter
12) For TCC – Timer/Counter for Control Applications, Register TCC.PER is write-synchronized, Register TCC.PATT is write-synchronized ,Size of PGVB and PGEB bits in TCC.PATTBUF is 8 bit.
13) Register TRNG.DATA has R/W access and register TRNG.EVCTRL is not enable-protected for TRNG – True Random Number Generator
14) Register USB.FNUM is read-only, USB.EPSTATUSCLRn is write-only, USB.EPSTATUSSETn is write-only, USB.STATUS_PIPE has R/W access, USB.QOSCTRL has Reset value 0x05 for USB – Universal Serial Bus.
15) Register DAC.CTRLB is not enable-protected for DAC – Digital-to-Analog Converter
16) Electrical Characteristics Data for 105°C device variant added; Updates for 85°C device variant: – Power Consumption table for OSC16M: symbol and description corrected. – Operating Conditions table for DAC: Conditions for VREF simplified.
17) Added Errata:

SERCOM: In USART autobaud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors. Errata reference 13852
DAC: DAC stepping does not work when data written from DMA. Errata reference 15210
EIC: Spurious INTFLAG is raised when EIC is configured LOW LEVEL with Filter mode. Errata reference 15278. Changing the NMI configuration(CONFIGn.SENSEx) on the fly may lead to a false NMI interrupt. Errata reference 15279
ADC: Clock request not going low in standby mode. Errata reference 15463
USART: PA24/PA25 pull-up/pull-down configuration erroneous when used as RTS, CTS. Errata reference 15581
PORT: PORT read/write attempts on non-implemented registers, including addresses beyond the last implemented register group (PA, PB, ...) do not generate a PAC protection error. Errata reference 15611
TCC: Using dithering mode with external retrigger events can lead to unexpected stretch of right aligned pulses, or shrink of left aligned pulses. Errata reference 15625
DMAC: When using more than one DMA channel and one of them is w/linked descriptor, a fetch error can appear on this channel. Errata reference 15670
DMAC: When at least one channel w/linked descriptors is already active, and the channel number of the channel being enabled is lower than the channel already active, enabling another DMA channel can result in a channel Fetch Error (FERR) or an incorrect descriptor fetch. Errata reference 15683
FDPLL: When changing on-the-fly the FDPLL ratio in DPLLnRATIO register, STATUS.DPLLnLDRTO will not be set when the ratio update will be completed.
Errata reference 15753 Errata reference for changed (content of errata unchanged): DFLL48M: 16192 (was 10669) and DFLL48M: 16193 (was 11938)

Impacts to Data Sheet: None

Reason for Change: To Improve Manufacturability

Change Implementation Status: Complete

Date Document Changes Effective: 30 June 2017

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):
SAM L21 Datasheet

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