74LV1T08

2-input single supply translating AND gate Rev. 5.1 — 20 March 2024

Product data sheet

1. General description

The 74LV1T08 is a single, level translating 2-input AND gate. The low threshold inputs support 1.8 V input logic at V_{CC} = 3.3 V and can be used in 1.8 V to 3.3 V level up translation. In addition, the 5 V tolerant input pins enable level down translation (3.3 V to 2.5 V output at V_{CC} = 2.5 V). The output level is referenced to the supply voltage and supports 1.8 V, 2.5 V, 3.3 V and 5.0 V CMOS levels. The wide V_{CC} range permits the generation of output levels to connect to controllers or processors.

2. Features and benefits

- Single supply voltage translator at 1.8 V, 2.5 V, 3.3 V and 5.0 V
- Up translation
 - 1.2 V to 1.8 V at V_{CC} = 1.8 V
 - 1.5 V to 2.5 V at V_{CC} = 2.5 V
 - 1.8 V to 3.3 V at V_{CC} = 3.3 V
 - 3.3 V to 5.0 V at V_{CC} = 5.0 V
- Down translation
 - 3.3 V to 1.8 V at V_{CC} = 1.8 V
 - 3.3 V to 2.5 V at V_{CC} = 2.5 V
 - 5.0 V to 3.3 V at V_{CC} = 3.3 V
- 5 V tolerant inputs
- Latch-up performance exceeds 250 mA per JESD 78 Class II
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Applications

- Portable applications
- PC and notebooks
- Industrial controller
- Telecom



4. Ordering information

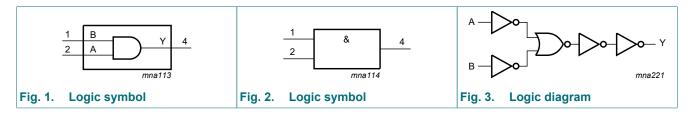
Table 1. Orderin Type number	Package									
	Temperature range	Name	Description	Version						
74LV1T08GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	<u>SOT353-1</u>						
74LV1T08GV	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	<u>SOT753</u>						
<u>74LV1T08GX</u>	-40 °C to +125 °C	X2SON5	plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 × 0.8 × 0.32 mm	<u>SOT1226-3</u>						

5. Marking

Table 2. Marking						
Type number	Marking code[1]					
74LV1T08GW	SJ					
74LV1T08GV	SJ					
74LV1T08GX	SJ					

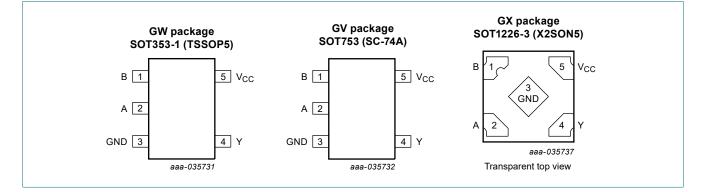
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

6. Functional diagram



7. Pinning information

7.1. Pinning



7.2. Pin description

Table 3. Pin description							
Symbol	Pin	Description					
В	1	data input					
A	2	data input					
GND	3	ground (0 V)					
Y	4	data output					
V _{CC}	5	supply voltage					

8. Functional description

Table 4. Function table

H = *HIGH* voltage level; *L* = *LOW* voltage level.

Input	Output	
Α	В	Y
L	L	L
L	Н	L
Н	L	L
Н	Н	Н

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9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
VI	input voltage	[1]	-0.5	+7.0	V
Vo	output voltage	output HIGH or LOW state [2][3]	-0.5	V _{CC} + 0.5	V
		output in power-off state [2]	-0.5	4.6	V
I _{IK}	input clamping current	V ₁ < 0 V	-20	-	mA
I _{OK}	output clamping current	V_{O} < 0 V or V_{O} > V_{CC}	-	±20	mA
I _O	output current	$V_{O} = 0 V$ to V_{CC}	-	±25	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 \ ^{\circ}C \ to +125 \ ^{\circ}C$ [4]	-	250	mW

[1] If the input current ratings are observed, the minimum input voltage ratings may be exceeded.

[2] If the output current ratings are observed, the output voltage ratings may be exceeded.

[3] This value is limited to 7 V maximum.

[4] For SOT353-1 (TSSOP5) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C. For SOT753 (SC-74A) package: P_{tot} derates linearly with 3.8 mW/K above 85 °C. For SOT1226-3 (X2SON5) package: P_{tot} derates linearly with 3.0 mW/K above 67 °C.

10. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CC}	supply voltage		1.6	5.0	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage	output HIGH or LOW state	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.8 V to 5.0 V	-	-	20	ns/V

11. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °	C	-40 °C to	+85 °C	-40 °C to +125 °C		Unit
			Min	Мах	Min	Мах	Min	Max	
V _{IH}	HIGH-level	V _{CC} = 1.65 V to 1.8 V	0.94	-	1.0	-	1.0	-	V
	input voltage	V _{CC} = 2.0 V	0.99	-	1.03	-	1.03	-	V
		V _{CC} = 2.25 V to 2.5 V	1.135	-	1.18	-	1.18	-	V
		V _{CC} = 2.75 V	1.21	-	1.23	-	1.23	-	V
		V _{CC} = 3.0 V to 3.3 V	1.35	-	1.37	-	1.37	-	V
		V _{CC} = 3.6 V	1.47	-	1.48	-	1.48	-	V
		V _{CC} = 4.5 V to 5.0 V	2.02	-	2.03	-	2.03	-	V
		V _{CC} = 5.5 V	2.10	-	2.11	-	2.11	-	V
V _{IL}	LOW-level	V _{CC} = 1.65 V to 2.0 V	-	0.58	-	0.55	-	0.55	V
	input voltage	V _{CC} = 2.25 V to 2.75 V	-	0.75	-	0.71	-	0.71	V
		V _{CC} = 3.0 V to 3.6 V	-	0.80	-	0.65	-	0.65	V
		V _{CC} = 4.5 V to 5.5 V	-	0.80	-	0.80	-	0.80	V
V _{OH}	HIGH-level	$V_{I} = V_{IH} \text{ or } V_{IL};$							
011	output voltage	V _{CC} = 1.65 V to 5.5 V; I _O = -20 μA	V _{CC} - 0.1	-	V _{CC} - 0.1	-	V _{CC} - 0.1	-	V
		V _{CC} = 1.65 V; I _O = -2 mA	1.28	-	1.21	-	1.21	-	V
		V _{CC} = 1.8 V; I _O = -2 mA	1.5	-	1.45	-	1.45	-	V
		V _{CC} = 2.3 V; I _O = -2.3 mA	2.0	-	2.0	-	2.0	-	V
		V _{CC} = 2.3 V; I _O = -3 mA	2.0	-	1.93	-	1.93	-	V
		V _{CC} = 2.5 V; I _O = -3 mA	2.25	-	2.15	-	2.15	-	V
		V _{CC} = 3.0 V; I _O = -3 mA	2.78	-	2.7	-	2.7	-	V
		V _{CC} = 3.0 V; I _O = -5.5 mA	2.6	-	2.49	-	2.49	-	V
		V _{CC} = 3.3 V; I _O = -5.5 mA	2.9	-	2.8	-	2.8	-	V
		V _{CC} = 4.5 V; I _O = -4 mA	4.2	-	4.1	-	4.1	-	V
		V _{CC} = 4.5 V; I _O = -8 mA	4.1	-	3.95	-	3.95	-	V
		V _{CC} = 5.0 V; I _O = -8 mA	4.6	-	4.5	-	4.5	-	V
V _{OL}	LOW-level	V _I = V _{IH} or V _{IL}							
	output voltage	V _{CC} = 1.65 V to 5.5 V; I _O = 20 μA	-	0.1	-	0.1	-	0.1	V
		V _{CC} = 1.65 V; I _O = 2 mA	-	0.2	-	0.25	-	0.25	V
		V _{CC} = 2.3 V; I _O = 2.3 mA	-	0.1	-	0.15	-	0.15	V
		V _{CC} = 2.3 V; I _O = 3 mA	-	0.15	-	0.2	-	0.2	V
		V _{CC} = 3.0 V; I _O = 3 mA	-	0.1	-	0.15	-	0.15	V
		V _{CC} = 3.0 V; I _O = 5.5 mA	-	0.2	-	0.252	-	0.252	V
		V _{CC} = 4.5 V; I _O = 4 mA	-	0.15	-	0.2	-	0.2	V
		V _{CC} = 4.5 V; I _O = 8 mA	-	0.3	-	0.35	-	0.35	V
I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 0 V$ to 5.5 V	-	±0.1	-	±1	-	±1	μA
I _{CC}	supply current		-	1	-	10	-	10	μA

Symbol Parameter		Conditions	25 °C		-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	Min	Max	1
ΔI _{CC} additional supply curre		per input pin; V _{CC} = 1.8 V; V _I = 0.3 V or 1.1 V; I _O = 0 A; other pins at V _{CC} or GND	-	10	-	10	-	10	μA
		per input pin; V _{CC} = 5.5 V; V _I = 0.3 V or 3.4 V; I _O = 0 A; other pins at V _{CC} or GND	-	1.35	-	1.5	-	1.5	mA

12. Dynamic characteristics

Table 8. Dynamic characteristics

GND = 0 V. For test circuit, see Fig. 5.

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to	o +125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
t _{pd} p	propagation	A, B to Y; see <u>Fig. 4</u> [1]								
	delay	V _{CC} = 1.8 V; C _L = 15 pF	-	6.5	9.7	-	10.9	-	11.7	ns
		V _{CC} = 1.8 V; C _L = 30 pF	-	7.6	10.9	-	12.4	-	13.4	ns
		V _{CC} = 2.5 V; C _L = 15 pF	-	4.6	6.6	-	7.6	-	8.2	ns
		V _{CC} = 2.5 V; C _L = 30 pF	-	5.3	7.5	-	8.6	-	9.2	ns
		V _{CC} = 3.3 V; C _L = 15 pF	-	3.8	5.4	-	6.1	-	6.5	ns
		V _{CC} = 3.3 V; C _L = 30 pF	-	4.4	6.1	-	6.8	-	7.3	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	3.2	4.1	-	4.5	-	4.7	ns
		V _{CC} = 5.0 V; C _L = 30 pF	-	3.6	4.6	-	5.1	-	5.4	ns
CI	input capacitance	$V_{I} = V_{CC}$ or GND; $V_{CC} = 3.3 V$	-	1.5	10	-	10	-	10	pF
Co	output capacitance	$V_{O} = V_{CC}$ or GND; $V_{CC} = 3.3 V$	-	2.5	-	-	-	-	-	pF
C _{PD}	power dissipation	per buffer; V_I = GND to V_{CC} ; [2] C_L = 30 pF; f = 10 MHz								
	capacitance	V _{CC} = 1.8 V	-	4.2	-	-	-	-	-	pF
		V _{CC} = 2.5 V	-	5.3	-	-	-	-	-	pF
		V _{CC} = 3.3 V	-	7.2	-	-	-	-	-	pF
		V _{CC} = 5.0 V	-	11.1	-	-	-	-	-	pF

[1] [2]

 $t_{pd} \text{ is the same as } t_{PLH} \text{ and } t_{PHL}. \\ C_{PD} \text{ is used to determine the dynamic power dissipation } (P_D \text{ in } \mu W). \\ P_D = C_{PD} \times V_{CC} \stackrel{2}{} \times f_i \times N + \sum (C_L \times V_{CC} \stackrel{2}{} \times f_o) \text{ where:}$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

 C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching; $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

12.1. Waveform and test circuit

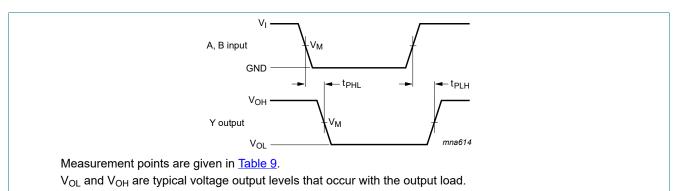
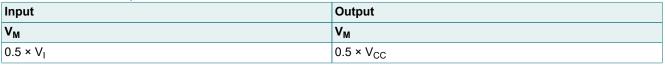
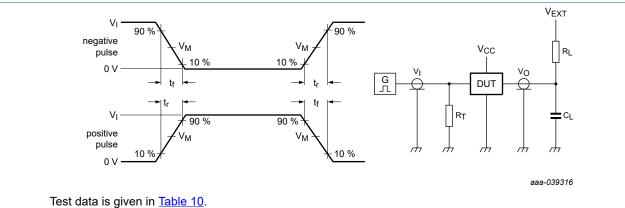


Fig. 4. The input A, B to output Y propagation delays

Table 9. Measurement points





Definitions test circuit:

 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance;

R_L = Load resistance;

V_{EXT} = External voltage for measuring switching times.

Fig. 5. Test circuit for measuring switching times

Supply voltage	ly voltage Input			roltage Input Load			V _{EXT}	V _{EXT}		
V _{cc}	VI	Δt/ΔV [1]	f _{max}	CL	RL	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}		
1.8 V	V _{CC}	≤ 1.0 ns/V	15 MHz	15 pF, 30 pF	1MΩ	GND	GND	V _{CC}		
2.5 V	V _{CC}	≤ 1.0 ns/V	25 MHz	15 pF, 30 pF	1MΩ	GND	GND	V _{CC}		
3.3 V	3 V	≤ 1.0 ns/V	50 MHz	15 pF, 30 pF	1MΩ	GND	GND	V _{CC}		
5.0 V	3 V	≤ 1.0 ns/V	50 MHz	15 pF, 30 pF	1MΩ	GND	GND	V _{CC}		

[1] dV/dt ≥ 1.0 V/ns

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13. Package outline

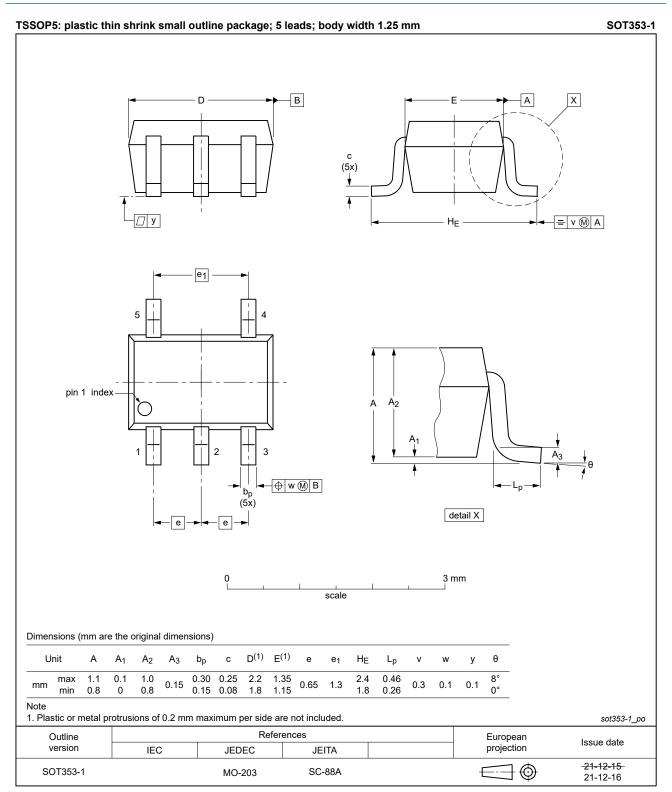


Fig. 6. Package outline SOT353-1 (TSSOP5)

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2-input single supply translating AND gate

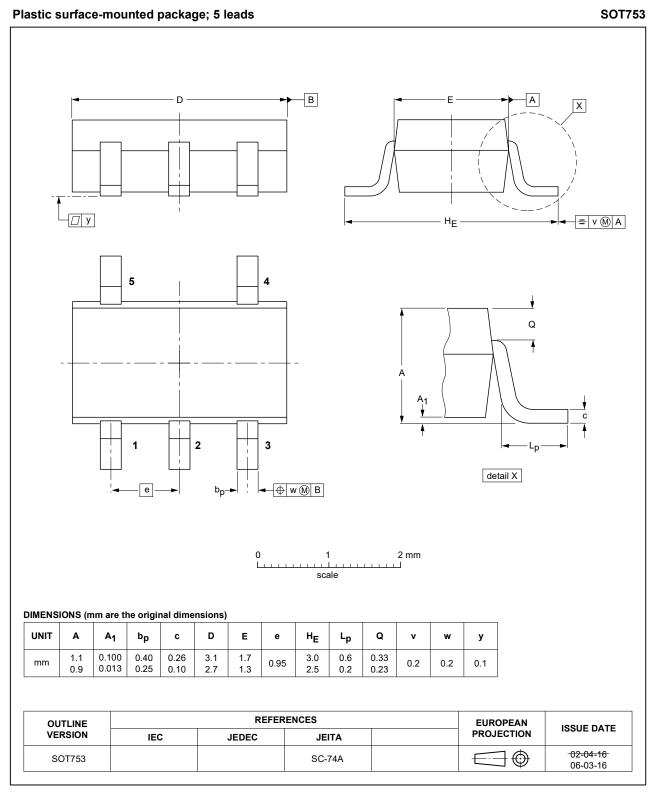


Fig. 7. Package outline SOT753 (SC-74A)

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2-input single supply translating AND gate

5 terminals; body 0.8 x 0.8 x 0.32 mm SOT1226-3 С Seating Plane ____y _____ 5x X Α В D E A₃ pin 1 . index area A₁ pin 1 е index area b // y1 C → v M C A B 2 ^(4x) φ w M C t L (4x) Ŧ 3 (6x) 1 5 4 1 mm 0 scale Dimensions (mm are the original dimensions) Unit D Dh Е А A_1 b Κ A₃ е L v w у У1 max 0.35 0.04 nom 0.32 0.02 0.85 0.30 0.85 0.80 0.25 0.80 0.25 0.27 0.10 0.20 0.50 mm nom 0.22 0.1 0.05 0.05 0.05 (Typ.) 0.75 0.20 0.20 0.17 min 0.30 0.00 0.75 0.15 sot1226-3_po References Outline European Issue date version IEC projection JEDEC EIAJ

X2SON5: plastic thermal enhanced extremely thin small outline package; no leads;

Fig. 8. Package outline SOT1226-3 (X2SON5)

- - -

- 19-11-06-19-11-07

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SOT1226-3

14. Abbreviations

Table 11. Abbreviations						
Acronym	Description					
CDM	Charge Device Model					
CMOS	Complementary Metal Oxide Semiconductor					
DUT	Device Under Test					
ESD	ElectroStatic Discharge					
HBM	Human Body Model					

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes					
74LV1T08 v.5.1	20240320	Product data sheet	-	74LV1T08 v.4					
Modifications:		 <u>Section 2</u>: ESD specification updated according to the latest JEDEC standard. <u>Fig. 5</u>: Errata. 							
74LV1T08 v.4	20220223	Product data sheet	-	74LV1T08 v.3					
Modifications:	Package St	Package SOT1226 (X2SON5) changed to SOT1226-3 (X2SON5).							
74LV1T08 v.3	20220207	Product data sheet	-	74LV1T08 v.2					
Modifications:	• <u>Fig. 6</u> : Pack	age outline drawing for SC	T353-1 (TSSOP5	i) has changed.					
74LV1T08 v.2	20191203	Product data sheet	-	74LV1T08 v.1					
Modifications:		 Type number 74LV1T08GV (SOT753/SC-74A) added. <u>Table 5</u>: Derating values for P_{tot} total power dissipation updated. 							
74LV1T08 v.1	20171122	Product data sheet	-	-					

16. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

 Please consult the most recently issued document before initiating or completing a design.

- [2] The term 'short data sheet' is explained in section "Definitions".
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