



STB12NK80Z STP12NK80Z - STW12NK80Z

N-channel 800V - 0.65Ω - 10.5A - TO-220 - D²PAK - TO-247
Zener - Protected SuperMESH™ MOSFET

General features

Type	V _{DSS} (@T _{jmax})	R _{DS(on)}	I _D	P _W
STB12NK80Z	800V	<0.75Ω	10.5 A	190W
STP12NK80Z	800V	<0.75Ω	10.5 A	190W
STW12NK80Z	800V	<0.75Ω	10.5 A	190W

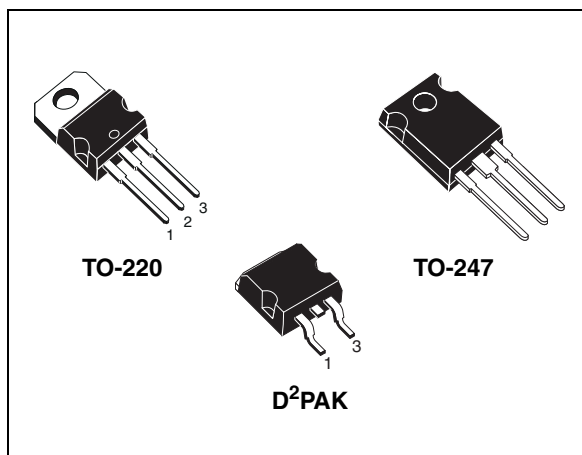
- Extremely high dv/dt capability
- Improved esd capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeability

Description

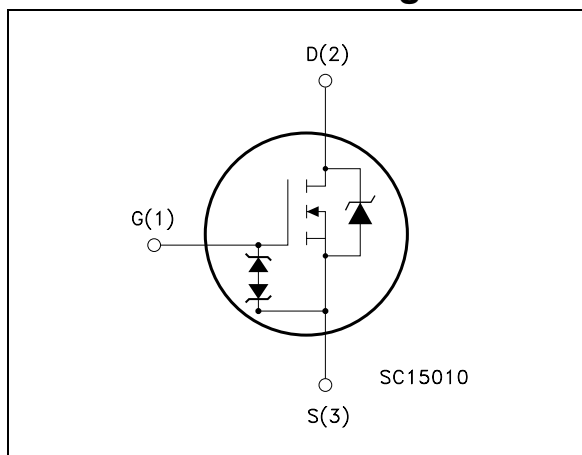
The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications.

Applications

- Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STB12NK80Z	B12NK80Z	D ² PAK	Tape & reel
STP12NK80Z	P12NK80Z	TO-220	Tube
STW12NK80Z	W12NK80Z	TO-247	Tube

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	800	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20K\Omega$)	800	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25^\circ C$	10.5	A
I_D	Drain current (continuous) at $T_C = 100^\circ C$	6.6	A
$I_{DM}^{(1)}$	Drain current (pulsed)	42	A
P_{TOT}	Total dissipation at $T_C = 25^\circ C$	190	W
	Derating Factor	1.51	W/ $^\circ C$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^\circ C$

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 10.5$ A, $di/dt \leq 200$ A/ μs , $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		TO-220/D ² PAK	TO-247	
$R_{thj-case}$	Thermal resistance junction-case Max	0.66		$^\circ C/W$
R_{thj-a}	Thermal resistance junction-ambient Max	62.5	50	$^\circ C/W$
T_l	Maximum lead temperature for soldering purpose	300		$^\circ C$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J Max)	10.5	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25^\circ C$, $I_d = I_{AR}$, $V_{dd} = 50V$)	400	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1mA, V_{GS} = 0$	800			V
I_{DSS}	Peak diode recovery voltage slope	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating},$ $T_C = 125^{\circ}C$			1 50	μA μA
I_{GSS}	Gate body leakage current ($V_{GS} = 0$)	$V_{GS} = \pm 20V$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100\mu A$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = V_{GS}, I_D = 250\mu A$	2	3	4	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15V, I_D = 5.25A$		12		S
C_{iss}	Input capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		2620		pF
C_{oss}	Output capacitance			250		pF
C_{rss}	Reverse transfer capacitance			53		pF
$C_{osseq}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0V \text{ to } 640V$		100		pF
Q_g	Total gate charge	$V_{DD} = 640V, I_D = 10.5A$		87		nC
Q_{gs}	Gate-source charge	$V_{GS} = 10V$		14		nC
Q_{gd}	Gate-drain charge	(see Figure 18)		44		nC
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400V, I_D = 5.25A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see Figure 19)		30		ns
t_r	Rise time			18		ns
$t_{d(off)}$	Off-voltage rise time			70		ns
t_f	Fall time			20		ns
$t_{r(Voff)}$	Off voltage rise time	$V_{DD} = 640V, I_D = 10.5A,$		16		ns
t_f	Fall time	$R_G = 4.7\Omega, V_{GS} = 10V$		15		ns
t_c	Cross-over time	(see Figure 19)		28		ns

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2. $C_{oss \text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				10.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				42	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=10.5A, V_{GS}=0$			1.6	V
t_{rr}	Reverse recovery time	$I_{SD}=10.5A,$ $di/dt = 100A/\mu s,$ $V_{DD}=100V, T_j=150^\circ C$		635		ns
Q_{rr}	Reverse recovery charge			5.9		μC
I_{RRM}	Reverse recovery current			18.5		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 7. Gate-source zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$BV_{GSO}^{(1)}$	Gate-Source breakdown voltage	$I_{gs}=\pm 1mA$ (Open drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220/ D²PAK

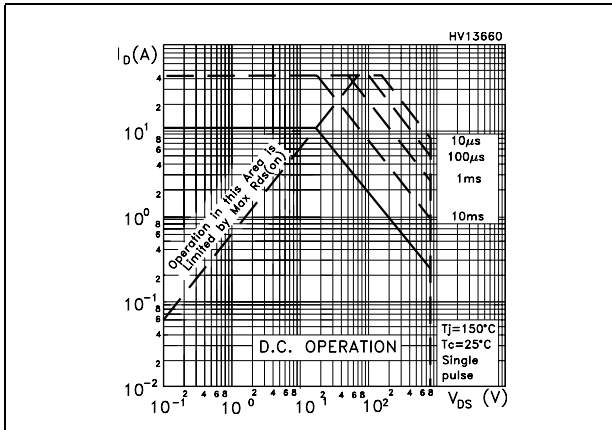


Figure 2. Thermal impedance for TO-220/ D²PAK

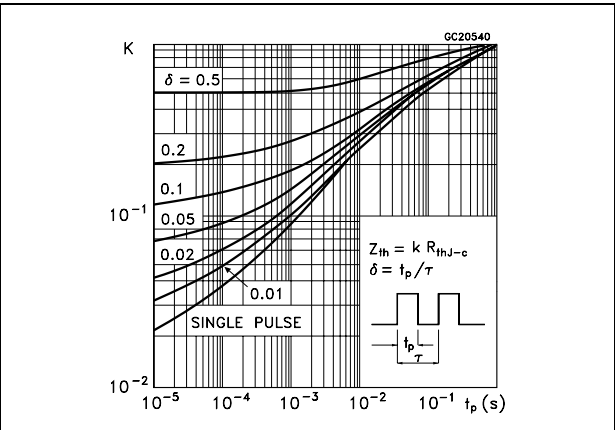


Figure 3. Safe operating area for TO-247

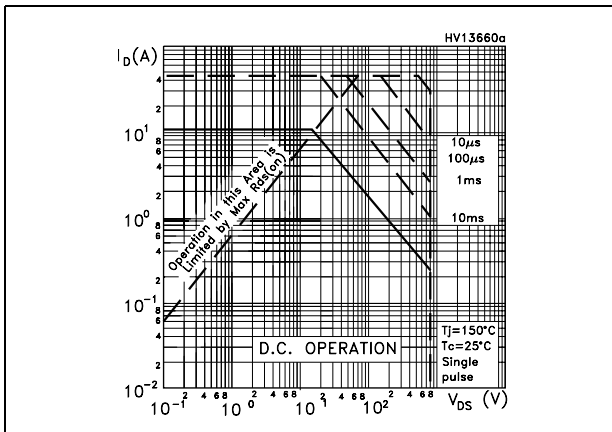


Figure 4. Thermal impedance for TO-247

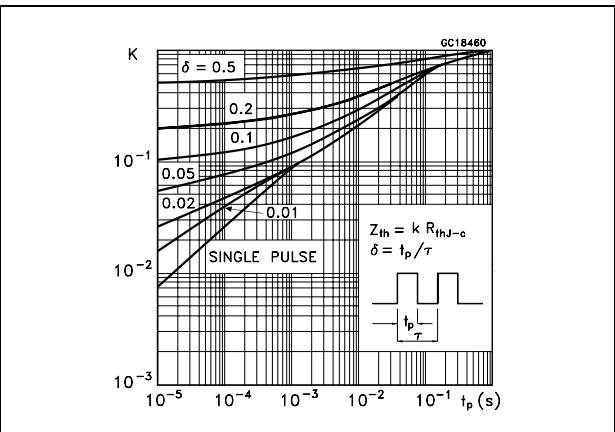


Figure 5. Output characteristics

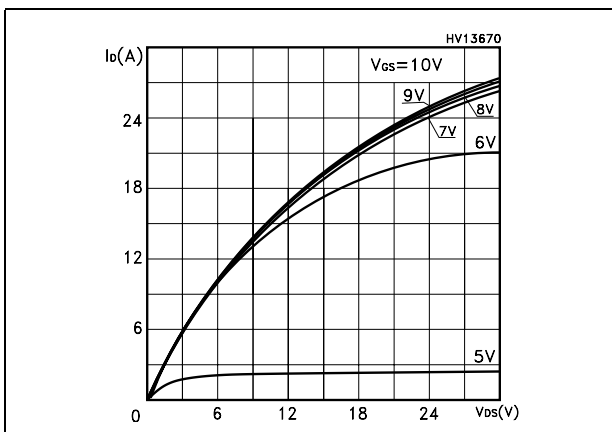


Figure 6. Transfer characteristics

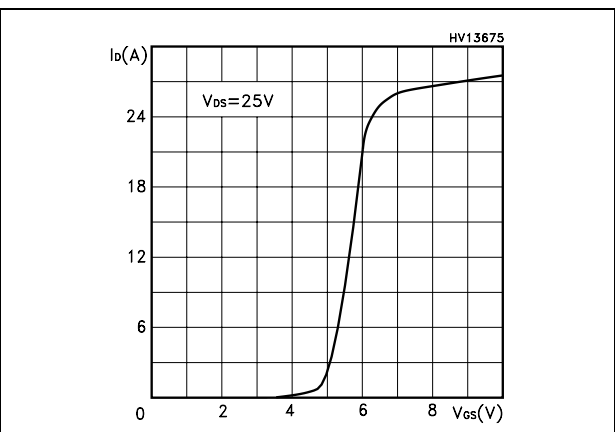


Figure 7. Transconductance

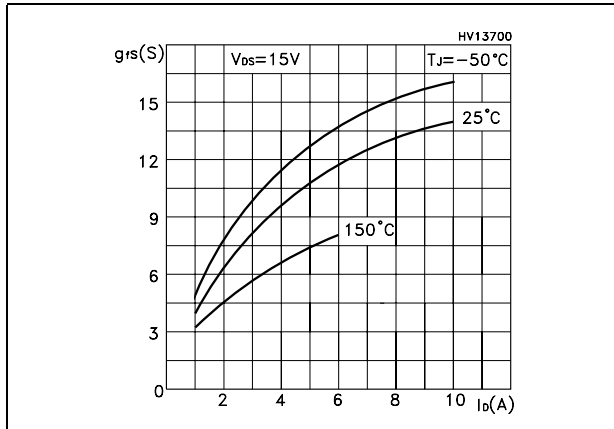


Figure 8. Static drain-source on resistance

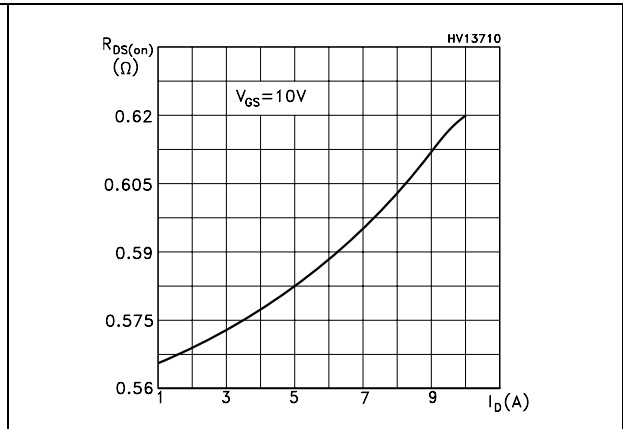


Figure 9. Gate charge vs gate-source voltage

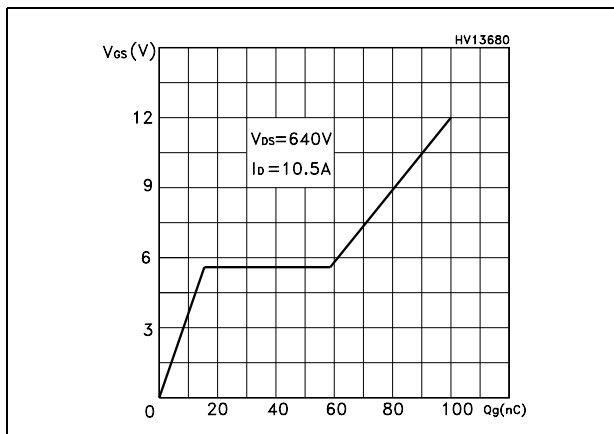


Figure 10. Capacitance variations

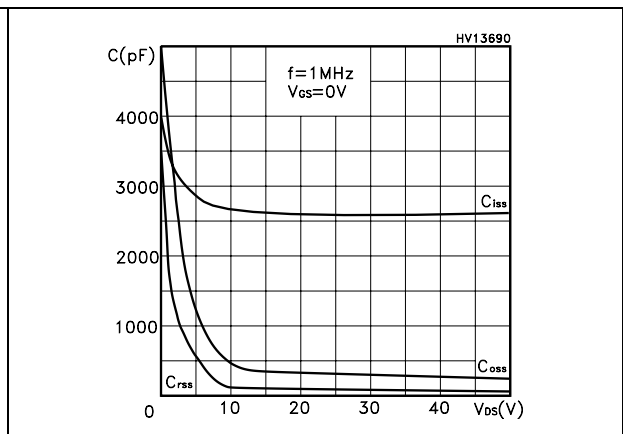


Figure 11. Normalized gate threshold voltage vs temperature

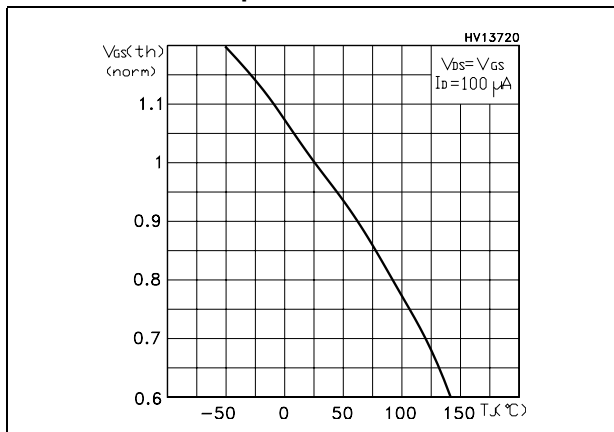


Figure 12. Normalized on resistance vs temperature

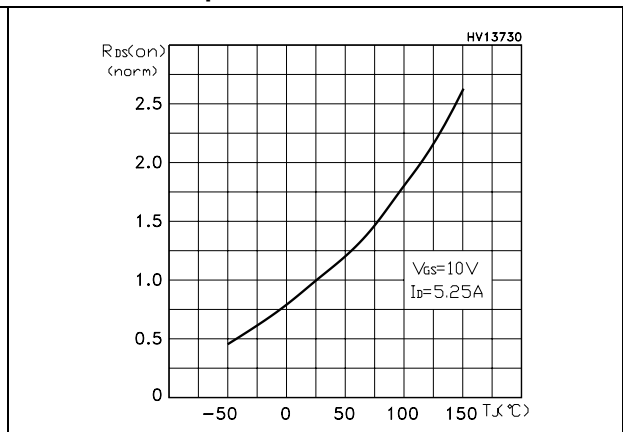


Figure 13. Source-drain diode forward characteristics

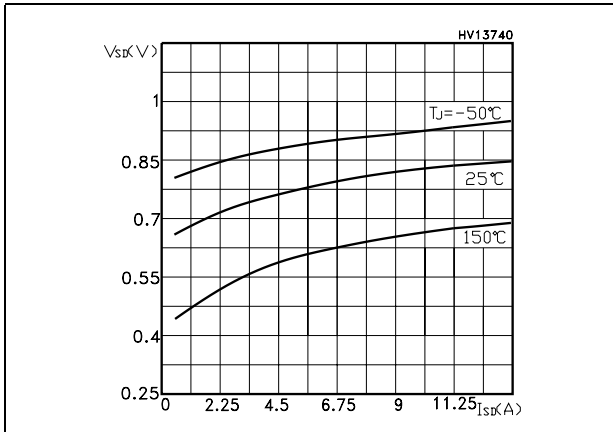


Figure 14. Normalized B_{VDSS} vs temperature

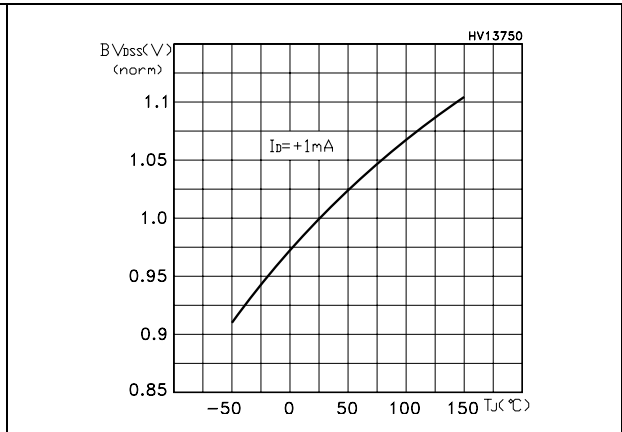
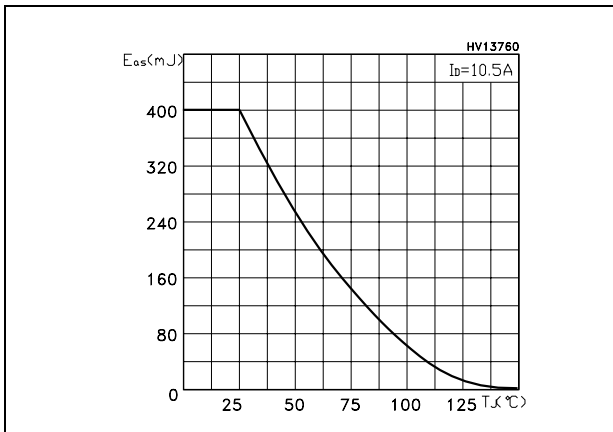


Figure 15. Maximum avalanche energy vs temperature



3 Test circuit Package mechanical data

Figure 16. Switching times test circuit for resistive load

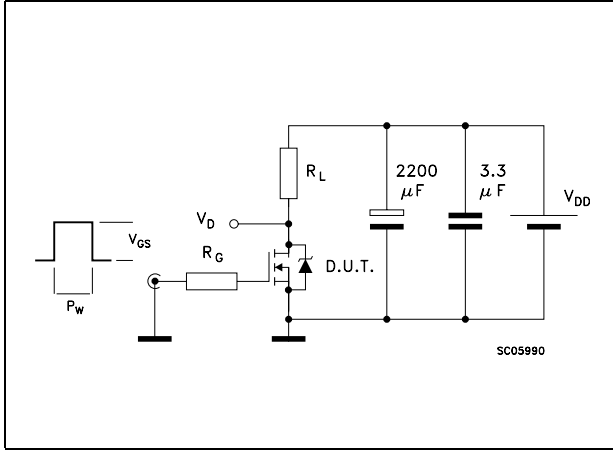


Figure 17. Gate charge test circuit

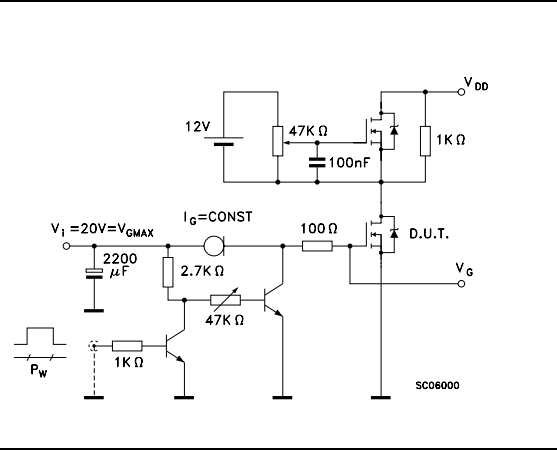


Figure 18. Test circuit for inductive load switching and diode recovery times



Figure 19. Unclamped Inductive load test circuit

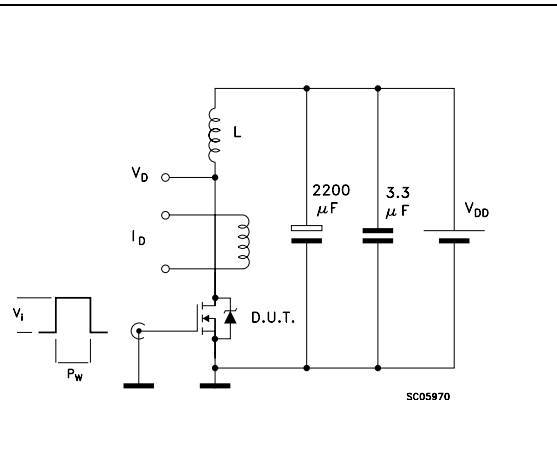
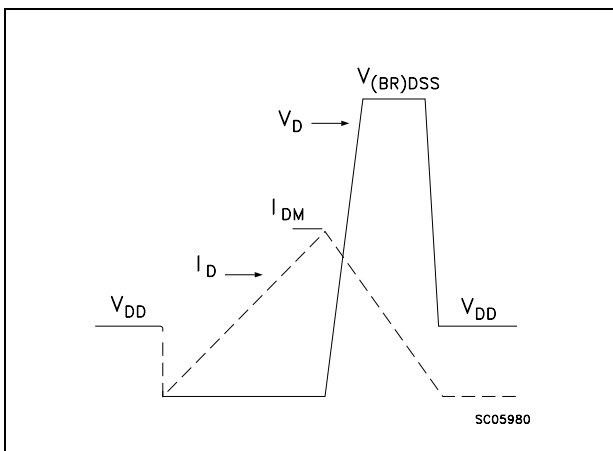


Figure 20. Unclamped inductive waveform

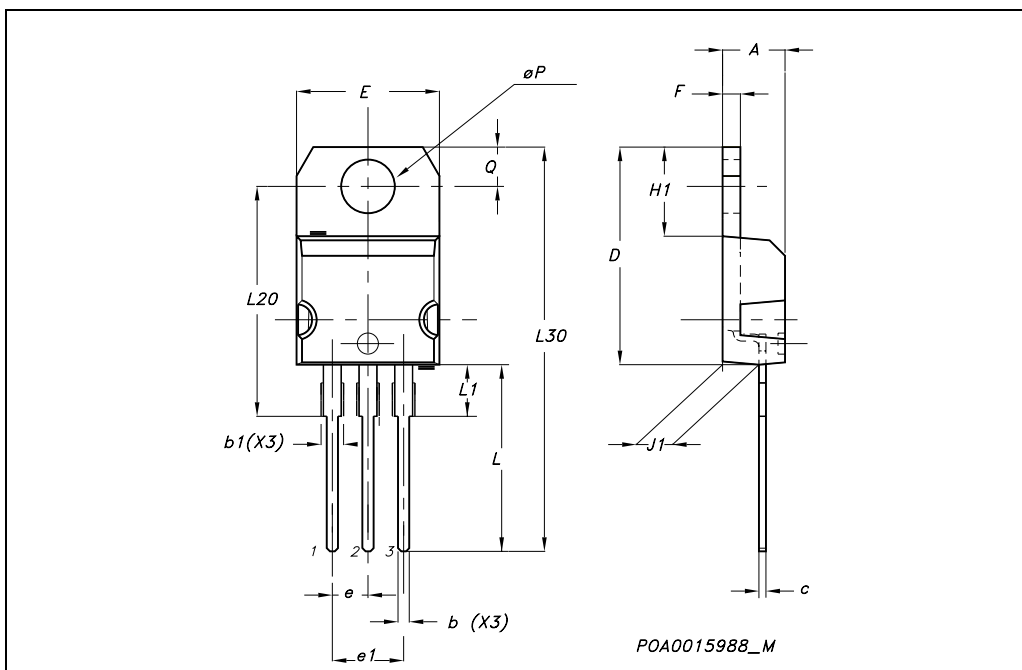


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

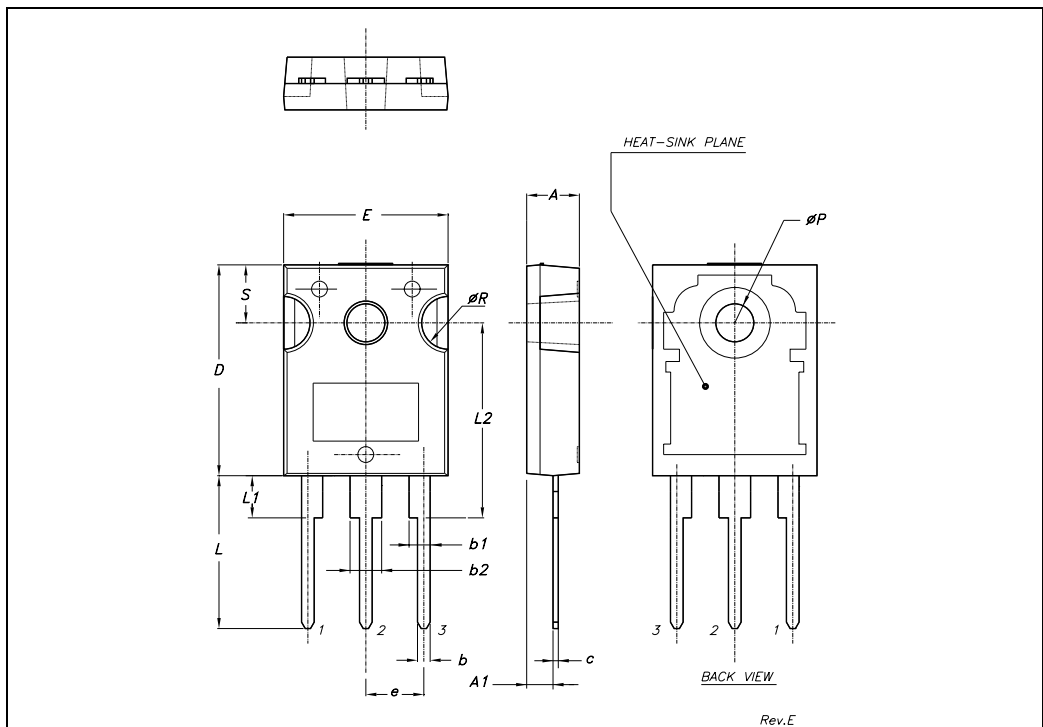
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



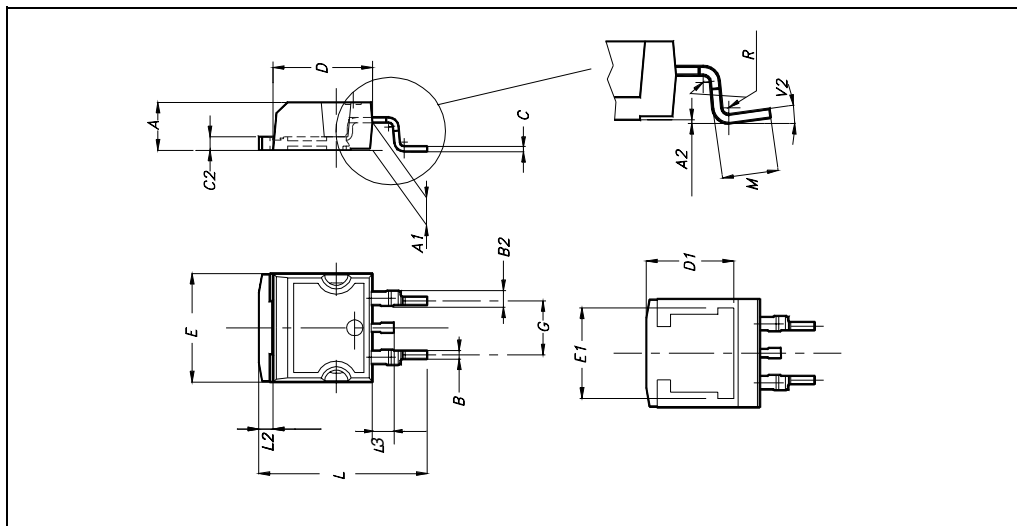
TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



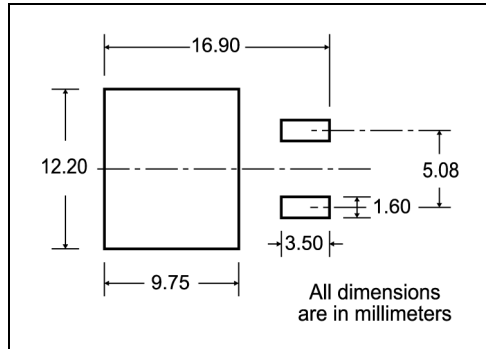
D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			



5 Packing mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956

REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

* on sales type

6 Revision history

Table 8. Revision history

Date	Revision	Changes
22-Jun-2004	2	Preliminary version
28-Jan-2005	3	Complete version
08-Sep-2005	4	<i>Figure 1</i> and <i>Figure 3</i> changed
31-Jul-2006	5	New template, no content change

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