UM11482 KITPF7100FRDMPGM evaluation board Rev. 1 – 24 September 2020

User guide



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1 Introduction

This document is the user guide for the KITPF7100FRDMPGM evaluation board, intended for the engineers involved in the evaluation, design, implementation, and validation of multichannel power management integrated circuit PF7100.

The scope of this document is to provide the user with information to evaluate the multichannel power management integrated circuit PF7100. This document covers connecting the hardware, installing the software and tools, configuring the environment and using the kit.

The customer evaluation board provides full access to all the features in the PF7100 device.

2 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for evaluation boards and its supported device(s) on http://www.nxp.com.

The information page for evaluation boards are at https://www.nxp.com/KITPF7100FRDMPGM. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a **Getting Started** tab. The **Getting Started** tab provides quick-reference information applicable to these evaluation boards, including the downloadable assets referenced in this document.

2.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, asking and answering technical questions, and receiving input on just about any embedded design topic.

The NXP community is at <u>http://community.nxp.com</u>.

3 Getting ready

Working with this evaluation board requires the kit contents, additional hardware and a Windows PC workstation with installed software.

3.1 Kit contents

- Assembled and tested evaluation board and preprogrammed FRDM-KL25Z microcontroller board in an antistatic bag
- USB-STD A to USB-B-mini cable
- Quick Start Guide

3.2 Windows PC workstation

This evaluation board requires a Windows PC workstation. Meeting these minimum specifications should produce great results when working with this evaluation board.

• USB-enabled computer with Windows 7, Windows 8, or Windows 10

3.3 Software

Installing software is necessary to work with this evaluation board.

Software package NXP_GUI_PR_revision.zip contains:

- KL25Z firmware files
- PF7100 NXPGUI Setup
- OTP mirror register read script

4 Getting to know the hardware

The NXP OTP programming boards provide an easy-to-use platform for programming the default configuration of the NXP PF7100 power management products. The boards support all voltages and signals needed for OTP programming.

4.1 Kit overview

The KITPF7100FRDMPGM is a programming board featuring a 48-pin QFN socket for PF7100 PMICs. The kit integrates all hardware needed to program the OTP registers in the PMIC.

The KITPF7100FRDMPGM integrates a communication bridge based on the FRDM-KL25Z freedom board to communicate with the NXPGUI software interface to program the OTP configuration.

4.1.1 Evaluation board features

Programming socket

Clamshell 48-pin QFN socket

System features

- 5.0 V operating input voltage range (from USB connector)
- Integrated boost converted to supply VDDOTP programming voltage
- USB to I²C communication via the FRDM-KL25Z interface
- Inline programming interface connector

4.1.2 Schematics

The board layout and bill of materials for the KITPF7100FRDMPGM are available at <u>www.nxp.com/KITPF7100FRDMPGM</u>.

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4.2 Kit featured components

Figure 5 identifies important components on the board.

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Figure 5. Evaluation board featured component locations

4.3 Default jumper configurations

Table 1.	Evaluation	board	jumper	descriptions
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Name	Default	Description
J7	Disconnected	External VIN supply
J14	Open	 Force VIN for the boost converter 1-2: disconnect VIN from the boost converter 2-3: force VIN to supply the boost converter Open: allow the MCU to control the boost input voltage supply
J8	1-2 Shorted	 KITPF7100FRDMPGM input supply selection 1-2 shorted: select USB 5 V from FRDM-KL25Z as input 3-4 shorted: select 3.3 V from FRDM-KL25Z as input
J5	Shorted	Filter capacitors for VDDOTP pin
J6	Shorted	Force VDDIO supply to 3.3 V from FRDM-KL25Z
J10	Open	 PWRON voltage selection 1-2 shorted: force PWRON high 2-3 shorted: force PWRON low Open: allows MCU to control PWRON pin
J13	Open	 TBBEN voltage selection 1-2 shorted: force TBBEN high 2-3 shorted: force TBBEN low Open: allows MCU to control TBBEN pin
J12	Open	Force VDDOTP to ground
J1, J2, J3, J4	—	Freedom board interface

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Name	Default	Description
J15	Shorted	Inline programming connector

4.4 Test points

The following test points provide access to various signals to and from the board.

 Table 2. Evaluation board test point descriptions

Name (label)	Signal name	Description
Ground test points		
TP12, TP13, TP14, TP15	GND	Ground plane test points
Digital I/O signal		
TP1	VIN	Connected to pin 27 (VIN) on socket
TP2	VDDIO	Connected to pin 9 (VDDIO) on socket
TP3	VDDOTP	Connected to pin 8 (VDDOTP) on socket
TP4	V1P5A	Connected to pin 24 (V1P5A) on socket
TP5	V1P5D	Connected to pin 28 (V1P5D) on socket
TP6	SDA	Connected to pin 10 (SDA) on PMIC. Main system I^2C bus
TP7	SCL	Connected to pin 11 (SCL) on PMIC. Main system I^2C bus.
TP8	TBBEN1	Connected to pin 32 (TBBEN) on socket
TP9	PWRON	Connected to pin 34 (PWRON) on socket
TP10	VDDOTPEN	Connected to VDDOTP enable FET on the boost converter block
TP11	TBBEN2	Connected to pin 3 (TBBEN2) on the inline programming connector; provided to support dual PMIC programming when doing inline programming

4.5 Inline programming interface configuration

In order to provide connectivity for programming of a PF7100 device on a target board, a set of jumper wires has been provided.



For systems that require inline programming capabilities, the following circuits should be provided in order to be able to interface with the KITPF7100FRDMPGM programming board via the interface connector.

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Notes:

- Inline programming interface connector may require mirror signals, depending on the cable configuration used to connect with the KITPF7100FRDMPGM programmer.
- The configuration signal might require isolation from the main system in order to allow proper communication with the PMIC during the OTP programming procedure. Such isolation may be achieved via 1x2 pin header, 0 Ω resistor or a dip switch array.
- TBBEN2 and GPIO pins in KITPF7100FRDMPGM interface connector are intended for advance system configuration. Connection is optional as needed.
- Make sure to use a connector cable that is eight inches or shorter to communicate between the KITPF7100FRDMPGM and the target board.

5 Software and firmware preparation

5.1 Installing NXPGUI on your computer

The KITPF7100FRDMPGM can use the NXPGUI for any of the PF7100 devices. Prior to the installation of the NXPGUI software and performing device firmware updates (if needed), download and unzip the NXP_GUI_PR_version.zip file to any desired location.

Open and run the NXP_GUI_version_Setup.exe file from the unzipped package. This installs the NXPGUI software in the system. Install it in a local destination folder.

The installation package is available at www.nxp.com/KITPF7100FRDMPGM.

5.2 Updating the PF7100 NXPGUI firmware

The FRDM-KL25Z freedom board is used to operate as a communication bridge to interface the NXPGUI with the PMIC and other I²C devices. The firmware is organized in three levels:

- 1. At the first level, the SDA uses the BOOTLOADER to operate as the main path to flash the functional code of the SDA processor. The BOOTLOADER is preprogrammed on the FRDM-KL25Z freedom boards and cannot be reflashed, to avoid permanent damage to the Freedom board.
- 2. At the second level, the SDA provides a *firmware loader* for quick drag-and-drop update of the KL25Z MCU firmware.
- At the third level, the KL25Z MCU provides the NXPGUI firmware. This firmware converts the USB communication into MCU instructions to control digital I/Os, as well as I²C communication to the PMIC.

If the FRDM-KL25Z is not loaded with the correct firmware to support a future software upgrade, the firmware can be updated in few simple steps.

Note: The following firmware updates are optional and can be skipped if the firmware is up-to-date.

5.2.1 Flashing the FRDM-KL25Z firmware loader

 This step is optional and should be performed only if the FRDM_KL25Z driver does not appear when the SDA port is connected. Press the push button on the Freedom board and connect the USB cable into the SDA port on the Freedom board. A new BOOTLOADER device should appear on the left pane of the file explorer.

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Figure 9. FRDM-KL25Z USB and SDA ports

- The file, *MSD-DEBUG-FRDM-KL25Z_Pemicro_v118.SDA*, should be located in the *KL25Z firmware* folder. Drag and drop this file into the BOOTLOADER drive.
- Disconnect and reconnect the USB cable into the SDA port (this time without pressing the push button). A new device called *FRDM_KL25Z* is installed on the PC.

5.2.2 Flashing the NXPGUI firmware

If a new software or silicon release requires a firmware update on the FRDM-KL25Z freedom board, use the following steps to upgrade or downgrade the firmware of the freedom board as needed. Note that this procedure is needed only to update the firmware and may be skipped if no change is needed.

- Connect the USB cable in the SDA port (without holding the push button). The PC installs a new device called FRDM_KL25Z.
- Locate the ".bin" NXPGUI driver to be installed, for example *nxp-gui-fw-frdmkl25z-usb_hid-pf7100_version.bin* and drag and drop the file into the FRDM_KL25Z driver.
- Freedom board firmware is successfully loaded.

6 Programming OTP configuration on the PF7100 PMIC

6.1 Launch NXPGUI to generate an OTP script

- 1. Open the NXPGUI application from the installation folder or from the Start menu to start the application.
- 2. The NXPGUI launcher is displayed with a list of possible configurations to load the NXPGUI. Select the appropriate option for the device and silicon revision to be used. If the device revision populated on the KITPF7100FRDMPGM is not available in the list, please contact your NXP representative to obtain the latest software update suitable for your device. Click OK to launch the NXPGUI.

NP Kit Selection	×
Select the kit,on board device(s), Kit and Devices	target MCU and USB interface
✓ KITPF502x	^
PF5020	
PF5023	
PF5024	
✓ KITPF7100	
PF7100	
✓ KITFS26	
FS26	¥
A kit for NXP PMIC evaluation	
Advanced Settings	
Feature Set	debug-i2c
Target MCU	FRDM-KL25Z
USB Interface	usb-hid
Use this configuration and Donot as	k again!
	OK Cancel

3. Set the desired OTP configuration using the OTP tab panel. If there is a predefined OTP configuration script, the user can load it by clicking on the Import button.

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Configuration Hard	ware Configuration Sec	ouencer	SW Regulate	rs LDO Regula	tors Program	n ID		Import	Save Config	- Customer D	at a la
Syst	em Configuration			1/0) Configuratio	on			<u>^</u>	Company Name*	[Company Name]
OTP_J2C_ADD OTP_J2C_CRC_EN OTP_VIN_OV.O_EN OTP_VIN_OV.O_DRNC OTP_VIN_OV.O_SOWN OTP_FALLT_MAX_CNT OTP_TIMER_FAULT	0x08 Disabled Disabled 10 µs Disabled Disabled 1 ms		910 00 910 00 910 00 910 00 910 000 910 000 910 000	WRON_MODE WRON_RST_EN WRON_RST_EN IRESET STANDBYIW PG_ACTIVE PG_CHECK (FAILB_EN	Level Sensitiv FED-32ms, R8 Shutdown on 2 s STANDBY Act GPO Mode No OV/UV che XFALLB Pio Di	e ED-32ms TRESET VIVE High Kecked at power sabled				Location Contact Name* Contact E-mal* Phone Number* Address#1* Address#2 City* Zip Code*	[Company Location] [Contact Name] [Contact E-mail] [Contact Phone Numbe [Company Address] [City] [Zip/ Postal Code]
			_9TO _9TO _9TO _9TO _9TO _9TO	EWARN_TIME	0.1 ms FSOB ignores FSOB ignores FSOB ignores FSOB ignores	v soft faults v hard faults v WDI faults v WD counter fr v				Other Info Program Dee Program Name* Application* Production Date Sample Date*	tails [Program Name] [Application Description [Targeted Production D [Require Sample Date]
Wa	tchdog monitoring			Clo	ck manageme	ent				Other Info	
OTP_WDI_MODE OTP_WDI_INV OTP_WDI_STBY_ACTIV OTP_WD_EN	Soft WD reset Faling edge of the WDI WDI disabled in STAND	* 1 * BY *	тто 0 ятто 0 ятто 0 ятто 0	_CLK_FREQ _FSYNC_RANGE _SYNCIN_EN _SYNCOUT_EN	2.500 MHz 2000KHz and 30 SYNCIN Disables SYNCOUT Disab	v 100KHz v d v led v	0000 0 0			Device Type OTP ID Part Number Target Market	PF7100-QM A0 PPF7100AMM Automotive

4. Select **OTP** from the **Export** tab in the menu and save the generated OTP file (.txt) to a known location with a desired filename.

File	View	Export	NXP	Help			
PF	710	ITO)		user-mode 🔻	Polling A	oply
		TBE HE	} K	Syste	are Configuration	Sequencer n	SW
-		OTP_I2C	_ADD		0x08	-	000
SCRI	PT	OTP_I2C	_CRC_E	N	Enabled	•	1
R	4	OTP_I2C	_SECUR	E_EN	Secure write Disabl	ed 🔻	0
PRC	G	OTP_VIN	_OVLO_	EN	Enabled	*	1
Π		OTP_VIN	_OVLO_	DBNC	100 µs	*	01
		OTP_VIN	_OVLO_	SDWN	Disabled	*	0
E	2	OTP_FAU	LT_MA)	(_CNT	Disabled	*	0000
MIRR	OR	OTP_TIM	ER_FAU	ILT	Disabled	•	1111
		OTP_FS_	BYPASS		Disabled	*	0
POW	ER	OTP_FS_I	MAX_CI	Л	16 Events	*	1111
1		OTP_FS_OK_TIMER		60 Minutes	*	111	
OT	P						

5. The script for OTP programming is ready.

(D) Computer (B) FRDM-KLZ25 USB Port (C) USB Cable Figure 10. Evaluation board setup

<u>Figure 10</u> presents a typical hardware configuration incorporating the development board and a Windows PC workstation.

To configure the hardware and workstation, complete the following procedure:

- 1. Connect the KITPF7100FRDMPGM board to the top of the Freedom KL25Z board.
 - For standalone chip programming, introduce a PF7100 QFN device in the socket (ensure pin 1 is properly aligned).
 - For inline programming, connect the interface connector to the system board and ensure VIN power is provided either from the programmer or at the system board. Ensure the SCL and SDA pins are connected only to the PMIC and isolated from the system bus. This configuration avoids the unpowered system from pulling the signal up or down, causing communication problems.
- 2. Connect the USB cable from the PC to the USB port on the Freedom board.
 - The green LED should light up.
- 3. The USB-HID connection will automatically search for the KITPF7100FRDMPGM, if a valid board is connected. This is displayed by the active Start button on the top-left corner of the GUI, then click **Start** to create a connection.

NXP G	UI - PF7100 - 3.1.57				
File Viev	v Export NXP Help				
PF71	00 Start I2C 💌	user-mode	Polling Apply	y ADDR: 0x08	
	Log Window	ØX	000 Register Map	PMIC Config	Functional Safe
ACCESS	Filter Messages 👻 🛓	LEAR RUN	iiii Functional	OTP_MIRROR	OTP_Misc

The Start button changes to a Stop button after it is clicked. The device status can be read from the bottom-left corner of the NXPGUI.

6.2 Connect the board

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Viev	v Export NXP Help											
F71	.00 Stop I2C 🔻 user-mode	e 🔻 Polling Appl	y ADDR: 0x08	- I2C	CRC: Sec	ure Write:	Enable Wa	tchdog Refre	sh Period	256 ms 🔻		N
	Log Window	1001 Register Map	PMIC Config	🛛 Fun	ctional Safety		egulators (D SW Regulato	rs 📶 AMU	IX		
	Filter Messages Filter	1001 Functional	100 OTP_MIRROR	OTP_Misc								
	PF7100 [SET_DPIN_PWRON] W :0 PF7100 [SET_DPIN_TBBEN] W :0	ID Registers			DEVICE ID	(0x00)	Read	0x80				
->	PF7100 [SET_DPIN_STANDBY] W :0	Interrupt Registers										
RIPT	PF7100 [SET_DPIN_WDI] W :0 PF7100 [SET_DPIN_PWRON] W :1	Fault Management			DEVICE							
ð	PF7100 [INT_STATUS1:0x04]R:0x18 PF7100 [INT_MASK1:0x05]R:0xff	System configuration	on		FAM[3]	FAM[2]	FAM[1]	FAM[0]	ID[3]	ID[2]	ID[1]	ID[0]
G	PF7100 [INT_SENSE1:0x06]R:0x06	Watchdog Configu	ration									
	PF7100 [INT_STATUS2:0x07]R:0x00 PF7100 [INT_MASK2:0x081R:0xff	Fault Counters			REV_ID (0x	01)	Read	0x10				
2	PF7100 [INT_SENSE2:0x09]R:0x00	AMUX Control					FULL LAVE	FULL LAVE				
	PF7100 [SW_MODE_MASK:0x0b]R:	SW1 Control			R_REV[3]	R_REV[2]	R_REV[1]	R_REV[0]	R_REV[3]	R_REV[2]	R_REV[1]	R_REV[0]
হ	PF7100 [SYS_INT:0x27]R:0x00 PF7100 [SW_ILIM_INT:0x121R:0x00	SW2 Control										
OR	PF7100 [SW_ILIM_MASK:0x13]R:0x4	SW3 Control			EMREV (0x0)2)	Read	0x00				
	PF7100 [SW_ILIM_SENSE:0x14]R:0x PF7100 [LDO_ILIM_INT:0x15]R:0x00	SW4 Control		1								
R	PF7100 [LDO_ILIM_MASK:0x16]R:0	SW5 Control			PROG_I DH[3]	PROG_I DH[2]	PROG_I DH[1]	PROG_I DH[0]	RESERVED	EMREV[2]	EMREV[1]	EMREV[0]
	PF7100 [SW_UV_INT:0x18]R:0x00	LDO1 Control]		/					
2	PF7100 [SW_UV_MASK:0x19]R:0x4f PF7100 [SW_UV_SENSE:0x1a]R:0x00	LDO2 Control			PROG_ID ()x03)	Read	0x00				
	PF7100 [SW_OV_INT:0x1b]R:0x00	VSNVS Control		1								
21	PF7100 [SW_OV_SENSE:0x1d]R:0x00	Page Select			PROG_I DL[7]	PROG_I DL[6]	PROG_I DL[5]	PROG_I DL[4]	PROG_I DL[3]	PROG_I DL[2]	PROG_I DL[1]	PROG_I DL[0]
NS	PF7100 (LDC_UV_INT:6x1e)Rc&x00 PF7100 (LDC_UV_ASK6x6x1)Rc&x03 PF7100 (LDC_UV_SENSE:0x20)Rc&x00 PF7100 (LDC_UV_INT:6x21)Rc&x00 PF7100 (LDC_UV_INT:6x22)Rc&x0 PF7100 (LDC_UV_SENSE:6x23)Rc&x1 PF7100 (PWRON_INT:6x24)Rc&x0 PF7100 (PWRON_SENSE:6x26)Rc&x1	SW1-SW4 Voltage										
	4				Select All	DEVICE_ID ((0x00)	- (4)	Read	Write	Reset	

4. If the board is properly recognized, press the Reset button on the Freedom board.

Once the device is connected, the system is ready to perform the OTP programming.

6.3 Load OTP script to program the device

There are two ways to program the PF7100 device with NXPGUI: using the **SCRIPT** tab or the **PROG** tab. The following sections introduce these two methods.

6.3.1 Program the device with SCRIPT tab

1. To begin the OTP configuration on the PMIC with the **SCRIPT** tab, select the **SCRIPT** tab and open the OTP script generated by the **OTP** Tab.

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- 2. Click the RUN button at the bottom of the **Script Commands Window**. Wait for the NXPGUI to finish the burning sequence.
- 3. To verify proper configuration of the device, stop the communication with the device, disconnect and reconnect the USB cable, and establish connection with the board again (this process is needed to ensure the PMIC has a complete power cycle and the new OTP configuration is loaded in the Mirror registers).
- 4. Click **OPEN** to load the PF7100_A0_Read_Mirror_Registers.txt file provided in the NXP_GUI_PR_version folder. Click the **RUN** button. The log is displayed in the **Script Results Window**.
- 5. The first command provides the device ID
 - PF7100 Auto QM = 0x80
 - PF7100 Auto ASILB = 0x88
- The last two commands verify the proper programing of the Mirror register sector status. If SECT_STATUS = 0x3F & FSTATUS = 0x00, the part is programmed correctly.
- 7. All other lines output the programmed value of the Mirror registers.

6.3.2 Program the device with PROG tab

1. To begin the OTP configuration on the PMIC with PROG tab, the PF7100 must first run in TBB mode. Select the tbb-mode in main menu and click the **Apply** button.

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File View	Export NXP Help					
PF71	00 Stop I2C 🔻 tbb-mode 💌 Polling	Apply ADDR: 0x08 -	I2C CRC: Secure	Write: Enable Watch	dog Refresh 📃 Perio	d 256 ms 💌
	Log Window	Device Programming				
	Filter Messages 👻 🛃 🛃	Device Programmi	ng Configuration	Fuse Box	Status	
ACCESS		Config Source	GUI	Programming Status	Sector Flags	
<> SCRIPT		Select Config Script	Browse	BUSY :	SECT_BE0 :	
-		Config Script	PF7100_BB4_OTP.txt	ERROR :	SECT_BE1:	
цф		Target State Machine	Main	ONE_ERR :	SECT_WP0 :	
PROG		Target Sector	S1	TWO_ERR :	SECT_WP1:	
		Status	completed:	PGM_FAIL :	CRC_OK0 :	
INT				PGM_FAIL_WP :	CRC_OK1:	
(A)				BOOT_ERR :		
MIRROR				VRR_ERR :		
		Program	Reset	Read		
POWER						

The PROG panel turns becomes active on TBB mode. The device status flags on the bottom bar indicates the device's current mode.

PF71	00 Stop I2C 🔻 tbb-mode	Polling Apply	ADDR: 0x08 - 12C	CRC: Secure Write:	Enable Watchdog Re	fresh Period 256 ms 🔻	N
	Log Window 🖉 🗵	Device Programming					
	Filter Messages 👻 🛃 RUN	Device Programm	ing Configuration	Fuse Box	Status		
	Pr7100 SEI_DPIR_WBDJ W 32 Pr7100 SEI_DPIR_WBDJ W 31 Pr7100 SEI_DPIR_WBDJ W 31 Pr7100 INT_STATUS:1xx04JR0 Pr7100 INT_SASK:0x06JR0.df Pr7100 INT_STATUS:2xx07F80 Pr7100 INT_STATUS:2xx07F80 Pr7100 INT_SKS22xx08JR0.df Pr7100 INT_SKS22xx08JR0.df Pr7100 INT_SKS22xx08JR0.df Pr7100 ISW_MDDE_INTSKx02R Pr7100 ISW_MDDE_MASKCh0 Pr7100 ISW_MDDE_MASKCh0 Pr7100 ISW_MDDE_MASKCh0	Config Source Select Config Script Config Script Target State Machine Target Sector Status	GUI Browse Main S1 Not Ready	Programming Status BUSY : ERROR : ONE_ERR : DNE_ERR : PGM_FAIL : PGM_FAIL WP :	Sect_BED: SECT_BED: SECT_BE1: SECT_VPD: SECT_VPD: SECT_VP1: CRC_OK0: CRC_OK1:		
	PF7100 [SW_LIM_NISKCN12]; PF7100 [SW_LIM_SENSE:0x14] PF7100 [LOD_LIM_NISKCN13]; PF7100 [LOD_LIM_MSKN215]; PF7100 [LOD_LIM_MSENSE:0x17 PF7100 [SW_UV_INT:0x18]; PF7100 [SW_UV_INT:0x18]; PF7	Program	Reset	BOOT_ERR :			
	PT100 [3W, UV_SENSEGAL 13]4 PF7100 [3W, UV_SENSEGAL 13]4 PF7100 [SW, UV_INSEGAL 13]4 PF7100 [SW, UV_INSEGAL 13]4 PF7100 [LD0_UV_INSEGAL 13]4 PF7100 [LD0_UV_INSEGAL 13]4 PF7100 [LD0_UV_ISESEGAL 23]4 PF7100 [LD0_UV_SESEGAL 23]						
	PF7100 [LDC_OV_SENSE0x23] PF7100 [PWRON_INT:0x24]R:0 PF7100 [PWRON_SENSE0x25]R PF7100 [PWRON_SENSE0x26] PF7100 [SET_DINI_TBBEN] W:1 PF7100 [SET_DINI_TSENSEN] W:0 PF7100 [SET_DINI_W10] W:0 PF7100 [SET_DINI_PWRON] W:0						

2. Go to the **PROG** tab, select the Config Source as **Script**, and click **Browse** to load the OTP script. The selected OTP script title shows up on the panel.

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Device Programming							
Device Program	ning Configuration	Fuse Box Status					
Config Source Select Config Script	Script	Programming Status	Sector Flags				
Config Script Target State Machine	PF7100_MA1_OTP_Rev B.txt		SECT_BE1:				
Target Sector Status	S1 Ready	TWO_ERR :	SECT_WP1:				
		PGM_FAIL_WP : BOOT_ERR : VRR_ERR :	CRC_OK1:				
Program	Reset	Rea	d				

3. Click the **Program** button and wait for the NXPGUI to finish the burning sequence. A pop-up window appears if the OTP programming is done.

Device Programming			
Device Programming Configuration		Fuse Box Status	
Config Source	Script 💌	Programming Status	Sector Flags
Select Config Script	Browse	BUSY :	SECT_BE0:
Config Script	PF7100_MA1_OTP_Rev B.txt	ERROR :	SECT_BE1:
Target State Machine	Main 🔻	ONE_ERR :	SECT_WP0:
Target Sector	NP PF7100	×	SECT_WP1:
Status	OTP programming cor	npleted!!!	CRC_OK0 : 📃 CRC_OK1 : 📃
	FSTATUS : 0x 3f		
	SECT_STATUS : 0x00		
Progr	am	OK	1

- 4. To verify proper configuration of the device, stop the communication with the device, disconnect and reconnect the USB cable, and establish connection with the board again. This process ensures the PMIC has a complete power cycle and the new OTP configuration is loaded in the Mirror registers).
- Go to SCRIPT tab, click OPEN to load the PF7100_A0_Read_Mirror_Registers.txt provided in the NXP_GUI_PR_version folder. Click RUN. The log prints out in the Script Results Window.
- 6. The first command provides the device ID
 - PF7100 Auto QM = 0x8

- PF7100 Auto ASILB = 0x88
- The last two commands verify the proper programing of the Mirror register sector status. If SECT_STATUS = 0x3F & FSTATUS = 0x00, the part is programmed correctly.
- 8. All other lines output the programmed value of the Mirror registers.

7 References

[1] **KITPF7100FRDMPGM** — detailed information on this board, including documentation, downloads, and software and tools

http://www.nxp.com/KITPF7100FRDMPGM

[2] **PF7100** — product information on Multichannel power management integrated circuit <u>http://www.nxp.com/PF7100</u>

8 Revision history

Revision history			
Rev	Date	Description	
v.1	20200925	Initial release	

KITPF7100FRDMPGM evaluation board

9 Legal information

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KITPF7100FRDMPGM evaluation board

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KITPF7100FRDMPGM evaluation board

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