



ELECTRONICS, INC.  
 44 FARRAND STREET  
 BLOOMFIELD, NJ 07003  
 (973) 748-5089  
<http://www.nteinc.com>

## NTE7473 Integrated Circuit TTL – Dual J–K Flip–Flop with Clear

**Description:**

The NTE7473 is a dual J–K flip–flop in a 14–Lead plastic DIP type package that contains two independent positive pulse–triggered J–K flip–flops with individual J–K clock, and direct clear inputs. J–K input is loaded into the master while the clock is high and transferred to the slave on the high–to–low transition. For this device the J and K inputs must be stable while the clock is high.

**Absolute Maximum Ratings:** (Note 1)

Supply Voltage,  $V_{CC}$  ..... 7V  
 Input Voltage ..... 5.5V  
 Operating Temperature Range,  $T_A$  ..... 0°C to +70°C  
 Storage Temperature Range,  $T_{stg}$  ..... –65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

**Recommended Operating Conditions:**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	$V_{CC}$	4.75	5.0	5.25	V
High–Level Input Voltage	$V_{IH}$	2	–	–	V
Low–Level Input Voltage	$V_{IL}$	–	–	0.8	V
High–Level Output Current	$I_{OH}$	–	–	–0.4	mA
Low–Level Output Current	$I_{OL}$	–	–	16	mA
Pulse Duration CLK High	$t_w$	20	–	–	ns
CLK Low		47	–	–	ns
$\overline{CLR}$ Low		25	–	–	ns
Input Setup Time Before CLK ↑	$t_{su}$	0	–	–	ns
Input Hold Time Data After CLK ↓	$t_h$	0	–	–	ns
Operating Temperature Range	$T_A$	0	–	+70	°C

**Electrical Characteristics:** (Note 2, Note 3)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Clamp Voltage	$V_{IK}$	$V_{CC} = \text{MIN}, I_I = -12\text{mA}$	-	-	-1.5	V
High Level Output Voltage	$V_{OH}$	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}, V_{IL} = 0.8\text{V}, I_{OH} = -0.4\text{mA}$	2.4	3.4	-	V
Low Level Output Voltage	$V_{OL}$	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}, V_{IL} = 0.8\text{V}, I_{OL} = 16\text{mA}$	-	0.2	0.4	V
Input Current	$I_I$	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$	-	-	1	mA
High-Level Input Current J or K	$I_{IH}$	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$	-	-	40	$\mu\text{A}$
$\overline{\text{CLR}}$ or CLK			-	-	80	$\mu\text{A}$
Low-Level Input Current J or K	$I_{IL}$	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$	-	-	-1.6	mA
$\overline{\text{CLR}}$			-	-	-3.2	mA
CLK			-	-	-3.3	mA
Short-Circuit Output Current	$I_{OS}$	$V_{CC} = \text{MAX}, \text{Note 4}$	-18	-	-57	mA
Supply Current	$I_{CC}$	$V_{CC} = \text{MAX}, \text{Note 5}$	-	10	20	mA

Note 2. For conditions shown as MIN or MAX, use the appropriate value specified under "Recommended Operation Conditions".

Note 3. All typical values are at  $V_{CC} = 5\text{V}, T_A = +25^\circ\text{C}$ .





Note 4. Not more than one output should be shorted at a time.

Note 5. With all outputs open,  $I_{CC}$  is measured with the Q and  $\overline{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.

**Switching Characteristics:** ( $V_{CC} = 5\text{V}, T_A = +25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Clock Frequency	$f_{\text{max}}$	$R_L = 400\Omega, C_L = 15\text{pF}$	15	20	-	MHz
Propagation Delay Time (From CLR Input to $\overline{Q}$ Output)	$t_{\text{PLH}}$		-	16	25	ns
(From $\overline{\text{CLR}}$ Input to Q Output)	$t_{\text{PHL}}$		-	25	40	ns
Propagation Delay Time (From CLK Input to Q or $\overline{Q}$ Output)	$t_{\text{PLH}}$		-	16	25	ns
	$t_{\text{PHL}}$		-	25	40	ns

**Function Table:**

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H		L	L	$Q_0$	$\overline{Q}_0$
H		H	L	H	L
H		L	H	L	H
H		H	H	Toggle	

### Pin Connection Diagram

