



## Product Change Notification / SYST-30SUPV010

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**Date:**

03-Aug-2020

**PCN Type:**

Document Change

**Notification Subject:**

ERRATA - PIC32MK General Purpose and Motor Control (GPK/MCM) with CAN FD Family Silicon Errata

**Affected CPNs:**

[SYST-30SUPV010\\_Affected\\_CPN\\_08032020.pdf](#)

[SYST-30SUPV010\\_Affected\\_CPN\\_08032020.csv](#)

**Notification Text:**

SYST-30SUPV010

Microchip has released a new Product Documents for the PIC32MK General Purpose and Motor Control (GPK/MCM) with CAN FD Family Silicon Errata of devices. If you are using one of these devices please read the document located at [PIC32MK General Purpose and Motor Control \(GPK/MCM\) with CAN FD Family Silicon Errata](#).

**Notification Status:** Final

**Description of Change:** This is the initial released version of this document.

**Impacts to Data Sheet:** None

**Reason for Change:** To Improve Productivity

**Change Implementation Status:** Complete

**Date Document Changes Effective:** 03 August 2020

**NOTE:** Please be advised that this is a change to the document only the product has not been changed.

**Markings to Distinguish Revised from Unrevised Devices:** N/A

**Attachments:**

## PIC32MK General Purpose and Motor Control (GPK/MCM) with CAN FD Family Silicon Errata

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Affected Catalog Part Numbers (CPN)

PIC32MK1024MCM064-E/MR  
PIC32MK1024GPK064-E/MR  
PIC32MK1024MCM064-E/PT  
PIC32MK1024GPK064-E/PT  
PIC32MK1024MCM100-E/PT  
PIC32MK1024GPK100-E/PT  
PIC32MK1024MCM064-I/MR  
PIC32MK1024GPK064-I/MR  
PIC32MK1024MCM064-I/PT  
PIC32MK1024GPK064-I/PT  
PIC32MK1024MCM100-I/PT  
PIC32MK1024GPK100-I/PT  
PIC32MK1024MCM064T-I/MR  
PIC32MK1024GPK064T-I/MR  
PIC32MK1024MCM064T-I/PT  
PIC32MK1024GPK064T-I/PT  
PIC32MK1024MCM100T-I/PT  
PIC32MK1024GPK100T-I/PT  
PIC32MK1024MCM064T-E/MR  
PIC32MK1024GPK064T-E/MR  
PIC32MK1024MCM064T-E/PT  
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# PIC32MK GPK/MCM Family

## PIC32MK General Purpose and Motor Control (GPK/MCM) with CAN FD Family Silicon Errata and Data Sheet Clarifications

### PIC32MK GPK/MCM with CAN FD Family Errata

The PIC32MK family of devices that you have received conform functionally to the current Device Data Sheet (DS60001519D), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. PIC32MK Family Silicon Device Identification. The silicon issues are summarized in the Table of Contents following this section.

The errata described in this document will be addressed in future revisions of the PIC32MK family silicon.

**Note:**

This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

**Table 1. PIC32MK Family Silicon Device Identification**

Devices	Device ID (DEVID[27:0])	Silicon Revision ID (DEVID[31:28])
		B2
PIC32MK1024MCM100	0x8B01053	0x3
PIC32MK1024MCM064	0x8B02053	
PIC32MK0512MCM100	0x8B04053	
PIC32MK0512MCM064	0x8B05053	
PIC32MK1024GPK100	0x8B0D053	
PIC32MK1024GPK064	0x8B0E053	
PIC32MK0512GPK100	0x8B10053	
PIC32MK0512GPK064	0x8B11053	

Data Sheet clarifications and corrections (if applicable) are located in the section [Data Sheet Clarifications](#), following the discussion of silicon issues.

## Table of Contents

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## 1. Silicon Errata Summary

Table 1-1. Errata Summary

Module	Feature	Item #	Issue Summary	Affected Revisions
				B2
Oscillator	Hardware Clock Source Selection	2.1.1	Clock source selection in hardware, that is, using the Fuse Configuration bits, FNOSC<2:0> bits (DEVCFG1 <2:0>), does not work.	X
USB	Low-speed mode	2.2.1	The USB operation in Low-Speed mode is not supported.	X
USB	VBUS pin	2.2.2	The VBUS pin is not 5V tolerant.	X
USB	VBUS	2.2.3	B-Device Session End threshold does not meet USB specification.	X
ADC	Scan Mode	2.3.1	Shared ADC7 has high Offset and Gain Error in Scan mode.	X
I <sup>2</sup> C	Speed	2.4.1	I <sup>2</sup> C master module does not meet low period of the SCL clock (t <sub>LOW</sub> ) parameter from I <sup>2</sup> C specification for clock frequency >= 400 kHz.	X
I <sup>2</sup> C	Slave	2.4.2	The 7-bit address that matches the 10-bit upper address value (111_10xx) is not accepted regardless of the STRICT bit setting.	X

## 2. Silicon Errata Issues

The following errata issues apply to the PIC32MK GPK/MCM family of devices.

**Notes:**

- An 'X' indicates the issue is present in this revision of silicon.
- Cells with a dash ('-') indicate that this silicon revision does not exist for this issue.
- Blank cells indicate an issue has been corrected or does not exist in this revision of silicon.

### 2.1 Oscillator

#### 2.1.1 Hardware Clock Source Selection

Clock source selection in hardware, that is, using the Fuse Configuration bits (FNOSC<2:0> bits (DEVCFG1 <2:0>)) or two speed start up IESO bit (DEVCFG1<7>) may not work, and the clock source would default to FRC.

**Workaround:**

Switch to desired clock source in software using the following steps:

1. Ensure Clock Switching is enabled by setting the fuse configuration bits:

```
- #pragma config FCKSM = CSECME //(enables software
    clock switch and fail safe clock monitor)
```

Or

```
- #pragma config FCKSM = CSECMD //(enables software clock switch
    but disables fail safe clock monitor)
```

2. Disable interrupts and DMA prior to the system unlock sequence.
3. Execute the system unlock sequence by writing the key values of 0xAA996655 and 0x556699AA to the SYSKEY register in two back-to-back Assembly or 'C' instructions.
4. Write the new oscillator source value to the NOSC <2:0> control bits.
5. Set the OSWEN bit in the OSCCON<0> register to initiate the clock switch.
6. Write a non-key value such as, 0x33333333 to the SYSKEY register to perform a lock. Continue to execute code that is not clock-sensitive (optional).
7. Check if the OSWEN bit is '0'. If it is, the switch was successful. Loop until the bit is '0'.
8. Re-enable interrupts and DMA.

**Affected Revisions:**

B2						
X						

### 2.2 USB

#### 2.2.1 Low-Speed Mode

The USB operation in low-speed mode is not supported.

**Workaround:**

None.

**Affected Revisions:**

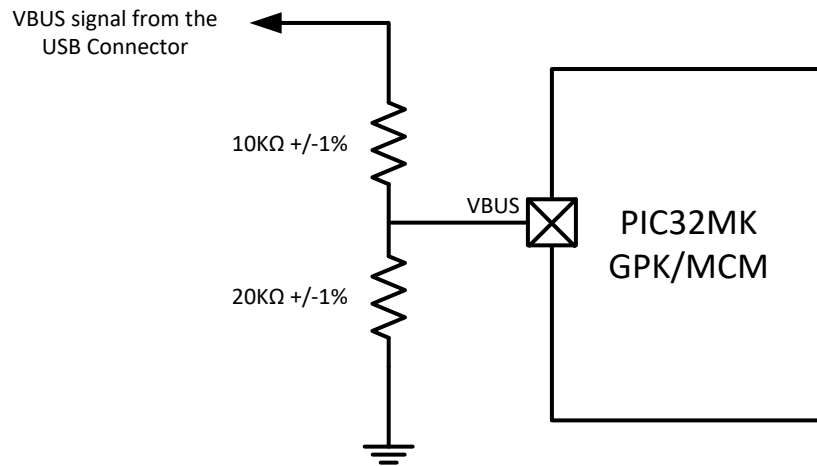
B2							
X							

### 2.2.2 VBUS pin

The VBUS pin is not 5V tolerant.

#### Workaround:

Connect an external voltage divider as shown in the following figure:



#### Affected Revisions:

B2							
X							

### 2.2.3 VBUS

The B-Device Session End threshold indicated by SESEND (UxOTGSTAT<2>) does not meet USB specification of being set at VBUS < 0.8V (maximum); instead, it is set at VBUS < 1.05V (maximum).

#### Workaround:

None.

#### Affected Revisions:

B2							
X							

## 2.3 ADC

### 2.3.1 Scan Mode

Shared ADC7 has high offset and gain error up to 38 Lsb in ADC7 Scan mode, as defined in the ADCCSS1/ADCCSS2 registers.

#### Workaround:

Increase the user-defined SAMC<9:0> bits (ADCCON2<25:16>) sample time register value by 4 T<sub>AD</sub>. This will reduce the ADC7 throughput that the user must consider, but it will reduce the gain and offset to less than 4 Lsb in 12-bit mode.

#### Affected Revisions:



B2							
X							

## 2.4 I<sup>2</sup>C

### 2.4.1 Speed

I<sup>2</sup>C master module does not meet low period of the SCL clock ( $t_{LOW}$ ) parameter from I<sup>2</sup>C specification for clock frequency  $\geq 400$  kHz.

**Workaround:**

None.

**Affected Revisions:**

B2							
X							

### 2.4.2 Slave

The 7-bit address that matches the 10-bit upper address value (111\_10xx) is not accepted regardless of the STRICT bit setting.

**Workaround:**

None.

**Affected Revisions:**

B2							
X							

### **3. Data Sheet Clarifications**

The following typographic corrections and clarifications are to be noted for the device data sheet (DS60001519D), and are showed in **BOLD** type.

There are currently no Data Sheet clarifications to report.

## **4. Revision History**

### **Revision A - June 2020**

This is the initial released version of this document.

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