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NTE74LS165
Integrated Circuit
TTL – 8–Bit Parallel–In/Serial–Out Shift Register

Description:

The NTE74LS165 is an 8–bit serial shift register in a 16–Lead plastic DIP type package that shifts the data in the direction of Q_A toward Q_H when clocked. Parallel–in access to each stage is made available by eight individual direct data inputs that are enabled by a low level at the shift/load input. This register also features gated clock inputs and complementary outputs from the eighth bit. All inputs are diode–clamped to minimize transmission–line effects, thereby simplifying system design.

Clocking is accomplished through a 2–input positive–NOR gate, permitting one input to be used as a clock inhibit function. Holding either of the clock inputs high inhibits clocking and holding either clock input low with the shift/load input high enables the other clock input. The clock inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the shift/load input is high. Data at the parallel inputs are loaded directly into the register while the shift/load input is low independently of the levels of the clock, clock inhibit, or serial inputs.

Features:

- Complementary Outputs
- Direct Overriding Load (Data) Inputs
- Gated Clock Inputs
- Parallel–to–Serial Data Conversion

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
DC Input Voltage, V_{IN} 7V
Power Dissipation, P_D 90mW
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High−Level Input Voltage	V_{IH}	2	–	–	V
Low−Level Input Voltage	V_{IL}	–	–	0.7	V
High−Level Output Current	I_{OH}	–	–	−0.4	mA
Low−Level Output Current	I_{OL}	–	–	8	mA
Clock Frequency	f_{clock}	0	–	25	MHz
Width of Clock Input Pulse Clock High	t_w(clock)	–	15	–	ns
Clock Low		–	25	–	ns
Width of Load Input Pulse Clock High	t_w(load)	25	–	–	ns
Clock Low		17	–	–	ns
Clock−Enable Setup Time	t_{su}	30	–	–	ns
Parallel Input Setup Time	t_{su}	10	–	–	ns
Serial Input Setup Time	t_{su}	20	–	–	ns
Shift Setup Time	t_{su}	45	–	–	ns
Hold Time at Any Input	t_h	0	–	–	ns
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −18mA		–	–	−1.5	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX, I_{OH} = −0.4mA		2.7	3.5	–	V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX	I_{OL} = 4mA	–	0.25	0.4	V
			I_{OL} = 8mA	–	0.35	0.5	V
Input Current	I_I	V_{CC} = MAX, V_I = 7V		–	–	0.1	mA
High Level Input Current	I_{IH}	V_{CC} = MAX, V_I = 2.7V		–	–	20	μA
Low Level Input Current	I_{IL}	V_{CC} = MAX, V_I = 0.4V		–	–	−0.4	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 4		−20	–	−100	mA
Supply Current	I_{CC}	V_{CC} = MAX, Note 5		–	18	30	mA

Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 3. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 4. Not more than one output should be shorted at a time and duration of short−circuit should not exceed one second.

Note 5. With the outputs open, clock inhibit and clock at 4.5V, and a clock pulse applied to the shift/load input. I_{CC} is measured first with the parallel inputs at 4.5V, then with the parallel inputs grounded.

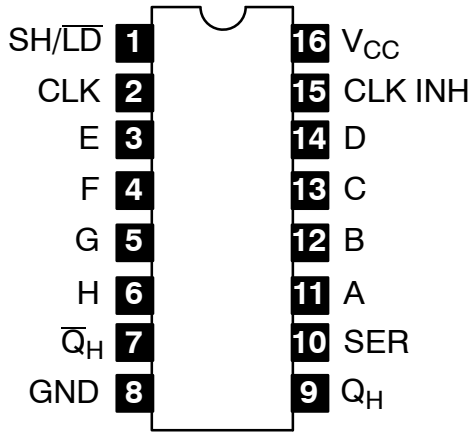
Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

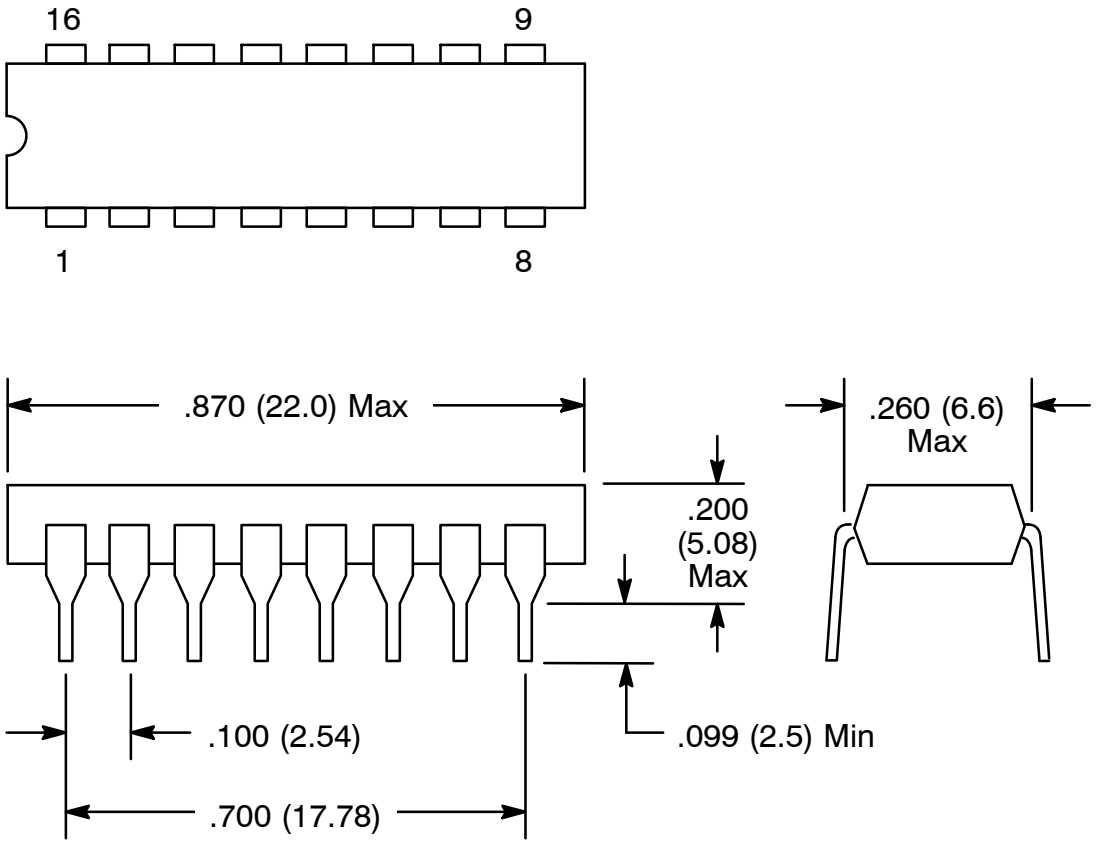
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Clock Frequency	f_{max}	R_L = 2kΩ, C_L = 15pF	25	35	–	MHz
Propagation Delay Time (From $\overline{Load}$ Input to Any Output)	t_{PLH}		–	21	35	ns
	t_{PHL}		–	26	35	ns
Propagation Delay Time (From Clock Input to Any Output)	t_{PLH}		–	14	25	ns
	t_{PHL}		–	16	25	ns
Propagation Delay Time (From H Input to Q_H Output)	t_{PLH}		–	13	25	ns
	t_{PHL}		–	24	30	ns
Propagation Delay Time (From H Input to $\overline{Q}_H$ Output)	t_{PLH}		–	19	30	ns
	t_{PHL}		–	17	25	ns

Function Table:

Inputs					Internal Outputs		Output
SHIFT/$\overline{LOAD}$	Clock Inhibit	Clock	Serial	Parallel A . . . H	Q_A	Q_B	Q_H
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

Pin Connection Diagram




16
9
1
8
.870 (22.0) Max
.260 (6.6)
Max
.200
(5.08)
Max
.100 (2.54)
.099 (2.5) Min
.700 (17.78)