



Product Change Notification / SYST-29ULYA009

Date:

16-May-2022

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - PIC18(L)F26/45/46/55/56K42 Silicon Errata and Data Sheet Clarification

Affected CPNs:

[SYST-29ULYA009_Affected_CPN_05162022.pdf](#)

[SYST-29ULYA009_Affected_CPN_05162022.csv](#)

Notification Text:

SYST-29ULYA009

Microchip has released a new Product Documents for the PIC18(L)F26/45/46/55/56K42 Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at [PIC18\(L\)F26/45/46/55/56K42 Silicon Errata and Data Sheet Clarification](#).

Notification Status: Final

Description of Change:

- Added Module 9.4 Double Sample Conversions, 13 Central Processing Unit (CPU), and 13.1 FSR Shadow Registers.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 11 May 2022

Revision History: 16 May 2022: Updated affected parts list.

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

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Affected Catalog Part Numbers (CPN)

PIC18F26K42-E/ML
PIC18F26K42-E/ML510
PIC18F26K42-E/ML511
PIC18F26K42-E/MLVAO
PIC18F26K42-E/MX
PIC18F26K42-E/SO
PIC18F26K42-E/SP
PIC18F26K42-E/SS
PIC18F26K42-E/SSVAO
PIC18F26K42-I/ML
PIC18F26K42-I/MX
PIC18F26K42-I/SO
PIC18F26K42-I/SP
PIC18F26K42-I/SS
PIC18F26K42T-E/ML511
PIC18F26K42T-E/MLVAO
PIC18F26K42T-I/ML
PIC18F26K42T-I/MX
PIC18F26K42T-I/SO
PIC18F26K42T-I/SS
PIC18F45K42-E/ML
PIC18F45K42-E/MV
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PIC18F45K42-E/PT
PIC18F45K42-I/ML
PIC18F45K42-I/MV
PIC18F45K42-I/P
PIC18F45K42-I/PT
PIC18F45K42T-E/MVV02
PIC18F45K42T-I/ML
PIC18F45K42T-I/MV
PIC18F45K42T-I/MVVAO
PIC18F45K42T-I/PT
PIC18F46K42-E/ML
PIC18F46K42-E/MV
PIC18F46K42-E/MVVAO
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PIC18LF26K42-E/SP
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PIC18LF26K42-I/MX
PIC18LF26K42-I/SO
PIC18LF26K42-I/SP
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PIC18LF26K42T-I/SO
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PIC18LF55K42T-I/MV
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PIC18LF56K42-I/MV
PIC18LF56K42-I/PT
PIC18LF56K42-I/PTC02
PIC18LF56K42T-I/MV
PIC18LF56K42T-I/PT
PIC18LF56K42T-I/PTC02



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11-May-2022

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - PIC18(L)F26/45/46/55/56K42 Silicon Errata and Data Sheet Clarification

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[SYST-29ULYA009_Affected_CPN_05112022.pdf](#)

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Attachments:

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PIC18F26Q10-E/SSVAO
PIC18F26Q10-E/SO
PIC18F26Q10-E/SOVAO
PIC18F45Q10-E/MP
PIC18F46Q10-E/MP
PIC18F46Q10-E/MPVAO
PIC18F452-E/P
PIC18F452-E/L
PIC18F452-E/ML
PIC18F452-E/PT
PIC18F452-E/PTC34
PIC18LF452-I/P
PIC18F452-I/P
PIC18F4539-I/P
PIC18LF4539-I/P
PIC18F452-I/PREL
PIC18LF452-I/L
PIC18F452-I/L
PIC18F452-I/LVAO
PIC18LF452-I/ML
PIC18F452-I/ML
PIC18LF452-I/PT
PIC18F452-I/PT
PIC18F452-I/PTC17
PIC18F452-I/PTVAO
PIC18F452T-I/L
PIC18LF452T-I/ML
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PIC18F452T-I/PTVAO
PIC18F458-E/P
PIC18F458-E/L
PIC18F458-E/PT
PIC18LF458-I/P
PIC18F458-I/P
PIC18F458-I/PREL
PIC18LF458-I/L
PIC18F458-I/L
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PIC18F458-I/PT
PIC18F458T-I/L
PIC18F458T-I/PT
PIC18F458T-I/PTVAO
PIC18F458T-E/PTVAO
PIC18LF452-I/PTC33
PIC18F2620-E/SP

PIC18F2620-E/SO
PIC18F4620-E/P
PIC18F4620-E/ML
PIC18F4620-E/PT
PIC18LF2620-I/SP
PIC18F2620-I/SP
PIC18F2620-I/SPC03
PIC18F2620-I/SPREL
PIC18F2620-I/SOB4
PIC18LF2620-I/SO
PIC18F2620-I/SO
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PIC18F4682T-I/PT022
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PIC18F4685T-E/PTV02

PIC18F2680-E/SP
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PIC18F2680-I/SO070
PIC18F2680-I/SO071
PIC18LF2680-I/SO
PIC18F2680-I/SO
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PIC18F4680-I/P
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PIC18F2680T-I/SO066
PIC18F2680T-I/SO067
PIC18F2680T-I/SO068
PIC18F2680T-I/SO070
PIC18F2680T-I/SO071
PIC18LF2680T-I/SO
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PIC18F4680T-E/PT072
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PIC18F26Q84-E/SP
PIC18F26Q83-E/SS
PIC18F26Q84-E/SS
PIC18F26Q83-E/SO
PIC18F26Q84-E/SO
PIC18F46Q83-E/NHX
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PIC18F46Q83-E/PT
PIC18F46Q84-E/PT
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PIC18F26Q84-I/5N
PIC18F26Q83-I/SP
PIC18F26Q84-I/SP
PIC18F26Q83-I/SS
PIC18F26Q84-I/SS
PIC18F26Q83-I/SO
PIC18F26Q84-I/SO
PIC18F46Q83-I/NHX
PIC18F46Q84-I/NHX
PIC18F46Q83-I/P
PIC18F46Q84-I/P
PIC18F46Q83-I/PT
PIC18F46Q84-I/PT

PIC18F26Q83T-I/5N
PIC18F26Q83T-E/5N
PIC18F26Q84T-E/SS
PIC18F26Q43-E/SP
PIC18F26Q43-E/SO
PIC18F46Q43-E/MP
PIC18F46Q43-E/P
PIC18F26Q43-E/STX
PIC18F46Q43-E/PT
PIC18LF46KS22T-I/MLV01
PIC18F46K20/WMD03
PIC18F46K20-E/P
PIC18F46K20-E/MV
PIC18F46K20-E/ML
PIC18F46K20-E/PT
PIC18F46K20-E/PTC03
PIC18F46K20-I/P
PIC18F46K20-I/MV
PIC18F46K20-I/ML
PIC18F46K20-I/MLV01
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PIC18F46K20-I/PTC06
PIC18F46K20T-I/ML
PIC18F46K20T-I/MLV01
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PIC18F46K20T-I/PT024
PIC18F46K20T-I/PT025
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PIC18F46K20T-I/PT030
PIC18F46K20T-I/PT031
PIC18F46K20T-I/PT
PIC18F46K20T-E/ML
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PIC18F26K20-E/SP
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PIC18F26J11-I/ML
PIC18LF26J11-I/SS
PIC18F26J11-I/SS
PIC18LF26J11-I/SO
PIC18F26J11-I/SO
PIC18LF46J11-I/ML
PIC18F46J11-I/ML
PIC18F45J11-I/ML
PIC18LF46J11-I/PT
PIC18F46J11-I/PT
PIC18F45J11-I/PT
PIC18F26J11T-I/ML
PIC18F26J11T-I/SS
PIC18LF46J11T-I/ML
PIC18F46J11T-I/ML
PIC18F46J11T-I/PT

PIC18F45J11T-I/PT
PIC18LF26J53-I/SP
PIC18F26J53-I/SP
PIC18LF26J53-I/ML
PIC18F26J53-I/ML
PIC18LF26J53-I/SS
PIC18F26J53-I/SS
PIC18LF26J53-I/SO
PIC18F26J53-I/SO
PIC18LF46J53-I/ML
PIC18F46J53-I/ML
PIC18LF46J53-I/PT
PIC18F46J53-I/PT
PIC18F46J53T-I/PT
PIC18LF26J13-I/SP
PIC18F26J13-I/SP
PIC18LF26J13-I/ML
PIC18F26J13-I/ML
PIC18LF26J13-I/SS
PIC18F26J13-I/SS
PIC18LF26J13-I/SO
PIC18F26J13-I/SO
PIC18LF46J13-I/ML
PIC18F46J13-I/ML
PIC18LF46J13-I/PT
PIC18F46J13-I/PT
PIC18LF45J10-I/P
PIC18F45J10-I/P
PIC18F45J10-I/PREL
PIC18LF45J10-I/ML
PIC18F45J10-I/ML
PIC18F45J10-I/PT
PIC18F45J10T-I/ML
PIC18F45J10T-I/PT
PIC18LF4553-I/PT
PIC18F4553-I/PT
PIC18F4550T-I/MLVAO
PIC18F4550T-I/PT028
PIC18LF4550T-I/PT
PIC18F4550T-I/PT
PIC18LF4550T-I/ML
PIC18F4550T-I/ML
PIC18F4520-I/PTC05
PIC18F4680T-I/PT041
PIC18F4680T-I/PT042
PIC18F4680T-I/PT043
PIC18F4680T-I/PT044
PIC18F46K40-I/PTVAO

PIC18(L)F26/45/46/55/56K42 Family Silicon Errata and Data Sheet Clarification

The PIC18(L)F26/45/46/55/56K42 family devices that you have received conform functionally to the current Device Data Sheet (DS40001919F), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).


The errata described in this document will be addressed in future revisions of the PIC18(L)F26/45/46/55/56K42 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 2](#) apply to the current silicon revision (**A3**).

Data Sheet clarifications and corrections start on [page 11](#), following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ().
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVID/REVID values for the various PIC18(L)F26/45/46/55/56K42 silicon revisions are shown in [Table 1](#).

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID<13:0> ^{(1), (2)}	Revision ID for Silicon Revision		
		A1	A2	A3
PIC18F26K42	6C60h	A001	A002	A003
PIC18F45K42	6C20h	A001	A002	A003
PIC18F46K42	6C00h	A001	A002	A003
PIC18F55K42	6BC0h	A001	A002	A003
PIC18F56K42	6BA0h	A001	A002	A003
PIC18LF26K42	6DA0h	A001	A002	A003
PIC18LF45K42	6D60h	A001	A002	A003
PIC18LF46K42	6D40h	A001	A002	A003
PIC18LF55K42	6D00h	A001	A002	A003
PIC18LF56K42	6CE0h	A001	A002	A003

Note 1: The Revision ID is located in addresses 3FFFFCh-3FFFFDh and Device ID is located in addresses 3FFFFEh-3FFFFFh.

2: Refer to the “PIC18(L)F26/45/46/55/56K42 Memory Programming Specification” (DS40001886) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item No.	Issue Summary	Affected Revisions ⁽¹⁾		
				A1	A2	A3
Electrical Specifications	SMBus 2.0	1.1	SMBus 2.0 logic levels.	X		
	SMBus 3.0	1.2	SMBus 3.0 logic levels.	X	X	X
	Min V _{DD} specification for LF devices	1.3	NVM access on LF devices may not work properly at specified voltage levels and temperatures.	X	X	X
	Fixed Voltage Reference (FVR) accuracy	1.4	FVR output tolerance may be higher than specified at temperatures below -20°C.	X	X	X
Signal Measurement Timer (SMT)	MFINTOSC clock sources into SMT	2.1	MFINTOSC clock sources into the SMT are not functional.	X	X	X
Direct Memory Access (DMA)	DMA reads from data EEPROM	3.1	DMA reads from data EEPROM does not operate.	X		
	DMA in Doze mode	3.2	DMA transfers may not work when CPU is in Doze mode.	X	X	
Universal Asynchronous Receiver Transmitter (UART)	BRGS Select	4.1	BRGS Select feature not functional in DALI mode.		X	X
	Stop bit interrupt flag	4.2	Stop bit interrupt flag functionality not available.	X		
	Auto-baud	4.3	The first character after auto-baud may be corrupted.	X	X	X
I ² C	I ² C receive buffer	5.1	Received data is transferred into the I ² CxRXB buffer on an incorrect clock edge.	X	X	X
	I ² C Start/Stop Flags	5.2	I ² C Start and/or Stop flags may be set when I ² C is enabled.	X	X	X
Nonvolatile Memory (NVM) Control	WRERR bit functionality	6.1	The WRERR bit cannot be cleared in hardware after being set once.	X	X	
Windowed Watchdog Timer (WWDT)	WWDT operation in Doze mode	7.1	Window violation occurs when WWDT operated in Doze mode.	X	X	
Power-Saving Operation Modes	Low-Power Sleep mode	8.1	Low-power Sleep mode does not operate at 3.1V < V _{DD} < 3.3V.	X	X	
Analog-to-Digital Converter with Computation (ADC ²)	ADC conversion	9.1	The 12-bit ADC shorts briefly at the beginning of the ADC conversion stage.	X		
	Burst Average mode Double Sampling	9.2	The ADC ² does not trigger the second conversion when operated in non-continuous double-sampling Burst Average mode.	X	X	
	ADC conversion in FOSC mode	9.3	ADC does not complete conversion successfully in FOSC mode.	X		
	Double Sample Conversions	9.4	An unexpected acquisition time is added between the first and second conversions.	X	X	X
Instruction Set	MOVFF/MOVSF instruction	10.1	MOVFF/MOVSF may corrupt destination.	X	X	X
Program Flash Memory	Endurance of PFM cell for LF devices	11.1	Endurance of the PFM cell is lower than specified.	X	X	X
In-Circuit Debugging (ICD)	Software breakpoints	12.1	Software breakpoints are not available.	X	X	X

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item No.	Issue Summary	Affected Revisions ⁽¹⁾		
				A1	A2	A3
Central Processing Unit (CPU)	FSR Shadow Registers	13.1	FSR Shadow Registers are not writable.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A3**).

1. Module: Electrical Specifications

1.1 SMBus 2.0

The SMBus 2.0 V_{IL} specification (Parameter D304) at 125°C is 0.7V.

Work around

None.

Affected Silicon Revisions

A1	A2	A3					
X							

1.2 SMBus 3.0

The SMBus 3.0 V_{IL} specification (Parameter D305) is temperature and V_{DD} dependent. Refer to the table below.

Temperature	V _{DD}	D305 SMBus 3.0 V _{IL} Specification
-40°C	1.8V	0.6V
-40°C	5.5V	0.8V
25°C	1.8V	0.6V
25°C	5.5V	0.8V
85°C	1.8V	0.6V
85°C	5.5V	0.7V
125°C	1.8V	0.5V
125°C	5.5V	0.7V

Work around

None.

Affected Silicon Revisions

A1	A2	A3					
X	X	X					

1.3 Min VDD Specification for LF Devices for A3 Rev

VDDMIN for LF devices has changed for temperatures below +25°C as shown below in **bold**.

PIC18LF26/45/46/55/56K42			Standard Operating Conditions (unless otherwise stated)				
PIC18F26/45/46/55/56K42							
Param. No.	Sym.	Characteristic	Min.	Typ.†	Max.	Units	Conditions
Supply Voltage							
D002	VDD		2.0	—	3.6	V	Fosc ≤ 16 MHz (-40°C to <+25°C)
			1.8	—	3.6	V	Fosc ≤ 16 MHz (≥+25°C to +125°C)
			2.5	—	3.6	V	Fosc > 16 MHz and Fosc ≤ 32 MHz
			2.7	—	3.6	V	Fosc > 32 MHz
D002	VDD		2.3	—	5.5	V	Fosc ≤ 16 MHz
			2.5	—	5.5	V	Fosc > 16 MHz and Fosc ≤ 32 MHz
			2.7	—	5.5	V	Fosc > 32 MHz

Work around

None.

Affected Silicon Revisions

A1	A2	A3					
X	X	X					

1.4 Fixed Voltage Reference (FVR) Accuracy

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

Work around

At temperatures above -20°C, the stated tolerances in the data sheet remain in effect. Operate the FVR only at temperatures above -20°C.

Affected Silicon Revisions

A1	A2	A3					
X	X	X					

2. Module: Signal Measurement Timer (SMT)

2.1 MFINTOSC Clock Sources into SMT

The Signal Measurement Timer does not operate when the MFINTOSC is selected as the clock source (i.e. CSEL = 0b100 and 0b101).

Work around

The MFINTOSC does not start up automatically. User software needs to manually enable the MFINTOSC by setting the MFOEN bit in the OSCEN register. The MFINTOSC will remain enabled as long as MFOEN bit is set.

Affected Silicon Revisions

A1	A2	A3					
X	X	X					

3. Module: Direct Memory Access (DMA)

3.1 DMA Reads from Data EEPROM

The DMA modules do not operate when configured to access the Data EEPROM (i.e., SMR<1:0> = 1x). The destination gets written to 0x00.

Work around

None. NVMCON reads work as described.

Affected Silicon Revisions

A1	A2	A3					
X							

3.2 DMA in Doze Mode

When the CPU is operated in Doze mode, DMA transfers may not work as expected.

Work around

None.

Affected Silicon Revisions

A1	A2	A3					
X	X						

4. Module: Universal Asynchronous Receiver Transmitter (UART)

4.1 Baud Rate Generator Speed Select

The Baud Rate Generator Speed Select feature (the BRGS bit in the UxCON0 register) in DALI mode is not functional. The Baud Rate Generator always operates at normal speed with 16 baud clocks per bit in DALI mode.

Work around

When using UART in DALI mode, operate the Baud Rate Generator in normal speed (BRGS = 0) only and use the following formula to calculate the UxBRGH:L register value:

$$U_xBRGH:L = \frac{F_{OSC}}{16 \times \text{Desired Baud Rate}} - 1$$

Example: To obtain the desired baud rate of 1200 at Fosc = 64 MHz,

$$U_xBRGH:L = \frac{64,000,000}{16 \times 1200} - 1 = 3332$$

Affected Silicon Revisions

A1	A2	A3					
	X	X					

4.2 Stop Bit Interrupt Flag

Stop bit interrupt flag functionality is not available in the CERIF bit in revision A1.

Work around

Use Timer2 with HLT and connect the UART RX port to the timer Reset trigger. Set the time-out period to the desired Stop bit time (for DALI mode, this is equivalent to two Stop bits at 1200 baud = 1.66 ms). When the Stop bit is received, the timer times out notifying end of data.

Affected Silicon Revisions

A1	A2	A3					
X							

4.3 Auto-Baud

When the UART is configured as follows, then the first character received after auto-baud may be corrupted:

- The UBRG registers are cleared.
- The BRGS bit is set (Fast Baud Rate mode).
- The Stop bits are configured for two Stop bits (STP = 0b1x).

Work around

- In asynchronous modes other than LIN: The transmitter may delay the first character by at least one character period after sending auto-baud.
- In all asynchronous modes including LIN: Clear the BRGS bit to select the normal baud rate mode.

Affected Silicon Revisions

A1	A2	A3					
X	X	X					

5. Module: I²C

5.1 I²C Receive Buffer

When receiving data into the receive buffer I2CxRXB, the byte is transferred into the buffer on the 9th rising clock edge rather than the expected 8th falling edge. This causes both the Receive Buffer Full (RXBF) status bit and the Receive Buffer Interrupt Flag (I2CxRXIF) to also be set on the 9th rising clock edge. The Data Write Interrupt (WRIF) and Address Interrupt Flag (ADRIF) will still be set on the 8th falling clock edge. If user software is configured to interrupt (or poll) when either the WRIF bit or the ADRIF bit is set, hardware will read an empty receive buffer, set the Receive Read Error (RXRE) status flag, and a NACK will be issued.

Work around

Do not use WRIF or ADRIF to determine when the receive buffer has received data. Instead, interrupt/poll using the I2CxRXIF interrupt bit or poll the RXBF bit. These bits are correctly set once the address/data byte has been transferred into I2CxRXB.

Affected Silicon Revisions

A1	A2	A3					
X	X	X					

5.2 I²C Start and/or Stop Flags May be Set When I²C is Enabled

When I²C is enabled, erroneous Start and/or Stop conditions may be detected. This can generate erroneous I²C interrupts if enabled.

Work around

Use the following procedure to correctly detect the Start and Stop conditions:

1. Disable Start and Stop conditions interrupt functions.
2. Enable I²C module.
3. Wait 250 ns + 6 instruction cycles (Fosc/4).
4. Clear the Start and Stop conditions interrupt flags.
5. Enable Start and Stop conditions interrupt functions if used.

```
I2CxPIEbits.SCIE = 0;
I2CxPIEbits.PCIE = 0;
I2CxCON0bits.EN = 1;
Delay();
I2CxPIRbits.SCIF = 0;
I2CxPIRbits.PCIF = 0;
I2CxPIEbits.SCIE = 1;
I2CxPIEbits.PCIE = 1;
```

Affected Silicon Revisions

A1	A2	A3					
X	X	X					

6. Module: Nonvolatile Memory (NVM) Control

6.1 WRERR Bit Functionality

When a Reset is issued while an NVM high-voltage operation is in progress, the WRERR bit in the NVMCON1 register is set as expected. After clearing the WRERR bit, if a Reset reoccurs, the WRERR bit is set again regardless of whether an NVM operation is in progress or not. A successful write operation will clear the WRERR condition.

Work around

None.

Affected Silicon Revisions

A1	A2	A3					
X	X						

7. Module: Windowed Watchdog Timer (WWDT)

7.1 WWDT Operation in Doze Mode

When the CLRWDT instruction is issued in Doze mode, a window violation error occurs in WWDT even though the window is open and armed.

Work around

Do not operate the WWDT in Doze mode.

Affected Silicon Revisions

A1	A2	A3					
X	X						

8. Module: Power-Saving Operation Modes

8.1 Low-Power Sleep Mode in F Devices

The F device resets when waking up from Sleep while in Low-Power mode (VREGPM = 1 in the VREGCON register) at $3.1V < V_{DD} < 3.3V$.

Work around

- If wake-up from Sleep is needed at $3.1V < V_{DD} < 3.3V$, operate the F device in Normal Power mode (VREGPM = 0).
- If wake-up from Sleep is needed at $3.1V < V_{DD} < 3.3V$, enable the Fixed Voltage Reference (EN = 1 in the FVRCON register). This increases the current in Sleep mode by typically 7 μA .

Affected Silicon Revisions

A1	A2	A3					
X	X						

9. Module: Analog-to-Digital Converter with Computation (ADC²)

9.1 ADC Conversion

At the very beginning of the ADC conversion, the input signal may briefly be pulled to ground, which in turn may take some charge out of the internal Sample-and-Hold capacitor. The problem is more pronounced on inputs with an impedance greater than 1 kOhm.

This issue will be seen when sampling the following internal channel inputs: FVR, DAC, and Temperature Indicator and when sampling external sources on an analog pin, including the CVD.

Work around

- When sampling the internal channel inputs, FVR, DAC, and Temperature Indicator, increase the minimum TAD time to 4 μs to increase accuracy.
- When sampling an external source through an analog pin, keep the input impedance below 1 kOhm.
- When using the ADC in CVD mode, there is no work around.

Affected Silicon Revisions

A1	A2	A3					
X							

9.2 Burst Average Mode Double Sampling

When the ADC² is operated in Burst Average mode (MD = 0b011 in the ADCON2 register) while enabling non-continuous operation and double-sampling (CONT = 0 in the ADCON0 register and DSEN = 1 in the ADCON1 register), the value in the ADCNT register does not increment beyond 0b1 toward the value in the ADRPT register.

Work around

When operating the ADC² in Burst Average mode with double-sampling, enable continuous operation of the module (CONT = 1 in the ADCON0 register) and set the Stop-On-Interrupt bit (SOI in the ADCON3 register). After the interrupt occurs, perform appropriate threshold calculations in the software and retrigger ADC² as necessary.

If the CPU is in Low-Power Sleep mode, alternatively the ADC² in non-continuous Burst Average mode can be operated with single ADC conversion (DSEN = 0 in the ADCON1 register) compromising noise immunity for lower power consumption by preventing the device from waking up to perform threshold calculations in the software.

Affected Silicon Revisions

A1	A2	A3					
X	X						

9.3 ADC Conversion in Fosc Mode

The ADCON0.GO bit remains set and the conversion does not complete successfully when configured to operate in FOSC mode (ADCON0.CS = 0) with Fosc > 40 MHz.

Work around

Use ADCRC as the ADC clock source (ADCON0.CS = 1).

Affected Silicon Revisions

A1	A2	A3					
X							

9.4 Double Sample Conversions

When enabling a Double Sample Conversion (DSEN = 1), with no Precharge time (ADPRE = 0) and no Acquisition time (ADACQ = 0), the maximum number of cycles of acquisition time is inserted prior to the second conversion.

The first conversion will be performed as expected with no Precharge time and no Acquisition time. It is only between the first and second conversions where a maximum number of cycles of Acquisition time is performed unexpectedly.

Work around

Method 1: Disable double conversion (DSEN = 0) and perform two single conversions back to back.

Method 2: If adding acquisition time is acceptable, then select no Precharge time, along with the desired Acquisition time.

Affected Silicon Revisions

A1	A2	A3					
X	X	X					

10. Module: Instruction Set

10.1 MOVFF/MOVSF Instruction

When the BSR points to the last bank of the SFR region (BSR = 0x3F) and the low byte of the source or destination address of a MOVFF/MOVSF instruction equals the low byte of an indirect addressing operation register address (INDFx, POSTINCx, POSTDECx, PREINCx, PLUSWx), the operation will not be completed as expected. Either, one or more of the destination, FSR value, or location pointed to by the FSR will be corrupted, or the move will simply not occur.

Work around

Ensure that the BSR does not point to the last bank of the SFR region (BSR = 0x3F) when the MOVFF/MOVSF instruction is being executed.

Affected Silicon Revisions

A1	A2	A3						
X	X	X						

11. Module: Program Flash Memory

11.1 Endurance of PFM Cell for LF Devices

The Flash memory cell endurance specification (Parameter MEM30) for PIC18LF26/45/46/55/56K42 devices is 1K cycles.

Work around

None.

Affected Silicon Revisions

A1	A2	A3						
X	X	X						

12. Module: In-Circuit Debugging (ICD)

12.1 Software Breakpoints

When debugging code, software breakpoints will not be available.

Work around

None.

Affected Silicon Revisions

A1	A2	A3						
X	X	X						

13. Module: Central Processing Unit (CPU)

13.1 FSR Shadow Registers

Writing to the FSR Shadow Registers does not result in accurate values being stored in the registers. Consequently, reading the FSR Shadow Registers after they have been written will return inaccurate data.

Work around

Writes to the FSR shadow registers can be performed safely using the following steps:

1. Save regular FSR2 value into RAM
2. Write the regular FSR2 with the targeted value minus the computed offset (IR[6:0] + 1, see below)
3. Write the shadow FSRxL (data doesn't matter), this will clock the shadow FSR with the FSR computed offset value.
4. Decrement FSR2 value by 1 since FSRxH increments the address by 1 (IR[6:0])
5. Write FSRxH
6. Restore the regular FSR2 from the stored RAM value.

The FSR shadow should have the value desired and the regular FSR should have the original value.

Affected Silicon Revisions

A1	A2	A3						
X	X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001919F):

Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev K Document (04/2022)

Added Module 9.4 Double Sample Conversions, 13 Central Processing Unit (CPU), and 13.1 FSR Shadow Registers.

Rev J Document (09/2021)

Added Module 5.2 I²C Start/Stop Flags.

Rev H Document (02/2021)

Added Module 11.1 Software Breakpoints. Minor corrections.

Rev G Document (11/2019)

Added Modules 1.4 Fixed Voltage Reference (FVR) Accuracy and 5.1 I²C Receive Buffer; Added Module 11 Program Flash Memory; Removed A2 rev in 9.3 (typo).

Rev F Document (03/2019)

Added silicon rev. A3. Updated Module 5.1. Added sections 4.3, 8.3 and 9.1.

Rev E Document (11/2018)

Updated Modules 3.1 and 4.1.

Data Sheet Clarifications: Deleted Module 1: Electrical Specifications.

Rev D Document (09/2018)

Updated Table 2. Updated Item 8.1.

Rev C Document (06/2018)

Updated Table 1 and Table 2; Added Module 4: UART; Module 3.2; Module 5: NVM Control; Module 6: WWDT; Module 7: Power-Saving Operation Modes; Added Module 8: ADC

Data Sheet Clarifications: Added Module 1: Electrical Specifications.

Other minor corrections.

Rev B Document (10/2017)

Added Module 3: DMA to Silicon Errata Issues. Other minor corrections.

Rev A Document (06/2017)

Initial release of this document.

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