

SN74ACT16373Q-EP

16-BIT D-TYPE TRANSPARENT LATCH WITH 3-STATE OUTPUTS

SCAS678B – MAY 2002 – REVISED JULY 2002

- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –40°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree†**
- **Member of the Texas Instruments Widebus™ Family**
- **Inputs Are TTL-Voltage Compatible**
- **3-State Bus Driving True Outputs**
- **Full Parallel Access for Loading**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, highly accelerated stress test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life.

description

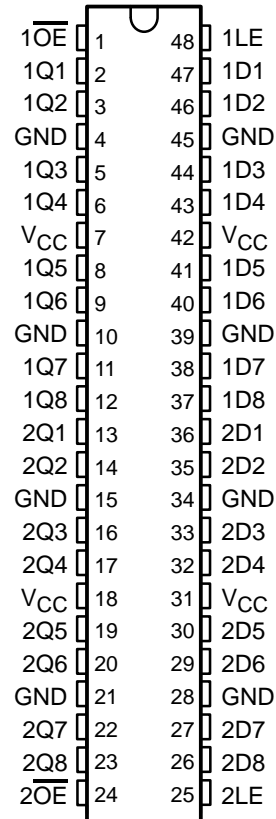
The SN74ACT16373Q-EP is a 16-bit D-type transparent latch with 3-state outputs, designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

This device can be used as two 8-bit latches or one 16-bit latch. The Q outputs of the latches follow the data (D) inputs if the latch-enable (LE) input is taken high. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines in a bus-organized system, without need for interface or pullup components.

\overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

DL PACKAGE
(TOP VIEW)



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SCAS678B – MAY 2002 – REVISED JULY 2002

ORDERING INFORMATION

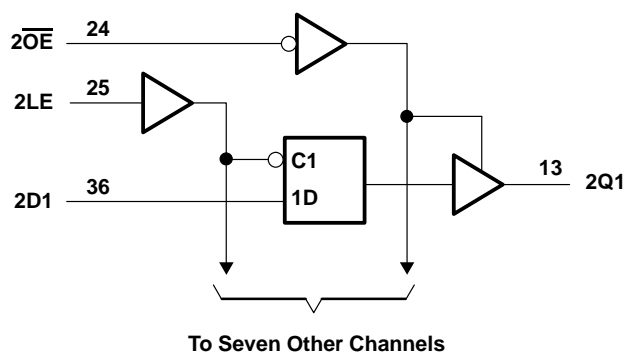
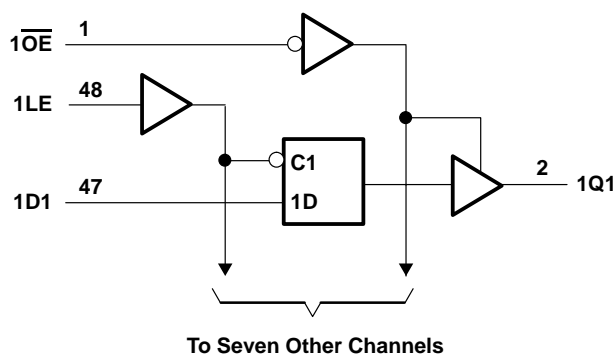
| T _A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-----------|---------------|-----------------------|------------------|
| -40°C to 125°C | SSOP – DL | Tape and reel | SN74ACT16373QDLREP | ACT16373QEP |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each section)

| INPUTS | | | OUTPUT |
|-----------------|----|---|----------------|
| \overline{OE} | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q ₀ |
| H | X | X | Z |

Logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|---|-----------------------------------|
| Supply voltage range, V _{CC} | -0.5 V to 7 V |
| Input voltage range, V _I (see Note 1) | -0.5 V to V _{CC} + 0.5 V |
| Output voltage range, V _O (see Note 1) | -0.5 V to V _{CC} + 0.5 V |
| Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC}) | ±20 mA |
| Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC}) | ±24 mA |
| Continuous output current, I _O (V _O = 0 to V _{CC}) | ±24 mA |
| Continuous current through V _{CC} or GND | ±260 mA |
| Maximum power dissipation at T _A = 55°C (in still air) (see Note 2): DL package | 1.2 W |
| Storage temperature range, T _{stg} | -65°C to 150°C |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

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SCAS678B – MAY 2002 – REVISED JULY 2002

recommended operating conditions (see Note 3)

| | | MIN | MAX | UNIT |
|-----------------|------------------------------------|-----|-----------------|------|
| V _{CC} | Supply voltage (see Note 4) | 4.5 | 5.5 | V |
| V _{IH} | High-level input voltage | 2 | | V |
| V _{IL} | Low-level input voltage | | 0.8 | V |
| V _I | Input voltage | 0 | V _{CC} | V |
| V _O | Output voltage | 0 | V _{CC} | V |
| I _{OH} | High-level output current | | -16 | mA |
| I _{OL} | Low-level output current | | 16 | mA |
| Δt/Δv | Input transition rise or fall rate | 0 | 10 | ns/V |
| T _A | Operating free-air temperature | -40 | 125 | °C |

- NOTES: 3. Unused inputs should be tied to V_{CC} through a pullup resistor of approximately 5 kΩ or greater to prevent them from floating. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
4. All V_{CC} and GND pins must be connected to the proper-voltage power supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | MIN | MAX | UNIT |
|--------------------|---|-----------------|-----------------------|-----|-----|------|-----|------|
| | | | MIN | TYP | MAX | | | |
| V _{OH} | I _{OH} = -50 μA | 4.5 V | 4.4 | | | 4.4 | | V |
| | | 5.5 V | 5.4 | | | 5.4 | | |
| | I _{OH} = -16 mA | 4.5 V | 3.94 | | | 3.7 | | |
| | | 5.5 V | 4.94 | | | 4.7 | | |
| | I _{OH} = -24 mA† | 5.5 V | | | | 3.85 | | |
| V _{OL} | I _{OL} = 50 μA | 4.5 V | 0.1 | | | 0.1 | | V |
| | | 5.5 V | 0.1 | | | 0.1 | | |
| | I _{OL} = 16 mA | 4.5 V | 0.36 | | | 0.5 | | |
| | | 5.5 V | 0.36 | | | 0.5 | | |
| | I _{OL} = 24 mA† | 5.5 V | | | | 0.5 | | |
| I _I | V _I = V _{CC} or GND | 5.5 V | ±0.1 | | | ±1 | | μA |
| I _{OZ} | V _O = V _{CC} or GND | 5.5 V | ±0.5 | | | ±10 | | μA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | 8 | | | 160 | | μA |
| ΔI _{CC} ‡ | One input at 3.4 V, Other inputs at GND or V _{CC} | 5.5 V | 0.9 | | | 1 | | mA |
| C _i | V _I = V _{CC} or GND | 5 V | 4.5 | | | | | pF |
| C _o | V _I = V _{CC} or GND | 5 V | 12 | | | | | pF |

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL-voltage levels rather than 0 V to V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

| | | T _A = 25°C | | MIN | MAX | UNIT |
|-----------------|-----------------------------|-----------------------|-----|-----|-----|------|
| | | MIN | MAX | | | |
| t _w | Pulse duration, LE high | 4 | | 4 | | ns |
| t _{su} | Setup time, data before LE↓ | 1 | | 1 | | ns |
| t _h | Hold time, data after LE↓ | 5 | | 5 | | ns |



SN74ACT16373Q-EP
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

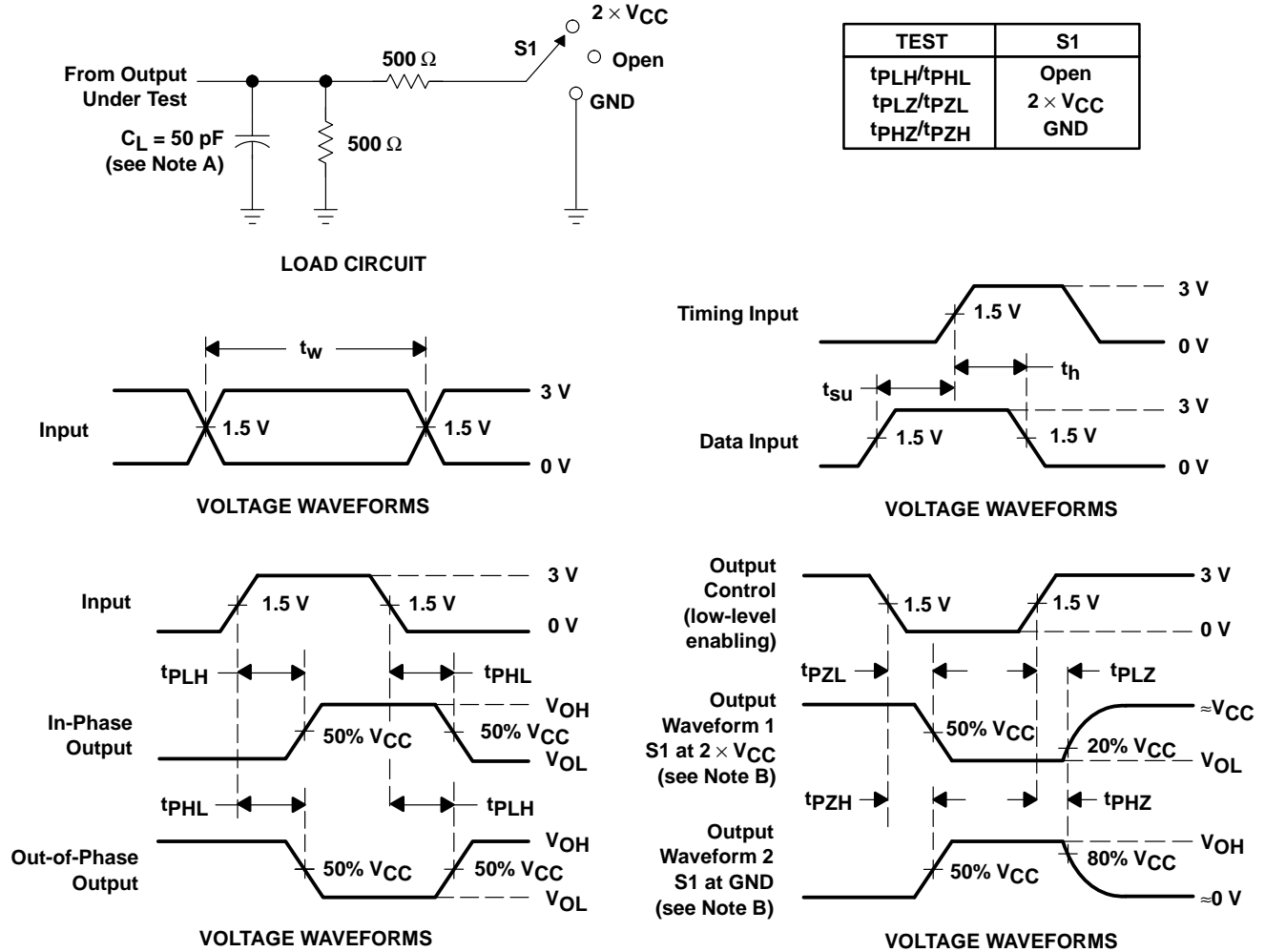
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | T _A = 25°C | | | MIN | MAX | UNIT |
|------------------|-----------------|-------------|-----------------------|-----|------|-----|------|------|
| | | | MIN | TYP | MAX | | | |
| t _{PLH} | D | Q | 3.8 | 7.9 | 9.4 | 3.8 | 11.8 | ns |
| t _{PHL} | | | 3.1 | 8.2 | 9.7 | 3.1 | 13 | |
| t _{PLH} | LE | Q | 4.6 | 9.3 | 10.8 | 4.6 | 13.7 | ns |
| t _{PHL} | | | 4.5 | 9.1 | 10.5 | 4.5 | 13 | |
| t _{PZH} | \overline{OE} | Q | 3.1 | 8 | 9.5 | 3.1 | 13 | ns |
| t _{PZL} | | | 3.8 | 9.4 | 11.1 | 3.8 | 15.1 | |
| t _{PHZ} | \overline{OE} | Q | 5.3 | 8.6 | 9.9 | 5.3 | 11 | ns |
| t _{PLZ} | | | 4.3 | 7.4 | 8.7 | 4.3 | 9.8 | |

operating characteristics, V_{CC} = 5 V, T_A = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|-----------------|---|-----------------------------------|-----------------|------|
| C _{pd} | Power dissipation capacitance per latch | C _L = 50 pF, f = 1 MHz | 43 | pF |
| | | | Outputs enabled | |
| | Outputs disabled | | 4.5 | |



PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|--------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74ACT16373QDLREP | ACTIVE | SSOP | DL | 48 | 1000 | None | Call TI | Level-1-235C-UNLIM |
| V62/03602-01XE | ACTIVE | SSOP | DL | 48 | 1000 | None | Call TI | Level-1-235C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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