**User manual** 



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## 1 Introduction

This document is the user guide for the KITFS85AEEVM evaluation board. This document is intended for the engineers involved in the evaluation, design, implementation, and validation of FS8500 Fail-safe system basis chip with multiple SMPS and LDO.

The scope of this document is to provide the user with information to evaluate the FS8500 Fail-safe system basis chip with multiple SMPS and LDO. This document covers connecting the hardware, installing the software and tools, configuring the environment and using the kit.

The KITFS85AEEVM enables development on FS84/FS85 family of devices. The kit can be connected to the FlexGUI software which allows you to play with registers, try OTP configurations, and burn the part.

This kit is suitable for truck application running at 24 V nominal. It is able to sustain up to 60 V at  $V_{\text{BAT}}.$ 

It is delivered with empty OTP content in order to leave the opportunity to the user to burn the OTP configuration. Burning the OTP three times, gives a good flexibility. The board contains a superset device (MC33FS8530AE0S), allowing tests on all the FS84/ FS85 derivatives.

## 2 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on <u>http://www.nxp.com</u>.

The information page for KITFS85AEEVM evaluation board is at <u>http://www.nxp.com/</u> <u>KITFS85AEEVM</u>. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a **Getting Started** tab. The **Getting Started** tab provides quick-reference information applicable to using the KITFS85AEEVM evaluation board, including the downloadable assets referenced in this document.

## 2.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, ask and answer technical questions, and receive input on just about any embedded design topic.

The NXP community is at http://community.nxp.com.

## 3 Getting ready

Working with the KITFS85AEEVM requires the kit contents, additional hardware and a Windows PC workstation with installed software.

## 3.1 Kit contents

- Assembled and tested evaluation board in an anti-static bag
- 3.0 ft USB-STD A to USB-B-mini cable
- Two connectors, terminal block plug, 2 pos., str. 3.81 mm
- Three connectors, terminal block plug, 3 pos., str. 3.81 mm

• Jumpers mounted on board

## 3.2 Additional hardware

In addition to the kit contents, the following hardware is necessary or beneficial when working with this kit.

• Power supply with a range of 8.0 V to 60 V and a current limit set initially to 1.0 A

## 3.3 Windows PC workstation

This evaluation board requires a Windows PC workstation. Meeting these minimum specifications should produce great results when working with this evaluation board.

• USB-enabled computer with Windows 7 or Windows 10

## 3.4 Software

Installing software is necessary to work with this evaluation board. All listed software is available on the evaluation board's information page at <u>http://www.nxp.com/</u> <u>KITFS85AEEVM</u> or from the provided link.

- FlexGUI latest version
- FS85\_FS84\_OTP\_Config.xlsm
- Java installation <a href="https://www.oracle.com/technetwork/java/javase/downloads/jre8-downloads-2133155.html">https://www.oracle.com/technetwork/java/javase/downloads/jre8-downloads-2133155.html</a>

## 4 Getting to know the hardware

The KITFS85AEEVM provides flexibility to play with all the features of the device and make measurements on the main part of the application. The KL25Z MCU installed on the board, combined with the FlexGUI software allows access to the registers in read and write mode. All regulators are accessible through connectors. Nonuser signal, like DC/DC switcher node is mapped on test points. Digital signals (SPI, I2C, RSTB, etc.) are accessible through connectors. Pin WAKE1 has a switch to control (Ignition) them. A VBAT switch is available to power On or Off the device.

This board can be operated in Emulation mode or in OTP mode. In emulation mode, as long as the power is supplied, the board configuration stays valid. The OTP mode uses the fused configuration. The device can be fused three times. In OTP mode, the device always starts with the fused configuration, except if the user wants to overwrite OTP configuration using Emulation mode. This board is able to fuse the OTP without any extra tools or board.

## 4.1 Kit overview

The KITFS85AEEVM is a hardware evaluation tool that allows performance test. The FS85xx part soldered on the board can be fused three times (see <u>Section 7.3</u> "Programming the device with an OTP configuration").

An Emulation mode is possible to test as many configurations as needed. The voltage monitoring hardware configuration is done through resistors. Note this configuration can be changed by selecting the appropriate bridges resistors:

• VMON1: assigned to VPRE, 4.1 V

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- VMON2: assigned to EXT\_MON2, (VMON bridge for 3.3 V input)
- VMON3: assigned to BUCK3, 2.3 V
- VMON4: assigned to EXT\_MON4, (VMON bridge for 5.0 V input)

This configuration can be changed by installing appropriate bridge resistors. This board was designed to sustain up to 10 A total on VPRE. Layout is done using six layer PCB stack up.

The FS84/FS85 family can be evaluated with this board as it is populated with a superset part. The FS84xx supports ASIL B design, while FS85xx supports ASIL D design.

An external LDO provides VDDI2C voltage with a choice of 1.8 V or 3.3 V (default). VDDIO is assigned by default to VDDI2C. From USB voltage, an external DC/DC generates the OTP programming voltage (8.0 V) without any need for an external power supply.

## 4.1.1 KITFS85AEEVM features

- VBAT power supply connectors (Jack and Phoenix)
- VPRE output capability up to 6.0 A (external MOSFET)
- VBUCK1/2 in Standalone (default) or Multiphase mode
- VBUCK3 up to 3.6 A peak
- VBOOST 5.0 V or 5.74 V, up to 400 mA
- LDO1 and LDO2, from 1.1 V to 5.0 V, up to 400 mA
- · Ignition key switch
- FS0B external safety pin
- Embedded USB connection for easy connection to software GUI (access to SPI/I2C bus, IOs, RSTB, FS0B, INTB, Debug, MUX\_OUT, regulators)
- · LEDs that indicate signal or regulator status
- · Support OTP fuse capabilities
- USB connection for register access, OTP emulation and programming

#### 4.1.2 VMON configuration

The VMONx configuration is highly dependent on the use case. This kit is delivered with a default configuration shown in <u>Figure 2</u>.

This configuration supports the following mapping:

- VPRE, assigned to VMON1; Bridge resistor set for 3.3 V
- BUCK2, assigned to VMON2; Bridge resistor set for 1.8 V
- BUCK3, assigned to VMON3; Bridge resistor set for 3.3 V
- LDO1, assigned to VMON4; Bridge resistor set for 3.3 V
- LDO2, assigned to VMON4; Bridge resistor set for 5.0 V

LDO1 and LDO2 use the same VMON, a reassignment is necessary to monitor both.

Due to the jumpers, VMONx can be tied to a 0.8 V to force a good voltage at pin level. This behaves like hardware disabling and makes debug easy in some cases.

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## 4.1.3 VPRE compensation network

This board is delivered with a VPRE compensation network defined for VPRE 4.1 V at 450 kHz. All other VPRE configurations require a new calculation for these components.



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Components	VPRE 450 kHz	VPRE 2.2 MHz
C18/C9	6.8 nF	1.5 nF
C59/C8	150 pF	22 pF
R32/R3	3.57 kΩ	16.9 kΩ
LPRE	4.7 μH or <b>6.8 μH</b>	<b>1.5 μH</b> , 2.2 μH or 4.7 μH

## 4.1.4 BUCK1 and BUCK2 multiphase configuration

The board is designed to work independently with BUCK1 and BUCK2. Due to R7 and R8, it is possible to connect both connectors together and work in multiphase.



## 4.1.5 SPI/I2C

The SPI and I2C buses are connected to KL25Z MCU. The user can use either one or the other. The choice can be done at start of the FlexGUI or at any time after launch (see <u>Section 8 "Using FlexGUI"</u>).

This kit uses a KL25Z MCU to communicate with FlexGUI. However, if the user wants to connect the SPI to another MCU, this is possible. In this case, remove J28 and appropriate jumpers to disconnect the KL25Z MCU (see Figure 5) and connect the external MCU on J30 connector as shown in Figure 6. In addition to this change, make sure that the VDDIO voltage domain is the same on MCU side and SBC side.

		J28		
		1	2	RSTb_SH
		3	4	FS0b_SH
		5	6	MISO_SH
		7	8	MOSI_SH
		9	10	SCLK_SH
		11	12	CSB_SH
		00		aaa-032768
Figure 5. SPI connection to KL25Z				

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## 4.1.6 VDDI2C

As an option, an external LDO is provided to feed VDDI2C. This LDO can also be used to feed VDDIO, which is the default implementation.

The I2C is compatible with 1.8 V or 3.3 V, while VDDIO is compatible with 3.3 V and 5.0 V. For this reason, the LDO default configuration is 3.3 V. The LDO is supplied by 5.0 V coming from the USB.



## 4.2 Device OTP user configuration

It is recommended to learn about OTP before operating with the device. The device has a high level of flexibility due to parameter configuration available in the OTP. This

#### KITFS85AEEVM evaluation board

impacts the functionality of the device. It is key to understand how OTP parameters can be programmed, the interaction with mirror registers and the FS85 SoC.

The OTP related operations can be performed either in Emulation mode, where the product uses a given configuration as long as power supply is not switched Off or from OTP fuse content that is valid even after a power down/power up sequence.

## 4.2.1 OTP and mirrors registers

There are two OTP blocks in the device. One is for the main section, and the other for the fail-safe. During configuration, each of them are using dedicated sectors. The OTP configuration scheme is shown in Figure 9 (same implementation for main and fail-safe).

The device can be fused three times using mirror registers. The user can first load the mirror register content with the desired contents, then decide either to use the device in Emulation mode or to burn the next sector. The first sector to be burned is S1, the second S1bis and the third S1ter. FlexGUI automatically manages the next sector to be burned. It is not possible to revert back to the previous sector. When the user reaches the sector S1ter, there no other possibility for burn, however emulation mode is still available.

**Note:** When device is operating in Emulation mode using configuration from mirror registers, few parameters must be overwritten by SPI/I2C. This concerns regulator TSD behaviors; VPRE slew rate high-side and low-side VBOOST slew rate. See <u>Section 8.4.10 "TestMode:Mirrors\_Main and TestMode:Mirrors\_Failsafe"</u> for additional details.



At boot, the content of the valid sector is loaded into the Mirror Register Sector 1. The mirror register content is accessible from FlexGUI by using specific SPI/I2C commands. The mirror configuration is managed by the FlexGUI, which eases the access.

## 4.2.2 OTP hardware implementation

To work in OTP emulation or OTP programming, it is required to start the device in Debug mode.

Figure 10 shows the sequence to be followed to enter in Debug mode. The voltage sequence on the kit is done using switches installed on the board, while the OTP registers configuration is managed by the FlexGUI GUI. This is described in detail in the following sections.

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Figure 11 shows the hardware kit implementation.



## 4.3 Kit featured components

Figure 12 identifies important components on the board and <u>Table 2</u> provides additional details on these components.

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#### Table 2. Evaluation board board component descriptions

Number	Description
1	VBAT Jack connector
2	<ul> <li>VBAT three position switch</li> <li>Left position: board supplied by Jack connector</li> <li>Middle position: board not supplied</li> <li>Right position: board supplied by Phoenix connector</li> </ul>
3	VBAT Phoenix connector
4	LDO1/LDO2 power supply
5	VPRE power supply
6	BUCK1/BUCK2 power supply

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Number	Description	
7	USB connector (for FlexGUI control)	
8	Debug connectivity. Access to: • VSUP, GND • FOUT/FIN • PGOOD/RSTB/FS0B • FCCUx • WAKE2 • PSYNC, ERRMON, AMUX • VMONx	
9	Programming • SPI bus • I2C bus • Debug pin • VPRE, VSUP, GND	
10	Wake1 switch	
11	OTP burning voltage switch	
12	VBOOST and BUCK3 power supply	
13	DEBUG voltage source either from USB (recommended) or from VSUP	
14	PGOOD LED indicator (enabled when jumper is plugged)	
15	VDDIO source from device regulators or external sources	
16	SPI, RSTB or FS0B can be disconnected between device and MCU	
17	RSTB, INTB and FS0B signals available here (device pin level)	
18	Allows to select VMON from regulators or a fix 0.8 V VDDI2C can be selected either 1.8 V or 3.3 V	

## 4.3.1 FS8500/FS8400: Fail-safe system basis chip with multiple SMPS and LDO

#### 4.3.1.1 General description

This device family is part of a global platform FS84 (fit for ASIL B) and FS85 (fit for ASIL D), pin to pin and software compatible. The FS85/FS84 is an automotive functionally safe multi-output power supply integrated circuit, with focus on Radar, Vision, ADAS domain controller, Radio and Infotainment applications. It includes multiple switch mode and linear voltage regulators. It offers external frequency synchronization input and output, for optimized system EMC performance.

The FS85/FS84 includes enhanced safety features, with fail-safe output, becoming a full part of a safety-oriented system partitioning, covering both ASIL B and ASIL D safety integrity level. It is developed in compliance with ISO 26262 standard. Several device versions are available, offering choice in number of output rails, output voltage setting, operating frequency and power up sequencing, to address multiple applications.

#### 4.3.1.2 Features

- 60 V DC maximum input voltage for 12 V and 24 V applications
- VPRE synchronous buck controller with external MOSFETs. Configurable output voltage, switching frequency, and current capability up to 10 A peak.
- Low voltage integrated synchronous BUCK1 converter, dedicated to MCU core supply with SVS capability. Configurable output voltage and current capability up to 3.6 A peak.

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- **Based on part number:** low voltage integrated synchronous BUCK2 converter. Configurable output voltage and current capability up to 3.6 A peak. Multi-phase capability with BUCK1 to extend the current capability up to 7.2 A peak on a single rail. Static voltage scaling capability.
- **Based on part number**: low voltage integrated synchronous BUCK3 converter. Configurable output voltage and current capability up to 2.5 A typical peak.
- BOOST converter with integrated low-side switch. Configurable output voltage and max input current up to 1.5 A peak.
- EMC optimization techniques including SMPS frequency synchronization, spread spectrum, slew rate control, manual frequency tuning
- 2x linear voltage regulators for MCU IOs and ADC supply, external physical layer. Configurable output voltage and current capability up to 400 mA DC.
- Standby OFF mode with very low sleep current (10 µA typ)
- 2x input pins for wake-up detection and battery voltage sensing
- Device control via 32 bits SPI or I2C interface with CRC
- Power synchronization pin to operate 2x FS85 devices or FS85 plus an external PMIC
- Scalable portfolio from ASIL B to ASIL D with independent monitoring circuitry, dedicated interface for MCU monitoring, simple and challenger watchdog function, power good, reset and interrupt, built-in self-test, fail-safe output
- Configuration by OTP programming. Prototype enablement to support custom setting during project development in engineering mode.

## 4.3.2 Indicators

The following LEDs are provided as visual output devices for the evaluation board:



Figure 13. Evaluation board indicator locations

Table 3. Evaluation board indicator of	descriptions
--	--------------

Label	Name	Color	Description	
D1	VBAT	Green	VBAT On	
D2	LDO1	Green	LDO1 On	

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## KITFS85AEEVM evaluation board

Label	Name	Color	Description
D3	LDO2	Green	LDO2 On
D4	BUCK1	Green	BUCK1 On
D6	BUCK2	Green	BUCK2 On
D7	BUCK3	Green	BUCK3 On
D8	VBOOST	Green	VBOOST On
D9	VPRE	Green	VPRE On
D11	DBG > 8.0 V	Blue	DBG pin voltage > 8.0 V (OTP programming)
D12	RSTB	Red	RSTb asserted (logic level = 0)
D13	INTB	Red	INTB asserted (logic level = 0)
D14	FS0B	Red	FS0B asserted (logic level = 0)
D15	P3V3_KL25	Green	P3V3_KL25 On
D106	PGOOD	Green	PGOOD released

## 4.3.3 Connectors

Figure 14 shows the location of connectors on the board.



## 4.3.3.1 VBAT connector (J1)

VBAT connects to the board through Phoenix connector (J1).

## Table 4. V<sub>BAT</sub> Phoenix connector (J1)

Schematic label	Signal name	Description
J1-1	VBAT	Battery voltage supply input
J1-2	GND	Ground

#### 4.3.3.2 Output power supply connectors

#### Table 5. BUCK1/BUCK2 connector (J14)

Schematic label	Signal name	Description
J14-1	BUCK2	BUCK2 power supply output
J14-2	BUCK1	BUCK1 power supply output
J14-3	GND	Ground

#### Table 6. VBOOST/BUCK3 connector (J16)

Schematic label	Signal name	Description
J16-1	VBOOST	VBOOST output
J16-2	BUCK3	BUCK3 power supply output
J16-3	GND	Ground

#### Table 7. LDO1/LDO2 connector (J2)

Schematic label	Signal name	Description
J2-1	LDO1	LDO1 power supply output
J2-2	LDO2	LDO2 power supply output
J2-3	GND	Ground

#### Table 8. VPRE connector (J3)

Schematic label	Signal name	Description
J3-1	VPRE	VPRE power supply output
J3-2	GND	Ground

## 4.3.3.3 Debug connector (J29)

#### Table 9. Debug connector (J29)

Schematic label	Signal name	Description
J29-1	FOUT	Frequency synchronization output
J29-2	FIN	Frequency synchronization input
J29-3	PGOOD	Power GOOD
J29-4	n.c.	not connected
J29-5	INTB	Interrupt, active low
J29-6	n.c.	not connected
J29-7	RSTB	Reset, active low
J29-8	n.c.	not connected
J29-9	ERRMON	Error monitoring
J29-10	n.c.	not connected
J29-11	AMUX	Analog multiplexer
J29-12	FS0B_Out	Fail-safe, active low
J29-13	VDDIO_EXT	VDDIO external reference

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Schematic label	Signal name	Description
J29-14	PSYNC	Power synchronization
J29-15	VDDIO	VDDIO used by FS85
J29-16	WAKE2_IN	Wake2 input
J29-17	FCCU1	Fault collector control unit 1
J29-18	VSUP	VSUP power supply
J29-19	FCCU2	Fault collector control unit 2
J29-20	GND	Ground

## 4.3.3.4 Program connector (J30)

Table 10. Program of	connector (J30)	
Schematic label	Signal name	Description
J30-1	WAKE1	WAKE1 input
J30-2	MOSI	SPI master output slave input
J30-3	VDDI2C	VDDI2C voltage
J30-4	MISO	SPI master input slave output
J30-5	I2C_SDA	I2C serial data
J30-6	SCLK	SPI clock
J30-7	I2C_SCL	I2C serial clock
J30-8	CSB	SPI chip select
J30-9	VDDIO_EXT	VDDIO supplied from external regulator
J30-10	VPRE	VPRE output
J30-11	DBG	Connected to Debug pin
J30-12	GND	Ground
J30-13	n.c.	not connected
J30-14	VSUP	Connected to VSUP pin
J30-15	GND	Ground
J30-16	GND	Ground

## 4.3.4 Test points

The following test points provide access to various signals to and from the board.

## KITFS85AEEVM evaluation board



#### Figure 15. Evaluation board test points

INTB

FS0B

PGOOD

#### Table 11. Evaluation board test point descriptions Test point name Description Signal name TP1 GND Ground TP2 GND Ground TP3 LDO1 LDO1 regulator output TP4 LDO2 LDO2 regulator output TP5 VPRE VPRE DC/DC regulator output GND TP6 Ground TP7 VBOOST VBOOST DC/DC output TP8 BOOST LS VBOOST low-side switcher BUCK1 SW BUCK1 switcher TP9 TP10 BUCK1 BUCK1 DC/DC regulator output TP11 BUCK3 BUCK3 DC/DC regulator output TP12 BUCK3\_SW BUCK3 switcher TP13 BUCK2 SW BUCK2 switcher **TP14** BUCK2 BUCK2 DC/DC regulator output TP19 GND Ground TP20 RSTb Reset

Interruption

Fail-safe output Power GOOD

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TP22

T26

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## 4.3.5 Jumpers



Figure 16. Evaluation board jumper locations

Name	Function	Pin number	Jumper/pin function
15	VBAT chunt	1-2	Shunt switch SW1 for current > 5.0 A
55	VDAT Shunt	3-4	Shunt switch SW1 for current > 5.0 A
16	VSLIP shunt	1-2	For current measurement (insert amperemeter)
50		3-4	For current measurement (insert amperemeter)
17	LDO1 input	1-2	LDO1_IN connected to VPRE
57		2-3	LDO1_IN connected to VBOOST
		1-2	VDDIO tied to LDO1
		3-4	VDDIO tied to LDO2
J8	VDDIO selection	5-6	VDDIO tied to VDDI2C (provided by external regulators)
		7-8	VDDIO tied to BUCK3
		9-10	VDDIO tied to VDDIO external
<b>J</b> 9	VBAT Jack	Jack	Used for VBAT supply using jack connector
111	I11 PLICK2 input	1-2	BUCK_INQ tied to VPRE
511	BOOKS liiput	2-3	BUCK_INQ tied to VBOOST
120		1-2	VMON4 tied to LDO2
520		2-3	VMON4 tied to LDO1
121		1-2	VMON1 tied to 0.8 V
521		2-3	VMON1 tied to VPRE
122		1-2	VMON2 tied to 0.8 V
522	VIVIONZ	2-3	VMON2 tied to BUCK2
123		1-2	VMON3 tied to 0.8 V
525		2-3	VMON3 tied to BUCK3

#### Table 12. Evaluation board jumper descriptions

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Name	Function	Pin number	Jumper/pin function
10.4	124 Dahur		Debug pin tied to P5V0_USB (5.0 V provided by USB connector)
JZ4	Debug	2-3	Debug pin tied to VBAT (through external protection) Do not use for OTP burning
J25	RSTB	1–2	Reset LED Enabled when jumper is plugged
J26	INTB	1–2	Interrupt LED Enabled when jumper is plugged
J27	FS0B	1–2	FS0B LED Enabled when jumper is plugged
J29	—	—	_
J30	—	—	_
J31	-	—	Use only during board manufacturing
J32	PGOOD	1–2	PGOOD LED Enabled when jumper is plugged

## 4.3.6 Switches



## Figure 17. Switch locations

#### Table 13. SW3

Position	Function	Description
RIGHT	OTP programming Off	OTP burning not possible
LEFT	OTP programming On	8.0 V on DBG pin allows OTP burning (blue LED turns On to indicate this state)

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Table 14. SW2		
Position	Function	Description
OFF	WAKE1 open	Wake1 pin not connected to $V_{\mbox{SUP}}$
ON	WAKE1 closed	Wake1 pin connected to V <sub>SUP</sub>

#### Table 15. SW1

Position	Function	Description
TOP	VBAT On	VBAT from J1
MIDDLE	VBAT Off	Board not supplied
BOTTOM	VBAT On	VBAT from J9

## 4.4 Schematic, board layout and bill of materials

The schematic, board layout and bill of materials for the KITFS85AEEVM evaluation board are available at <u>http://www.nxp.com/KITFS85AEEVM</u>.

## 5 Installing and configuring software and tools

This development kit uses FlexGUI software. FlexGUI software is based on Java JRE.

Preparing the Windows PC workstation consists of three steps.

- 1. Install the appropriate Java SE Runtime Environment (JRE).
- 2. Install Windows 7 FlexGUI driver.
- 3. Install FlexGUI software package.

## 5.1 Installing the Java JRE

- Download Java JRE (Java SE Runtime Environment), available at <u>http://www.oracle.com/technetwork/java/javase/downloads/jre8-downloads-2133155.html</u> (8u162 or newer).
- 2. Open the installer and follow the installation instructions.
- 3. Following the successful installation, restart the computer.

## 5.2 Installing Windows 7 FlexGUI driver

On Windows 7 PCs, a virtual COM port installation is required. Install the Windows 7 FlexGUI driver using the following procedure.

**Note:** On Windows 10, it is not necessary to install virtual com port as Windows 10 uses a generic COM port driver.

- 1. Connect the kit to the computer as described in <u>Section 6 "Configuring the hardware</u> <u>for startup"</u>
- 2. On the Windows PC, open the Device Manager.
- 3. In the **Device Manager** window, right-click on **SECON FLEX GUI SLAVE**, and then select **Properties**.

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4. In the SECON FLEX GUI SLAVE Properties window, click Update Driver.

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SECON FLE	X GUI SLAVE Prop	perties 🗾
General	Driver Details	
	SECON FLEX GL	JI SLAVE
	Device type:	Other devices
	Manufacturer:	Unknown
	Location:	Port_#0002.Hub_#0002
Devic The Ther To fi	e status drivers for this devic e is no driver select nd a driver for this de	e are not installed. (Code 28) ed for the device information set or element. evice, click Update Driver.
		Update Driver
		Close
		aaa-03198

5. in the Update Software Driver window, select Browse my computer for driver software.

lo	w do you want to search for driver software?	
<b>,</b>	Search automatically for updated driver software Windows will search your computer and the Internet for the latest driver software for your device, unless you've disabled this feature in your device installation settings.	
•	Browse my computer for driver software Locate and install driver software manually.	

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- 6. Select Let me pick from a list of device drivers on my computer, and then click Next.

7. Select Ports (COM & LPT) from the list, and then click Next.

Sciect your device	s type from the list	below.		
Common hardware type	S:			
Network Client			*	]
- Network Protocol				
BNetwork Service				
😹 Non-Plug and Play [	Drivers			
PCMCIA adapters				
Portable Devices	_			
Ports (COM & LPT)				
🖶 Printers	-			
Processors			=	
⊆ Proximity Devices				J
🟺 SBP2 IEEE 1394 Devi	ices			
SD host adapters				
Security Devices			-	

8. Click Have Disk.

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	In the local distance	lige to		×
$\bigcirc$	Update Driver Software - SECON FL	EX GUI SLAVE		
	Select the device driver you v Select the manufacturer and disk that contains the driver	vant to install for this hardware. model of your hardware device and then you want to install, click Have Disk.	click Next.	If you have a
	Manufacturer (Standard port types) Brother Compaq GSM Radio Card NBC This driver is digitally signed. Tell me why driver signing is imp	Model Communications Port ECP Printer Port Multiport Communications Port Printer Port	Ha	ıve Disk
			Next	Cancel

aaa-031987

9. Click Browse.

HON NO.	NOT BUT BURK Properties	X
🕞 👖 Update D	Driver Software - SECON FLEX GUI SLAVE	
Select the o	device driver you want to install for this ha	ardware.
Selec Install From	t the manufacturer and model of your hardware device n Disk	and then click Next If you
N C	Insert the manufacturer's installation disk, and then make sure that the correct drive is selected below.	OK Cancel
A B	Copy manufacturer's files from:	Browse
This drive	r is digitally signed. /hy driver signing is important	Have Disk
	_	Next Cancel
		aaa-03198

10.In the Locate File window, locate and select fsl\_ucwxp, and then click Open.

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11.In the Install from Disk window, click OK.

Install From	n Disk	X
4	Insert the manufacturer's installation disk, and then make sure that the correct drive is selected below.	OK Cancel
	Copy manufacturer's files from: C:\Users\B59702\Desktop  ✔	Browse
		aaa-0319

12.If prompted, in the **Windows Security** window, click **Select this driver software anyway**.

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13.Close the window when the installation is complete.



14.In the **Virtual Com Port Properties** window, verify that the device is working properly, and then click **Close**.

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Virtual Cor	m Port (COM47) Pr	operties	X
General	Driver Details		
1	Virtual Com Port (	COM47)	
	Device type:	Other devices	
	Manufacturer:	NXP	
	Location:	Port_#0002.Hub_#0002	
Devic	e status device is working pr	operly.	
			~
		Close	Cancel

aaa-031993

The Virtual Com Port appears in the Device Manager window.

## KITFS85AEEVM evaluation board



aaa-031994

## 5.3 Installing FlexGUI software package

The FlexGUI software installation requires only extracting the zip file in a desired location.

- 1. If necessary, install the Java JRE and Windows 7 FlexGUI driver.
- 2. Download the latest FlexGUI (32-bit or 64-bit) version, available at <u>http://www.nxp.com/KITFS85AEEVM</u>.
- Extract all the files to a desired location on your PC. FlexGUI is started by running the batch file, \bin\flexgui-app-fs85.bat.

# <figure><figure>

## 6 Configuring the hardware for startup

Figure 18 presents a typical hardware configuration incorporating the development board, power supply and Windows PC workstation.

To configure the hardware and workstation as illustrated in <u>Figure 18</u>, complete the following procedure:

1. Install jumpers for the configuration.

Γable 16. Jumper configuration					
Jumper	Configuration				
J24	connect 1-2 (connect 5.0 V on DBG pin from the USB)				

2. Configure switches for the configuration

Fable 17. Switch configuration						
Switch	Configuration					
SW1	middle position (VBAT off)					
SW2	open (WAKE1)					
SW3	open (OTP programming off)					

3. Connect the Windows PC USB port to the KITFS85AEEVM development board using the provided USB 2.0 cable.

Set the DC power supply to 12 V and current limit to 1.0 A. With power turned off, attach the DC power supply positive and negative output to KITFS85AEEVM  $V_{BAT}$  Phoenix connector (J1).

- 4. Turn on the power supply.
- 5. Close SW2.

**Note:** At this step, the product is in debug mode and all regulators are turned off. The user can then power up with OTP configuration or configure the mirror registers before power up. Power up is effective as soon as J24 jumper is removed.

## 7 Using the KITFS85AEEVM evaluation board

This section summarizes the overall setup. Detailed description is provided in the following sections.

Before starting the process, choose the mode you want to run the device.

- In Normal mode, the configuration comes from OTP fuses.
- In Debug mode, you can either use the current configuration from OTP fuse, if any, or use the OTP emulation mode to write in the mirror register.

The Normal mode or Debug mode is defined at startup depending on the DBG pin level.

- Normal mode is set by tying DBG to ground.
- Debug mode is set by setting DBG voltage to 5.0 V.

In OTP emulation, you can overwrite the mirror registers from a given OTP fuse configuration. See <u>Section 4.2.1 "OTP and mirrors registers"</u> and <u>Section 8.3 "Working</u> with the <u>Script editor"</u> to define your configuration.

In OTP fuse configuration, use the configuration fused in the OTP. So, if a valid OTP fuse configuration exists, then it is copied to the mirror registers at startup.

## 7.1 Generating the OTP configuration file

Define and generate your OTP configuration using the excel file *FS85\_FS84\_OTP\_Config.xlsm*. This file allows configuring the device for parameters controlled by the the main state machine and the fail-safe state machine.

**Note:** You can avoid this step by using a trial script (FS85\_UG\_Config.txt) available on the website.

To generate the script:

1. Fill data in the **OTP\_conf\_main\_reg** sheet.

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					MAIN	OTP_REGISTERS					
Register Name	DDRES	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BITO	Data_Bin	Data_Hez
OTP_CFG_VPRE_1	14					VPRE 10000	EV[5:0] 0 - 5 0V			00100000	0+20
OTP CEG VEBE 2	15					VPBE	SC(5:01			00100000	0420
		0	0		000111-70mV/as						
OTP_CFG_VPRE_3	16	VPREI	LIM[1:0]	VPRET	OFF[1:0]	VPRES	RLS[10]	VPRES	RHS[1:0]		
		10 - 13	20m¥	10 -	40ns	11 - PU/P	D/900mA	00 - PU/F	PD/130mA	10101100	0zAC
DTP_CFG_BOOST_	17			VPRE_MODE	Reserved		VBS1	V[3:0]		00001101	0-00
TE CES POOST	10	POOSTEN	VDCTI	CONTINEID01	U		VDCTCC14.01	0.749		00001101	020D
	10	1. Enabled	1001	0 - 60ns			01100 - 125mV/ws			10001100	0x8C
DTP CFG BOOST	19	VBSTRC	OMPI1:01	VBSTCC	OMP[1:0]	VBSTI	LIMITED	VBST	'SR(1:01		
		00 - 75	Okohms	00 -	125pF	01-	-2A	11 - 51	00V/µ.s	00000111	0x07
OTP_CFG_BUCK1_	1A					VB1V[7:0]					
DTD OFO DUOKL	10				10	1001000 - 1.25V	0000			10001000	0z88
DIP_CFG_BOCK[2	IB		otp_SPAREU	20	VBIND	0P1[10]	VBISW	150	0 - Disabled	00000110	0*06
DTP_CFG_BUCK2_	1C					VB2V[7:0]					
						10110001 - 1.8V				10110001	0xB1
DTP_CFG_BUCK2_:	1D		VB2I	NDOPT[1:0]	BUCK2EN	VB2SV	ILIM(190)	VB3_CTRL_RC	VB3_CTRL_GM		
DTR CEG PUCK2	15	PUCK2EN	VD2	JU - 1µH	1 - Enabled	11-1	4.5A	U - Liefault	U - Default	00011100	UEIC
DIF_CFG_BOCKS_	IC.	1-Enabled	VDO	10 - 10H			10101 - 3.3V			10010101	0x95
DTP_CFG_BUCK3_3	1F		VB2GMCOMP[	2:0]		VBIGMCOMP[2:0]		VB3SW	/ILIM[1:0]		
			100 - 65 GM			100 - 65 GM		11-	4.5A	10010011	0x93
OTP_CFG_LDO	20	LDO2ILIM		LD02V[2:0]		LDO1LIM		LDO1V[2:0]			
		0 - 400mA		111 - 5.0V		1 - 150mA		111 - 5.0V		01111111	0x7F
OTP_CFG_SEQ_1	21			000.5	VB2S[2:0]	01.10	000 5	VB1S[2:0]		00000000	0.00
OTP CEG SED 2	22	0	0	1-000	regulator Start and Stop I	n Slot U	000-F	regulator start and stop i	IN SIDE U	00000000	0200
		0	0	111 - Regulat	or does not Start (Enable	d by SPI/I2C)	000 - F	Regulator Start and Stop in Slot 0		00111000	0x38
OTP_CFG_SEQ_3	23	DVS_BL	CK12[1:0]	DVS_B	JCK3[1:0]	Tslot		VB3S[2:0]			
		00 - 7.8	lm∀łµs	00 - 10	lm∀łµs	0 - 250µs	000 - F	Regulator Start and Stop i	in Slot 0	00000000	0x00
DTP_CFG_CLOCK_	24				VPRE_ph[2:0]		400	CLK_DIV2[2:0]	201-	00000400	0.04
DTD OFO OLOOK	05	U	U		DUO - delay U		100	divide by 44 - CLK2=400	ok Hz	00000100	0204
DIP_CFG_CLOCK_	25	0	0		110 dolou 6			000_dolar/0		00110000	0=20
TTP. CEG. CLOCK	26				BUCK3 pb[2:0]			BUCK2 pb[2:0]		00110000	04.50
		0	0		011 - delau 3			000 - delau 0		00011000	0z18
DTP_CFG_CLOCK_	27	BUCK3_clk_sel	BUCK2_clk_sel	BUCK1_clk_sel	VBST_clk_sel	VPRE_clk_sel	PLL_sel	CLK_I	DIV1[1:0]		
		0 - CLK1	0 - CLK1	0 - CLK1	0 - CLK1	1 - CLK2	0 - Disabled	10 - divide by 9	- CLK1=2.22MHz	00001010	0x0A
OTP_CFG_SM_1	28					conf_	tsd[5:0]		1		
OTD OFO ON A	20	0		U-BUUS [Shutdown	1-BUCK1Shutdown +	U - BUCK2 Shutdown	1 - BUCK3 Shutdown +	U - LUUI Shutdown	0 - LUU2 Shutdown	00010100	Uz14
UIF_CFG_SM_2	29		orp_SPARE1[2	20	1.22mc	Autoretry_infinite	Autoretry_en	0.245205	PorNU_EN 0. Disabled	00011100	8=10
TTP. CEG. VSUP. U	24		000		oto SPARE216	Sol	I I Litabled	0-240000	VSUPCEG	00011100	- Offic
	-0				0000000				0 - 4.9V for Vpre < 4.5V	00000000	0z00
OTP_CFG_I2C	2B						M_I2CDEV	ADDR[3:0]			
		0	0	0	0		0001 - Ad	idress D1		00000001	8z01
OTP_CFG_OV	2C		-		-		1	/DDIO_REG_ASSIGN[2:	0]		
070 000 000		0	0	0	0	0		100 - BUCK3		00000100	8x04
UTP_CFG_DEVID	20					JeviceID[7:0]				00000001	0.04
TR M SLCPC 18	25				OTP N	00000001 4 S1 CDC 1 SD[7:0]				00000001	0201
THE ME AL CHE LS	٤E				Automatica	alls filled in bu Sidence IP				00000000	0+00
TP M SI CRC MS	2F				OTP M	SI CRC MSB[7:0]					
					Automatica	ally filled in by Sidence IP				00000000	0z00

Figure 19. OTP\_conf\_main\_reg spreadsheet example

2. Fill data in the OTP\_conf\_failsafe\_reg sheet.



#### Figure 20. OTP\_conf\_failsafe\_reg spreadsheet example

3. See the **OTP\_conf\_summary** sheet to review the complete configuration (main and fail-safe).

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#### Figure 21. OTP\_conf\_summary example

 Generate script in the OTP\_conf\_file\_generation sheet. Once the configuration is ready, the user can generate the script file. Go to OTP\_conf\_file\_generation, enter the path in the File repository, and then click Write\_OTP\_File\_GUI.



## 7.2 Working in OTP emulation mode

At startup, the device always uses the content from the mirror register. This content can come from OTP fuse or from configuration written directly in the mirror register. OTP

#### KITFS85AEEVM evaluation board

emulation means that the user can emulate the OTP writing in the mirror register. This allows trials before burning the OTP.

- 1. Configure the hardware. See Section 6 "Configuring the hardware for startup".
- 2. Launch the FlexGUI software.
- 3. Switch to Debug mode:
  - a. Place SW1 in TOP direction (VBAT switched On).
  - b. Close SW2 (WAKE1).

While in Debug mode, all regulators are turned Off.

- 4. Load the mirror registers to work in OTP emulation mode. See <u>Section 8.3 "Working</u> with the <u>Script editor"</u>.
- 5. Unplug jumper J24 1-2 to start the device with the mirror configuration setting.
  - a. If the mirror registers are filled (with a configuration using the Script editor), that configuration is used in the emulation session.
  - b. If the mirror registers are not filled (with a configuration using the Script editor), the currently-programmed OTP fuse configuration is used, if it exists.
  - c. Otherwise, the mirror registers are not filled and the OTP fuse is not burned, and the device will not start up.

As long as initialization phase is not closed by a first good WD\_Answer, the WD does not start and regulators do not stay alive. Also, as long as Debug mode is not exited by writing FS\_STATES:[DBG\_EXIT] bit to 1, the FS0B pin cannot be released.

 Use the FlexGUI software to evaluate the device configured. See <u>Section 8 "Using</u> <u>FlexGUI"</u>.

# 7.2.1 Example script: Closing initialization phase, disabling FCCU monitoring and releasing FS0B

The following script can be used to:

- Disable the WD (simple WD configuration is used here).
- Disable the FCCU monitoring.

On the hardware kit, the FCCU1 is pulled to GND and FCCU2 is pulled to VDDIO, which is detected as error phase by default. Disabling the FCCU by SPI/I2C avoids safety issue at startup.

- · Close the initialization phase.
- Exit the Debug mode.
- Release FS0B pin. This is valid only if WD is activated in OTP.
   Seven good consecutive WD answers are required to have the FLT\_ERR\_CNTR back to 0. This is one of the conditions to allow FS0B release.

Step	Register name	Value	Description
1	FS_WD_WINDOW	0x0200	WDW_WINDOWS[3:0] = 0x0 => Watchdog disabled
2	FS_NOT_WD_WINDOW	0xF50F	NOT of FS_WD_WINDOW
3	FS_I_SAFE_INPUTS	0x51C6	FCCU_CFG[1:0] = 0x0 => 0x1 => Monitoring by pair FCCU12_FLT_POL[0] = 1 => FCCU1 or 2 = 0 is a fault
4	FS_I_NOT_SAFE_INPUTS	0xAC18	NOT of FS_I_SAFE_INPUTS
5	FS_WD_ANSWER	0x5AB2	1st good WD answer (for simple WD selection in OTP) Close the initialization phase
6	FS_STATES	0x4000	DBG_EXIT[0]=1 => Exit Debug mode

#### Table 18. FS85 starting sequence example

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Step	Register name	Value	Description
7	FS_WD_ANSWER	0x5AB2	2nd good WD answer
8	FS_WD_ANSWER	0x5AB2	3rd good WD answer
9	FS_WD_ANSWER	0x5AB2	4th good WD answer
10	FS_WD_ANSWER	0x5AB2	5th good WD answer
11	FS_WD_ANSWER	0x5AB2	6th good WD answer
12	FS_WD_ANSWER	0x5AB2	7th good WD answer
13	FS_RELEASE_FS0B	0xB2A5	FS0B pin released (pulled to high level)
14	MFLAG2	0x40F1	Clear flags VSUPUV7; VPREUVL, VSUPUVL, WAKE1FLG
15	FS_OVUVREG_STATUS	0x4550	Clear UV status flags

This sequence can be sent using a script built with FlexGUI. See <u>Section 8.3.2 "Script</u> <u>sequence files</u>".

## 7.3 Programming the device with an OTP configuration

The device configuration can be changed three times (see <u>Section 4.2.1 "OTP and</u> <u>mirrors registers"</u>). The programming steps are exactly the same as the OTP emulation mode up to step 6.

Then, the user has to burn the part with FlexGUI. See <u>Section 8.4.8 "OTP programming"</u>. Follow the instructions on the screen to proceed.

## 8 Using FlexGUI

To follow the steps in this section, make sure that the board is connected using the appropriate hardware configuration (see <u>Section 7.2 "Working in OTP emulation mode"</u>).

Note: It is recommended to use the latest version of FlexGUI.

## 8.1 Starting the FlexGUI application

After FlexGUI is launched with the *flexgui-app.bat* file, the FlexGUI launcher displays available kits.

Communication bus, SPI or I2C can be selected at this level. It is also possible to switch from one to the other using the communication tab from the main panel (see <u>Section 8.2</u> "Establishing the connection between FlexGUI and the hardware").

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FlexGUI Laund	cher		_		$\times$
Select a kit, on	board device(s), tar	get MCU a	ind USB	interfa	ce.
-Kit and Device(	s)				
▼ FS85 KITs					
▼ FS85					
▼ ✓ FS	\$8530				
	B0				
$\checkmark$	C0				
A kit for FS85 a	nd FS84 evaluation.				
A kit for FS85 a	Ind FS84 evaluation. SPI or I <sup>2</sup> C bu	is selection			
A kit for FS85 a A kit for FS85 a Advanced Set Feature Set	nd FS84 evaluation. SPI or I <sup>2</sup> C bu ettings debug-spi	ıs selection	ist loaded	d tabs, et	tc.
A kit for FS85 a A kit for FS85 a Advanced Set Feature Set Target MCU	nd FS84 evaluation. SPI or I <sup>2</sup> C bu ettings debug-spi KL25Z (embedd	is selection	ist loaded	d tabs, et IW setup	tc.
A kit for FS85 a A kit for FS85 a Advanced Set Feature Set Target MCU USB Interface	nd FS84 evaluation. SPI or I <sup>2</sup> C bu ettings debug-spi KL25Z (embedd	Adju Adju Chec Chec	ist loaded ck your H ck used fi	d tabs, et IW setup irmware.	tc.
A kit for FS85 a A kit for FS85 a Advanced Se Feature Set Target MCU USB Interface Application	Ind FS84 evaluation. SPI or I <sup>2</sup> C bu ettings debug-spi KL25Z (embedd usb_cdc	Is selection	ist loaded ck your H ck used f	d tabs, et IW setup irmware.	tc. ).
A kit for FS85 a A kit for FS85 a Feature Set Target MCU USB Interface Application Password	nd FS84 evaluation. SPI or I <sup>2</sup> C bu debug-spi KL25Z (embedd usb_cdc Mode	Is selection	ist loader ck your H ck used fi Ele	d tabs, et IW setup irmware. evate	tc.
A kit for FS85 a A kit for FS85 a Feature Set Target MCU USB Interface Application Password Launch Privileg	Ind FS84 evaluation. SPI or I <sup>2</sup> C but debug-spi KL25Z (embedd usb_cdc Mode provide secret es BASIC	IS Selection	ist loader ck your H ck used f	d tabs, et IW setup irmware. evate	tc.
A kit for FS85 a A kit for FS85 a Feature Set Target MCU USB Interface Application Password Launch Privileg Use this cor	Ind FS84 evaluation. SPI or I <sup>2</sup> C but debug-spi KL25Z (embedd usb_cdc Mode provide secret es BASIC afiguration and do not a	Is selection Adju Chec Chec Chec Adju Chec	ist loaded ck your H ck used fi Ele	d tabs, et IW setup irmware. evate	tc.
A kit for FS85 a A kit for FS85 a Feature Set Target MCU USB Interface Application Password Launch Privileg Use this cor	Ind FS84 evaluation. SPI or I <sup>2</sup> C bu- debug-spi KL25Z (embedd usb_cdc Mode provide secret tes BASIC afiguration and do not a	Is selection Adju Chec Chec Chec Sk again	ist loaded ck your H ck used f Ele OK	d tabs, et IW setup irmware. evate Ca	tc. ),

Figure 23. Launcher panel - bus selection

When the configuration is selected, click **OK**.

## 8.2 Establishing the connection between FlexGUI and the hardware

The board must be connected to the USB before establishing a connection.

- Click **Search** to detect the COM port of the board.
- Click Start to enable the connection.

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COM9 - Search Stop														
VFO 👻 500 🜩 🖌 💾	FS85:FS8530:C0 Script editor													
er messages	1 Register map Clocks Regulators Me	asurem	ents Interrupt Flag	as INIT Safe	ty Diag Safety OTP, prog	TestMode:Sequence	r TestMode:Mirrors	Main TestMode:Mir	rors_FailSafe					
> FS85 [M_TM_STATUS1:0x1F] R: 0x020E > FS85 [FS_STATES:0x16] R: 0x4006	Tree View  Flat View Regist	🐼 🗋 Tree View & Flatz View Registers Per Page 8 🚭 Bit Buttors Per Line 8 😓 Soft By Address 🖉 Uniform Buttors 🖉 Show Bit Facabion												
> F\$85 [M_TM_STATUS1:0x1F] R: 0x022E	functional		Write Read	Copy Rese	s .									
> FS85 [FS_STATES:0x16] R: 0x4006	safety													
> FS85 [M_TM_STATUS1:0x1F] R: 0x022E	Write_INIT_Safety				W 0x0				RESERVED	ALSERVED	RESERVED	RESERVED	RESERVED	
FS85 [FS_STATES:0x16] R: 0x4006	\ Start		MELAG	0.00	A A	RESERVED	RESERVED	RESERVED	SPUMUCLK	SPUMUREQ	SPUMUCRC	ISC_M_CRC	IQC_M_REQ	1
> FS85 [M_1M_STATUSTORTF] RE000228	Communication		all the	0.00		COM_ERR	WU,6	VPRE_6	V800ST_6	VBUCK1_6	V8UCK2_6	VBUCK3,6	VLDO1_6	
> F585 IM TM STATUS1 0x1FI 8: 0x0226	\ \				K OxO	VLD02_G		RESERVED	SPILMUCLK	SPUNUREQ	SPUMUCRC	I2C_M_CRC	I2C_M_REQ	
F585 [FS_STATES:0x16] R: 0xA006														
> FS85 [M_TM_STATUS1.0x1F] R: 0x022E	Search				W 0x0		Gastrio				RESERVED	RESERVED	REPORT	
FS85 [FS_STATES:0x16] R: 0xA006	COM Port		M MODE	0x01			EXTLR NLDIS				W2DIS	W1DIS	GOTOSTBY	
> FS85 [M_TM_STATUS1:0x1F] R: 0x022E						RESERVED	ALSERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	PLL_LOCK_RT	1
> FS85 [FS_STATES:0x16] R: 0x04006					K 010	EXT_FIN_SEL_RT	RESERVED	MAIN_NORMAL	RESERVED	RESERVED	W2D/5	WIDIS	RESERVED	
> FS85 [M_TM_STATUS1:0x1F] R: 0x022E									Automat		NUCCON	100107	100307	
> FS85 [FS_STATES:0x16] R: 0x4006					W 0x0	1000000	1990	80031013	SUCCIDIS	6000203	8000303	1001013	100203	
<ul> <li>FS85 [M_1M_STATUSTORTF] R: 0x0226</li> <li>FF88 IFF CTATEROLISTIC ALONG</li> </ul>	User mode or Test		M_REG_CTRL1	0x02	0		VPEN	BOOSTEN	BUCKTEN	BUCKZEN	BUCKSEN	LDO1EN	LDOZEN	1
> FS85 [FS_STATES/0810] R: 084000	< Made Selection					VPRE_PO_DIS	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	
5 Pins	<ul> <li>Mode Selection</li> </ul>				K UKU	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	
ode						VETTERNI	VECTORIN	PROSTROVES	811711760/65	auroration as	BUT/2750/265	1001700/06	100200000	
vitch Mode: test-mode - Poll					W 0x0	(ostale)	(acceded			000000				
			M_REG_CTRL2	0x03	0	RESERVED	RESERVED	RESERVED	Vakterreli	Voltesats[0]	RESERVED	VPRESRHS[1]	VPRESRHS[0]	1
ting: SPI-routing *						V8STSR(1)	VESTSRIDI	BOOSTTSDCPG	BUCK1TSDCFG	BUCK2TSDCPG	BUCK3TSDCFG	LDO1TSDCFG	LDO2TSDCFG	1
SPI1	SPI or I2C Switch					RESERVED	RESERVED	RESERVED	VPRESRLS[1]	VPRESRL5[0]	RESERVED	VPRESRHS[1]	VPRESRHS(0)	
us: SPI														
equency (kHz): 5000					W Oxe				110000	110000	44.00079	448.0777		
Main Status			M_AMUX	0x04	0			~10	********	Amodal	Annual I	www.ultil	www.codoj	1
					R Ox0				RESERVED	RESERVED		RESERVED	RESERVED	
Extended Status						RESERVED	ALSERVED	RATIO	AMUX[4]	AML0(3)	AM/U00[2]	AMUR[1]	AMUX[0]	1
.DO2_G: No event						MOD_CON#	FOUT_MUX_SEL[3]	FOUT_MUX_SEL[2]	FOUT_MUX_SEL[1]	FOUT_MUX_SEL[0]	FOUT_PHASE[2]	FOUT_PHASE[1]	FOUT_PHASE[0]	
4_M_CLK: No error					W 0x0	FOUT OF SE	EVT ON SEL	EN DV	MOD EV	OK DINER	OV TUNED	CIX DINESS	OKTINES	
L_M_REQ: No error			M_CLOCK	0x05	0	- Construction	and here		and get	encionets)	erectionite)	enclosed ()	enc.unity)	
I_M_CRC: No error	Communication				R 0x0	MOD_CON#	HOUT, MUX, SEL[3]	HOUT, MUX, SEL[2]	POUT_MUX_SEL[1]	POUT_MUX_SEL[0]	POUT, PHASE[2]	POUT,PHASE[1]	POUT_PHASE[0]	
_M_CRC: No error	< Status					POUT_CLK_SEL	RESERVED	FIN_DIV	MOD_EN	CUK,TUNE(3)	CUC,TUNE[2]	CDC_TUNE[1]	CUK_TUNE[0]	1
_M_REQ: No error								< 1 2	3					
								1/3		Anatientien			H. Thu C & 02 16 01	ma

#### Figure 24. Main panel

<u>Figure 24</u> shows the mode selection. At first launch, the FlexGUI starts in User mode. The user can then decide to switch to Test mode using the Switch mode drop-down list followed by clicking **Apply**.

The **GUI-Device Status** field checks the connection from MCU to the device. The **ONLINE** status indicates a good connection, while **ERROR** status indicates an issue (e.g. V<sub>SUP</sub> is not provided to the device).

The SPI/I2C communication bus can be changed at any time using the drop-down list. This change is managed by the onboard MCU to communicate with the desired bus.

It is also possible to change the clock frequency using this panel.

Note that in the case of I2C, most of the time, the default address used by the device are 0x20 for main and 0x21 for the fail-safe.

The I2C address is managed differently in Debug and Normal mode

- Debug mode :
  - I2C address when debug mode pin is set to 5.0 V are 0x20 for main and 0x21 for failsafe.
  - The user can change this address in the mirror register. The new address is taken into account only after debug pin is released to 0 V.
- Normal mode:
  - The address is burned in the OTP.

The user can read in which mode the device is operating. It is also possible to switch from user mode to test mode (and vice-versa).

The current operating mode is refreshed periodically by default at FlexGUI startup. This automatic refresh can be disabled by disabling Poll button as shown in <u>Figure 25</u>.

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ſ	FS85			
	Mode			
	Switch Mode:	user-mode	•	Apply
	Current Mode:	user-mode		Poll
				aaa-032771
Figure 25. Disal	oling device mode p	olling		

To move from one mode to the other, select the mode with switch mode drop-down button and click **Apply** to validate. At this time, the current mode is updated at the condition that Poll button is enabled.

## 8.3 Working with the Script editor

The register and OTP emulation can be configured with the script editor. This is particularly useful to try various OTP configurations in Emulation mode.

IFO 🔹 500 🕂 🍯 📕 💾	FS85 Scrip	t editor					
r mesages 🔹 🔮	Device:	F585 -		Commands:	Results:		
ESES JES_MIRRORCMURATI/JW: 0x0118	Alias	No values	٠	//Device configuration: FS8530	//Device configuration: FS8530		
SES IFS MIREORCMD 0x171 W 0x0119			_	//Sample marking: PC33FS8530A0ES	//Sample marking: PC33FS8530A0ES		
585 [FS_OTPCMD.0x18] W: 0x0125	<ul> <li>Digital pins</li> </ul>			//autoc: NAP //Customer: NDP	//Author: NXP		
85 [FS_OTPCMD:0x18] W: 0x0124	<ul> <li>Analog pins</li> </ul>		_	//Date: 11/8/2018	//Customer: NXP		
85 IFS TM STATUS1.0x2A1 R: 0xA0C0	<ul> <li>Registers</li> </ul>			//Time: 10:12:14 AM //Generated from ISBS OTD Mannion File registron: Rev 1.4	//Date: 11/8/2018		
85 [M. TM. STATUS1:0x1F] R: 0x0022	▶ Mode			//Emulate/Program: Emulate	//Time: 10:12:14 AM		
15 [FS_STATES:0x16] R: 0x4001	<ul> <li>Generator</li> </ul>			//GUL_rev: > 0.6	//Generated from FS85_OTP_Mapping file revisi	on: Rev 1.4	
5 [M_TM_STATUS1:0x1F] R: 0x0022				SET_MODE/ENTRY SET_MODE/ES85test-mode	//Emulate/Program: Emulate		
35 [FS_STATES:0x16] R: 0xA001	0	Command		//BEGIN MAIN	//GUI rev: > 0.6		
5 [M_TM_STATUS1:0x1F] R: 0x0022				//Verify Main Test Mode Entry (expect 0x0022) GET_REG_ESSS_M_TextMode_M_TM_STATUS1	//TEST_MODE_ENTRY		
15 [FS_STATES:0x16] R: 0xA001	5	cript Editor		//CONFIGURE OTP MIRROR REGISTERS Script Text Editor	OK: set mode = test-mode	Script Results	
5 [M_TM_STATUS1:0x1F] R: 0x0022				SET_REG:FS85:M_OTP:M_MIRRORDATA.0x000F	//BEGIN MAIN		
5 [FS_STATES:0x16] R: 0xA001				SEL_REG:S85:M_OTP:M_MIRRORCMD:00114 SET_REG:FS85:M_OTP:M_MIRRORDATA.0x0007	//Verify Main Test Mode Entry (expect 0x0022)		
5 [M_TM_STATUS1:0x1F] R: 0x0022	Send	and Receive	d	SET_REG/FS85:M_OTP:M_MIRRORCMD:0x0115	OK mad man M TM STATUS1 = 0x0022		
5 [FS_STATES:0x16] R: 0xA001	Com	mands		SET_REG/FS85/M_OTP/M_MIRRORDATA.0x00EF	//CONFIGURE OTP MIRROR REGISTERS		
5 [M_TM_STATUS1:0x1F] R: 0x0022	00111	nanao		SET_REG:FS85:M_OTP:M_MIRRORDATA.0x000D	MD.60116 // CONIKURA (17) MICRA NULLA (1		
5 [FS_STATES:0x16] R: 0xA001				SET_REG/FS85/M_OTP:M_MIRRORCMD:0x0117			
ins				SET_REG/FS85/M_OTP/M_MIRRORDATA/0x008C SET_REG/FS85/M_OTP/M_MIRRORCMD/0x0118			
			S	SET_REG:FS85:M_OTP.M_MIRRORDATA:0x0007	OK write reg. M_MIRODRUATA II 0007		
			SET_REG/585-M_OTP.M_MIRRORCMD.0x0119	OK: write reg. M_MIRROROMD = 0x0115			
Mode: test-mode *				SET_REGIFS85IM_OTPIM_MIRRORCMD.0011A	OK: write reg. M_MIRRORDATA = 0xet		
Mode: test-mode				SET_REG:FS85:M_OTP:M_MIRRORDATA:0x0006	Of write reg. M MIRRORDATA = 0x01		
Splanuting w				SET_REG/FS85/M_OTP/M_MIRRORCMD:0x0118 SET_REG/FS85/M_OTP/M_MIRRORCMD:0x0118	OK: write reg. M_MIRRORDATA = 0x0d		
unround				SET_REG:FS85:M_OTP:M_MIRRORCMD.0x011C	OK write reg. M_MRAORORDATA = 0.01		
				SET_REG/FS85-M_OTP-M_MIRRORDATA.0x001C	OK write reg. M_MIRNORDATA II GIOC		
SIPI				SEL_REG/S85/M_OTP/M_MIRROROMD/MOTIO	OK: WHE REG. M_MINIORCMD II GIDTIS		
ty [kHz]: 5000				SET_REG/FS85/M_OTP.M_MIRRORCMD.0x011E	OK: write reg. M_MIRIORDATA = 0x07		
Status				SET_REG:FS85:M_OTP.M_MIRRORDATA.0x0093	OK: write reg. M_MIRIORCMD = 0x0119		
R: No failure				SET_REG/FS85/M_OTP/M_MIRRORDATA.0x0076	OR: write reg. M_MIRIORDATA = 0x64		
Event occurred				SET_REG:FS85:M_OTP:M_MIRRORCMD:0x0120	OR: write reg. M_MIRIORCMD = 0x011a		
Event occurred				SET_REG/S85:M_OTP:M_MIRRORCMD:0x00121	OR: write reg. M_MIRIORDATA = 0x06		
G: Event occurred				SET_REG:FS85:M_OTP.M_MIRRORDATA;0x0023	OR: write reg. M_MIRIORCMD = 0x0116		
C No wast				SET_REG/FS85/M_OTP.M_MIRRORCMD.0x0122	OK: write reg. M_MIRRORDATA = 0x88		
To: No event				SET_REG/S85/M_OTP/M_MIRRORCMD/0x0123	OK: write reg. M_MIRRORCMD = 0x011c		
2_G: No event				SET REGISSES M OTPM MIRRORDATA0x0004	OK: write reg. M_MIRRORDATA = 0x1c		
3_G: No event				💽 ∞ 💾 들 🚽 👩 Script Execution and Management	🔡 🛅 🥑 Results mana	agement	
I_G: No event	el .						

### Figure 26. Script Editor

The main subareas of this panel are:

- Send and receive command: displays a summary of commands sent and received from the device
- Command script editor: builds commands to be sent to the device
- Script text editor: sends a sequence of register configurations from a text file or from command edited directly in this area
- Script results: displays result status of each command sent to the device

#### 8.3.1 Script text editor

Using Script editor, you can execute any command either directly or from a file. It is also possible to save and modify a script. Using the brush symbol, it is possible to clean windows if needed.

All commands have to follow a specific syntax. The Help menu describes commands available in the script editor and their syntax.

This help page describes commands available in the script editor and their format.

#### List of commands

- SET\_REG: sets value of a selected register.
- READ\_REG: reads value of a selected register.
- SET\_DPIN: sets value of a selected digital pin.
- GET\_DPIN: gets value of a selected digital pin.
- GET\_APIN: gets value of a selected analog pin. Returned value is in mV.
- PAUSE: shows a dialog with user defined message. The script is paused until the user cofirms the dialog.
- EXIT: stops execution of the script.
- SET\_MODE: sets device mode. List of modes depends on a device.

## **Command format**

The following table describes command parameters. All paramaters are mandatory.

	lst parameter	2nd parameter	3rd parameter	4th parameter	5th parameter
SET_REG	Device	Reg. set	Reg. name / Reg. address	Reg. value	-
GET_REG	Device	Reg. set	Reg. name / Reg. address	-	-
SET_DPIN	Device	Pin name	Dig. pin value	-	-
GET_DPIN	Device	Pin name	-	-	-
GET_APIN	Device	Pin name	-	-	-
PAUSE	Message	-	-	-	-
EXIT	-	-	-	-	-

Description of command parameters mentioned in the table above:

- Device: device name (alias used in application).
- Reg. set: register set name. Register sets allows to associate registers which have similar function.
- Reg. name: register name as defined in datasheet.
- Reg. address: register address in decimal or hexadecimal (with 0x prefix) format.
- Reg. value: register value in decimal or hexadecimal (with 0x prefix) format.
- Pin name: name of digital or analog pin as defined in device datasheet.
- Dig. pin value: value of digital pin. Allowed strings are 'low' and 'high'.
- · Message: a message to be displayed in a dialog. It cannot contain ':' character, which is used as delimiter of
- parameters.
- Mode: name of a device mode.

Figure 27 shows an example to build a command from the panel.

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	FS85 Script editor					
	Device: FS	\$85	•	Commands:		
	<ul> <li>Digital pins</li> </ul>			SET_REG:FS85:functiona	al:M_REG_CTRL1:0x0800	
	Analog pins			Comma	l Ind Built	
	<ul> <li>Registers</li> </ul>					
	Operation:	Write reg.	•			
	Reg. set:	functional	-			
	Reg. name/address:	M_REG_CTRL1	-			
	Reg. value:	0x0800				
	Build	 Command			aaa-032336	
Figure 27. B	uild a command	1				

The value 0x0800 is sent to the register M\_REG\_CTRL1 (BUCK2DIS). The user can then send it to the device by clicking the arrow (see Figure 28).

	Send Script aaa-032337	
Figure 28. Send script	:	
	Commands:	
	// This command will disable // Regulator BUCK2 SET_REG:FS85:functional:M_REG_CTRL1:0x0800	
Figure 29. Correct for	mat	
	Commands:	
	// This command will disable Regulator BUCK2 SET_REG:FS85:functional:M_REG_CTRL1:0x0800	
Figure 30. Wrong forn	nat ("//" missing in second line)	

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## 8.3.2 Script sequence files

The Script editor allows the user to save script sequence files. A script sequence file is text file that contains a set of commands sent to the device in the order they are written, as shown in the following example.

```
// FS85_Release_FS0b
SET_REG:FS85:safety:FS_WD_WINDOW:0x0200
SET_REG:FS85:safety:FS_NOT_WD_WINDOW:0xF50F
SET_REG:FS85:Write_INIT_Safety:FS_I_SAFE_INPUTS:0x51C6
SET_REG:FS85:write_INIT_Safety:FS_I_NOT_SAFE_INPUTS:AC18
SET_REG:FS85:safety:FS_WD_ANSWER:0x5AB2
```

Note: Comments can be added with a // prefix.

## 8.4 Understanding the FS85 workspace

The FS85 workspace consists of several tabs, each dedicated to a specific aspect of device functionality or configuration.

- · Register map
- Clocks
- Regulators
- Measurements
- Interrupt flags
- · INIT safety
- Diag safety
- OTP programming
- TestMode:Sequencer
- TestMode:Mirrors\_Main and TestMode:Mirrors\_Failsafe

#### 8.4.1 Register map

All SPI/I2C registers can be accessed in write and read mode using this tab.

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# • **Register map**: allows access to functional register, safety register and write init register which are accessible only during initialization phase

- Read: allows you to read any register either individually or by bank
- Write: allows you to write any register either individually or by bank
- Register expansion: displays the value of each device parameter

## 8.4.2 Clocks



This tab allows:

OTP:

• Read current OTP configuration (write operation is not possible). To display the accurate data, the device needs to operate in Test mode.

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SPI/I2C:

- · Configure the device to work with FIN input
- Select the signal to apply on FOUT pin
- Play with manual frequencies and spread spectrum

## 8.4.3 Regulators

The regulator has two main areas:

- · Low voltage (LV) regulators configuration
- VPRE compensation network calculation

Each regulator can either be enabled or disabled by SPI/I2C. The thermal shutdown behavior can be configured to either shutdown the regulator, or shutdown the regulator and transition to deep fail-safe. The write button applies to the entire table. The VPRE compensation network calculator helps to define the value for VPRE external compensation network.

Low Voltage Regulators						VPRE compensation network calculation
	LV Buck1			LV Buck2		VPRE [V]
State in normal mode	Disable Regulates Shutdown	-	State in normal mode	Disable Regulator Shutdown	•	VPRE ILIM [mV]
senavior in case of 150	Regulator_shutdown	•	behavior in case of 150	Regulator_shutdown		Rshunt [mOhm]
	LV Buck3			LDO1		Cout [uF]
State in normal mode	Disable	-	State in normal mode	Disable	-	Lvpre [uH]
Behavior in case of TSD	Regulator_Shutdown	•	Behavior in case of TSD	Regulator_Shutdown	•	Rcomp [KOhm]         N/A           Ccomp [nF]         N/A           Chf [pF]         N/A
	LDO2			VBOOST		Current limit [A] N/A
State in normal mode Behavior in case of TSD	Disable Regulator_Shutdown	•	State in normal mode Behavior in case of TSD	Disable Regulator_Shutdown	* *	alope compensation (mir) us nove
		Wr	ite			Calculate
						aaa-0-

#### 8.4.4 Measurements

This tab enables two features:

- Read any of the AMUX signals over time
- · Display regulator voltage summary

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## 8.4.5 Interrupt flags

This tab allows you to set or clear flags. It is also possible to mask the interruption.

	Over/under-	voltage			Over-	temperatu	ire	
	Status   (	Clear	Mask		Statu	us Clear	r	Mask
VSUP UVH		$\checkmark$	INT_not_masked	LDO1 shutdown				INT_not_maske
VSUP UVL		$\checkmark$	INT_not_masked	LDO2 shutdown				INT_not_maske
VSUP UV7		$\checkmark$	INT_not_masked	BUCK1 shutdown				INT_not_maske
VPRE UVH		$\checkmark$	INT_not_masked	BUCK2 shutdown				INT_not_maske
VPRE UVL		$\checkmark$	INT_not_masked	BUCK3 shutdown				INT_not_maske
VPRE FB_OV			INT_not_masked	VBOOST shutdown				INT_not_maske
VBOS UVH		$\checkmark$	INT_not_masked	BOS				INT_not_maske
VBOOST UVH	-	$\checkmark$	INT_not_masked		Write	Read	Poll	
VBOOST OV			INT_not_masked					
	Over-cur Status	r <mark>rent</mark> Clear	Mask		Mise State	c <mark>ellaneous</mark> 1s Clear	; r	Mask
LDO1	Over-cur Status	rrent Clear	Mask INT not masked	LDQ1 ST	Mise State	cellaneous us Clear	i r	Mask
LDO1 LDO2	Over-cur Status (	rrent Clear	Mask INT_not_masked INT_not_masked	LDO1 ST LDO2 ST	Mise State	cellaneous us Clear	7	Mask
LDO1 LDO2 BUCK1	Over-cur Status (	rrent Clear	Mask INT_not_masked INT_not_masked INT_not_masked	LDO1 ST LDO2 ST BUCK1 ST	Mis Stati	cellaneous us Clear	2	Mask
LDO1 LDO2 BUCK1 BUCK2	Over-cur Status (	rrent Clear	Mask INT_not_masked INT_not_masked INT_not_masked INT_not_masked	LDO1 ST LDO2 ST BUCK1 ST BUCK2 ST	Mise State	cellaneous us Clear	- -	Mask
LDO1 LDO2 BUCK1 BUCK2 BUCK3	Over-cur   Status   (	Clear	Mask INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked	LDO1 ST LDO2 ST BUCK1 ST BUCK2 ST BUCK3 ST	Mise State	cellaneous us Clear	5	Mask
LDO1 LDO2 BUCK1 BUCK2 BUCK3 VBOOST	Over-cur   Status   (	rrent Clear	Mask INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked	LDO1 ST LDO2 ST BUCK1 ST BUCK2 ST BUCK3 ST VBOOST ST	Miso Statu	cellaneous us Clear		Mask
LDO1 LDO2 BUCK1 BUCK2 BUCK3 VBOOST VPRE	Over-cur Status (	Clear	Mask INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked	LDO1 ST LDO2 ST BUCK1 ST BUCK2 ST BUCK3 ST VBOOST ST WK1 FLG	Miso Statu	cellaneous us Clear		Mask INT_not_maske
LDO1 LDO2 BUCK1 BUCK2 BUCK3 VBOOST VPRE	Over-cur Status (	rrent Clear	Mask INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked	LDO1 ST LDO2 ST BUCK1 ST BUCK2 ST BUCK3 ST VBOOST ST WK1 FLG WK2 FLG	Misa Statu	cellaneous Is Clear		Mask INT_not_maske INT_not_maske
LDO1 LDO2 BUCK1 BUCK2 BUCK3 VBOOST VPRE	Over-cur Status ( Write Read	d Pol	Mask INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked	LDO1 ST LDO2 ST BUCK1 ST BUCK2 ST BUCK3 ST VBOOST ST WK1 FLG WK2 FLG WK1 RT	Miss State	cellaneous ıs Clean		Mask INT_not_maske INT_not_maske
LDO1 LDO2 BUCK1 BUCK2 BUCK3 VBOOST VPRE	Over-cur Status ( Write Read	rrent Clear	Mask INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked	LDO1 ST LDO2 ST BUCK1 ST BUCK2 ST BUCK3 ST VBOOST ST WK1 FLG WK2 FLG WK1 RT WK2 RT	Miss State	cellaneous us Clean		Mask INT_not_maske INT_not_maske
LDO1 LDO2 BUCK1 BUCK2 BUCK3 VBOOST VPRE	Over-cur Status (	rrent Clear	Mask INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked	LDO1 ST LDO2 ST BUCK1 ST BUCK2 ST BUCK3 ST VBOOST ST WK1 FLG WK2 FLG WK1 RT WK2 RT	Miss State	Cellaneous us Clear	Poll	Mask INT_not_maske INT_not_maske

## 8.4.6 INIT safety

This tab allows you to manage all registers that can be configured to close the initialization phase. Note that the initialization phase is closed by the first good watchdog refresh before 256 ms timeout.

	Fault impact						
Fault source	Settings	FSOB RSTB		Error counters limit		OV/UV Safe React	ion 1
COREMON_OV	No_effect 👻		WD_ERR_LIMIT	6 -	6	VCore ABIST2	No_ABIST
DDIO_OV	No_effect 👻		WD_RFR_LIMIT	6 -	6	VDDIO ABIST2	No_ABIST
MON1_OV	No_effect 👻		FLT_ERR_CNT_LIMIT	6 👻	6	VMon2 ABIST2	No_ABIST
MON2_OV	No_effect 👻					VMon3 ABIST2	No_ABIST
MON3_OV	No_effect 👻					VMon4 ABIST2	No_ABIST
MON4_OV	No_effect 👻						
COREMON_UV	FSOB 👻			Safe Inputs		Miscellaneous	3
DDIO_UV	FSOB 👻		FCCU pin config	FCCU1_FCCU2_pair •	FCCU1_FCCU2_pair	RSTB pulse duration 10ms	▼ 10ms
MON1_UV	FSOB 👻		FCCU12 polarity		FCCU1_L_FCCU2_H	Assert RSTB on FS0B short	RESET_asserted
MON2_UV	FSOB 👻	•	FCCU2 polarity		FCCU2_L	Disable 8S timer	Counter_enables
MON3_UV	FSOB 👻		FCCU1 polarity impact	$\checkmark$	FSOB_RSTB		
MON4_UV	FSOB 👻		ERRMON polarity		Negative_edge		
CCU12	FSOB_RSTB -		ERRMON timing config	8ms •	oms		
CCU1	FSOB_RSTB -						
CCU2	FSOB_RSTB -			Static Voltage Scaling			
RRMON	FSOB_RSTB -		Static voltage scaling	0mV 👻	0mV		
VD_FS_IMPACT	FSOB_RSTB -						
LT_ERR_IMPACT	FSOB_RSTB +						
npact							
o impact							
	Write Read				Write	ed.	
	White				write		
							aaa-0323

## 8.4.7 Diag safety

The watchdog type configured in the OTP has to be manually selected in the dropdown list to play with the watchdog features. If the user is not aware about the type of watchdog configured in the OTP, it can be found in TestMode:Mirrors\_Failsafe and Miscellaneous tabs.

## KITFS85AEEVM evaluation board

Register map Clocks Regulators Measurements Interrup	pt Flags INIT Safety Diag Safety OTP_prog TestMode:Sequence	er TestMode:Mirrors_Main TestMode:Mirrors_FailSafe
Safe IO	Diag Safety	INTR Mask
Report PGCOD change         N/V           Report PGCOD event         N/V           Report PGCOD sense         N/V           External reset         N/V           RSTB driver         N/V           RSTB sense         N/V           RSTB vent         N/V           RSTB driver         N/V           RSTB drag         N/V           RSTB request         FS08 driver           FS08 drag         N/V           FS08 fragest         Goto INIT fail-sete	FCCU12 error         N/V           FCCU12 error         N/V           FCCU2 error         N/V           FCCU2 error         N/V           FRRMON input status         N/V           ERRMON input status         N/V           WD refresh status         N/V           WD terring         N/V           SPI CLK status         N/V           SPI CLK status         N/V           I2C CRC status         N/V           I2C access status         N/V	VMON4 OV/UV int. enable     N/V       VMON3 OV/UV int. enable     N/V       VMON2 OV/UV int. enable     N/V       VMON1 OV/UV int. enable     N/V       VDDIO OV/UV int. enable     N/V       VCDREMON OV/UV int. enable     N/V       WD refresh int. enable     N/V       FRRMON int. enable     N/V       FCCU2 int. enable     N/V       FCCU1 int. enable     N/V
Write Read	Write Read	Write Read
Watchdog management	OV/UV status	Flags and Status
Watchdog Type     Simple_WD       Good watchdog refresh     WD ANSWER Good       Bad watchdog refresh     WD ANSWER Bad       FS08 release     FSRELEASE_FS08 Command       FS08 release script     FS08 release script       WD_RR_CNT     FS08 release script       WD_RR_CNT     FS08 release script       WD_RR_CNT     Disable IN/V       WDW_DC (Duty Cycle)     31.25 IN/V       WDW_RECO VERY     Disable IN/V       Write     Read       Send right FS_RELEASE_FS08	VCOREMON OV         N/V           VCOREMON UV         N/V           VDDIO OV         N/V           VDDIO OV         N/V           VDDIO UV         N/V           VMONA OV         N/V           VMON3 UV         N/V           VMON2 OV         N/V           VMON2 UV         N/V           VMON1 UV         N/V           FS DIG REF OV         N/V           Write         Read           Ecript to release FSOb pin when         rom power-up           register value         V	Communication error     N/V       WD refresh error     N/V       IO error     N/V       Voltage monitoring error     N/V       ABIST1 status     N/V       ABIST2 status     N/V       LBIST_CK status     N/V       Leave debug mode     N/V       Debug mode     N/V       OTP bit corruption     N/V       INIT register corruption     N/V       Write     Read
Select the current watchdog OTP config before to use the watchdog manageme Figure 37. Diag safety	guration nt window	aaa-032345

The FS\_Release\_FS0B command calculates and sends the right secure16-bit word to release FS0B.

A simplified way to release FS0B after power up is to, first, select the right type of watchdog configured in the OTP, then, hit FS0B Release script button. This sends the right sequence to close the initialization sequence, sets the error counter back to 0, then releases FS0B.

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## 8.4.8 **OTP** programming

This tab allows you to burn the OTP using a script generated by the excel file OTP configuration (see <u>Section 7.1 "Generating the OTP configuration file "</u>).



## Figure 38. OTP burning

To set up the hardware before OTP burning, see <u>Section 7.3 "Programming the device</u> with an OTP configuration".

See Figure 38 and follow the steps:

- Browse and load the script file you want to burn. The program button is then available.
- Click Program.

FlexGUI pops up to turn the 8.0 V On, and then turns Off. Note that the blue LED on the board indicates that an 8.0 V voltage is available on the Debug pin. This voltage is used only during the burning process, and should not be applied in any other configuration. At the end of the first OTP programming, the MTP index = 1, WP, BE and CRC flags are green.

The Sector Flags area provides status <u>Table 19</u> provides the state of main flags after a read. This helps to determine how many times the part was burned.

OTP burning step	BE	WP	CRC	MTP Index
OTP not burn Mirrors Empty	Red	Red	Red	1
OTP not Burn Mirrors Filled	Red	Red	Green	1
1	Green	Green	Green	1
2	Green	Green	Green	2
3	Green	Green	Green	3

#### Table 19. OTP burning flag status

Example shown in Figure 38 corresponds to the OTP burning step 2 from Table 19.

To check if a valid OTP configuration is already burned, switch  $V_{BAT}$  Off, then On, and start the device. The device starts with the OTP configuration.

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## 8.4.9 TestMode:Sequencer

The sequencer allows you to display the slot configuration for the device. To be able to access this tab, the device has to be in Test mode. The configuration is read from mirror register. It is possible to modify it and update the mirror register.

As an example, the slot sequence is filled at start up with the content of OTP fuses. Then the user can decide to modify any of the configurations coming from the OTP fuse. Note that all these actions are done with Debug pin at 5.0 V and in test mode.



Use the drop-down button (see <u>Figure 40</u>) to select the appropriate slot. The selection configuration can be sent to the device by clicking Write button. The current status can be read by using Read button.



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## 8.4.10 TestMode:Mirrors\_Main and TestMode:Mirrors\_Failsafe

The TestModeMirrors\_Main and TestModeMirrors\_FailSafe tabs allow access to the OTP main mirrors and fail-safe registers. These tabs are available in Test mode.

	VPRE			BOOST			LDOs	
VPRE mode	Force PWM 👻	Force PWM	Output voltage	1	<b>~</b> 1	VLDO2 current limitation	400mA ~	400mA
Output voltage	17 -	17	BOOST enable	Disabled	<ul> <li>Disabled</li> </ul>	VLDO2 output voltage	1.2V -	1.2V
Slope compensation	170mV/us -	170mV/us	BOOST minimum ON time	60ns		LDO2 sequencing slot	Slot2 -	Slot2
Current limitation threshold	50mV ~	50mV	VBOOST slope compensation	17	▼ 17	Regulator behavior in case o	LDO2 shutdown + *	LDO2 shutdown +.
Low Side slew rate control	130mA ~	130mA	Compensation Network Resistor Rco.	750Kohms	<ul> <li>750Kohms</li> </ul>	VLDO1 current limitation	400mA ~	400mA
High Side slew rate control	260mA -	260mA	Compensation Network Capacitor C	. 1	<b>*</b> 1	VLDO1 output voltage	1.2V ~	1.2V
VPRE phase (delay) selection	Delay2 👻	Delay2	VBOOST current limitation	0	<b>~</b> 0	LDO1 sequencing slot	Slot1 -	Slot1
Delay to turn OFF VPRE at device power down	32ms 👻	32ms	VBOOST Low Side slew rate control	1	<b>*</b> 1	Regulator behavior in case o	LDO1 shutdown 👻	LDO1 shutdown
VPRE clock selection	CLK_DIV1 -	CLK_DIV1	BOOST phase (delay) selection	Delay1	<ul> <li>Delay1</li> </ul>			
			BOOST clock selection	CLK_DIV2	<ul> <li>CLK_DIV2</li> </ul>			
			Regulator behavior in case of TSD	BOOST shutdown	<ul> <li>BOOST shut</li> </ul>			
Writ	e Read		٧	Vrite Read			Write Read	
	BUCK1			BUCK2			BUCK3	
VBUCK1 output voltage	17 💌	17	VBUCK2 output voltage	17 -	17	VBUCK3 output voltage	2.8V	▼ 2.8V
BUCK1 inductor selection	1.5uH *	1.5uH	BUCK2 inductor selection.	1uH -	1uH	BUCK3 enable	Disabled	<ul> <li>Disabled</li> </ul>
VBUCK1 current limitation	0 -	0	BUCK2 enable	Enabled -	Enabled	BUCK3 inductor selection	1uH	▼ 1uH
VBUCK1 & VBUCK2 multiphase operation	Enabled -	Enabled	VBUCK2 current limitation	0 -	0	VBUCK3 current limitation	2.6A	▼ 2.6A
BUCK1 Compensation Network	65GM -	65GM	BUCK2 compensation network	0 -	0	BUCK3 compensation resistor	Default	▼ Default
BUCK1 sequencing slot	Slot1 -	Slot1	BUCK2 sequencing slot	Slot2 -	Slot2	BUCK3 gain control	1	▼ 1
BUCK1 phase (delay) selection	Delay2 -	Delay2	BUCK2 phase (delay) selection	Delay1 ~	Delay1	BUCK3 sequencing slot	Slot1	✓ Slot1
BUCK1 clock selection	CLK_DIV1 -	CLK_DIV1	BUCK2 clock selection	CLK_DIV1 -	CLK_DIV1	BUCK3 phase (delay) selection	Delay2	▼ Delay2
Regulator behavior in case of TSD	BUCK1 shutdown +	BUCK1 shutdown +	Regulator behavior in case of TSD	BUCK2 shutdown -	BUCK2 shutdown	BUCK3 clock selection	CLK_DIV1	· CLK_DIV1
BUCK1 and BUCK2 Soft start/stop configura	7.81mV/us *	7.81mV/us				Regulator behavior in case of	BUCK3 shutdown	<ul> <li>BUCK3 shutd.</li> </ul>
						Soft start/stop configurability	3.47mV/us	
Weit	e Read		v	Vrite Read			Write Read	
Pi Lanabla	Dirabled w Dirabled		Deep Fail-rafe infinite auto-th-	SM Dirabled	* Dirabled	VSUR Linder Voltage Thread of	Configuration 6.31/	× 6.74
PLL enable	Disabled + Disabled		Deep rail-safe infinite autoretry enab	Disabled	Disabled	VSOP Under Voltage Threshold	Configuration 0.2V	+ 0.2V
Divides 2 setting	Divide10 = Divide10		Suppreside autoretry criable	2.6595	2.000	regulator assigned to VDDIO (C	VPRE	· VPRE
Divider 2 setting	Divide to - Divide to		Synchronization with 1x PS85 of 1x P	FOC CAPSOD	· Excelled			
			Device I2C address	D1	<ul> <li>Enabled</li> <li>D1</li> </ul>			
Writ	Read		V	Vrite Read			Write Read	
<b>F</b>			•					aaa-03235
Figure 41. Test	tMode: Mi	rrors_Ma	ain					

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## **NXP Semiconductors**

# UM11193

## KITFS85AEEVM evaluation board

Register map Clocks Regulators Measurements Inte	errupt Flags INIT Safety Diag Safety OTP_prog T	estMode:Sequencer TestMode:Mirrors_Ma	in TestMode:Mirrors_FailSafe	
VMON1		VMON2	VMON3	
Overvoltage threshold [%] 112 -	112 Overvoltage threshold [%]	112 - 112	Overvoltage threshold [%] 112	• 112
Overvoltage Filtering Timing [us] 45 🔹	45 Overvoltage Filtering Timing [us]	45 👻 45	Overvoltage Filtering Timing [us] 45	≠ 45
Undervoltage threshold [%] 88 🔹	88 Undervoltage threshold [%]	88 - 88	Undervoltage threshold [%] 88	- 88
Undervoltage Filtering Timing [us] 25 🔹	25 Undervoltage Filtering Timing [u	s] 25 👻 25	Undervoltage Filtering Timing [us] 25	- 25
Assignment to PGOOD	Not_Assigned Assignment to PGOOD	Not_Assigned	Assignment to PGOOD	Not_Assigned
Assignment to ABIST1	Not_Assigned Assignment to ABIST1	Not_Assigned	Assignment to ABIST1	Not_Assigned
Monitoring	Disabled Monitoring	Disabled	Monitoring	Disabled
write Read	writ	te Read	write	ead
VMON4		VDDIO	VCORE	
Overvoltage threshold [%] 112 •	112 Overvoltage threshold [%]	112 • 112	Overvoltage threshold (BUCK1) [%] 112	▼ 112
Overvoltage Filtering Timing [us] 45 🔹	45 Overvoltage Filtering Timing [us]	45 🕶 45	Overvoltage Filtering Timing [us] 45	◄ 45
Undervoltage threshold [%] 88 👻	88 Undervoltage threshold [%]	88 🕶 88	Undervoltage threshold [%] 88	- 88
Undervoltage Filtering Timing [us] 25 🔹	25 Undervoltage Filtering Timing [ut	s] 25 💌 25	Undervoltage Filtering Timing [us] 25	- 25
Assignment to PGOOD	Not_Assigned Assignment to PGOOD	Not_Assigned	Assignment to PGOOD	Not_Assigned
Assignment to ABIST1	Not_Assigned Assignment to ABIST1	Not_Assigned	Assignment to ABIST1	Not_Assigned
Monitoring	Disabled Voltage selection	3.3V = 3.3V	Monitoring voltage (VBUCK1) 1.25	iV = 1.25V
write Read	writ	Read	write	ead
	Miscellaneous			
SVS max value allowed NoSVS - NoSVS	RSTB assignment to PGOOD	Not_Assigned		
Watchdog monitoring 🖌 Enabled	Watchdog mode Simple_WD	<ul> <li>Simple_WD</li> </ul>		
ERRMON monitoring Disabled	d FCCU monitoring	Disabled		
Fault recovery strategy Disabled	d Device I2C address D0	• D0		
	write Read			
				aaa-032351

#### Figure 42. TestMode: Mirrors\_FailSafe

The Read button provides the current status. The Write button changes the configuration in mirror register. This can be useful, for example, to modify few parameters from OTP fuse to start up the board.

## 9 References

- [1] **KITFS85AEEVM** detailed information on this board, including documentation, downloads, and software and tools <u>http://www.nxp.com/KITFS85AEEVM</u>
- [2] **FS8500** product information on FS8500, Safety system basis chip for S32 microcontrollers, ASIL D capable <u>http://www.nxp.com/FS8500</u>
- [3] FS8400 product information on FS8400, Safety system basis chip for S32 microcontrollers, ASIL B capable <u>http://www.nxp.com/FS8400</u>
- [4] FS85\_FS84\_OTP\_Config.xlsm OTP configuration file

## 10 Revision history

Revision	levision history							
Rev	Date	Description						
v.2.1	20200130	<u>Section 2, Section 3.4, Section 4.4</u> : fixed links (tool summary)						
v.2	20191206	<ul> <li><u>Section 8.1</u>: updated <u>Figure 23</u></li> <li><u>Section 8.2</u>: updated description and <u>Figure 24</u></li> <li><u>Section 8.3</u>: updated <u>Figure 26</u></li> <li><u>Section 8.3.1</u>: updated <u>Figure 28</u></li> <li><u>Section 8.4.1</u>: updated <u>Figure 31</u></li> </ul>						
		<ul> <li>Section 8.4.2: updated Figure 32</li> <li>Section 8.4.6: updated Figure 36</li> <li>Section 8.4.3: updated Figure 33</li> <li>Section 8.4.10: updated Figure 41</li> </ul>						
v.1	20190220	Initial version						

## KITFS85AEEVM evaluation board

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