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NTE4096B
Integrated Circuit
CMOS, Gated J–K Master–Slave Flip–Flop w/Set–Reset Capability and Inverting and Non–Inverting J & K Inputs

Description:

The NTE40896B is a J–K Master–Slave Flip–Flop in a 14–Lead DIP type package featuring separate AND gating of multiple J and K inputs. The gated J–K inputs control transfer of information into the master section during clocked operation. Information on the J–K inputs is transferred to the Q and $\overline{Q}$ outputs on the positive edge of the clock pulse. SET and RESET inputs (active high) are provided for asynchronous operation.

Features:

- 16Mhz Toggle Rate (Typ) at $V_{DD} - V_{SS} = 10V$
- Gated Inputs
- Quiescent Current Specified to 20V
- Maximum Input Leakage of 1μA at 20V over Full Package Temperature Range
- 1V Noise Margin (Full Package Range)
- 5V, 10V, and 15V Parametric Ratings

Applications:

- Registers
- Counters
- Control Circuits

Absolute Maximum Ratings:

DC Supply Voltage Range (Voltages referenced to V_{SS} terminal), V_{DD} . . . . . –0.5 to +20V
Input Voltage Range, All Inputs . . . . . –0.5 to V_{DD}+0.5V
Power Dissipation (T_A = –55° to +100°C), P_D 500mW
T_A = +100° to +125°C . . . . . Derate Linearly at 12mW/°C to 200mW
Device Dissipation (Per Output Transistor)
For T_A = Full Package Temperature Range 100mW
Operating Temperature Range, T_A . . . . . –55° to +125°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 1/16” ±1/32” from case, 10sec Max), T_L . . . . . +265°C

Recommended Operating Conditions: (T_A = +25°C, Note 1 unless otherwise specified)

Parameter	Min	Typ	Max	Unit
Supply Voltage Range (For T_A = Full package Temperature)	3	–	18	V
Dat Setup Time, t_S				
V_{DD} = 5V	400	–	–	ns
V_{DD} = 10V	160	–	–	ns
V_{DD} = 15V	100	–	–	ns
Clock Pulse Width, t_W				
V_{DD} = 5V	140	–	–	ns
V_{DD} = 10V	60	–	–	ns
V_{DD} = 15V	40	–	–	ns
Clock Input Frequency, f_{CL}				
V_{DD} = 5V	dc	–	3.5	MHz
V_{DD} = 10V	dc	–	8.0	MHz
V_{DD} = 15V	dc	–	12.0	MHz
Clock Rise or Fall Time, t_{rCL}, t_{fCL}				
V_{DD} = 5V	–	–	15	µs
V_{DD} = 10V	–	–	15	µs
V_{DD} = 15V	–	–	5	µs
Set or Reset Pulse Width, t_W				
V_{DD} = 5V	200	–	–	ns
V_{DD} = 10V	100	–	–	ns
V_{DD} = 15V	50	–	–	ns

Note 1. For maximum reliability, nominal operating conditions should be selected so that operation is always within the above ranges.

Static Electrical Characteristics:

Characteristic	Conditions			Limits at Indicated Temperature (°C)							Units
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55°C	–40°C	+85°C	+125°C	+25°C			
								Min.	Typ.	Max.	
Quiescent Device Current I_L Max.	–	–	5	5	5	50	100	–	0.02	5	µA
	–	–	10	10	10	100	200	–	0.02	10	µA
	–	–	15	20	20	200	400	–	0.02	20	µA
	–	–	20	100	100	1000	2000	–	0.04	100	µA
Output Drive Current N–Ch (Sink) I_DN Min.	0.4	–	5	0.5	0.45	0.36	0.3	0.4	0.8	–	mA
	0.5	–	10	1.1	1.0	0.75	0.65	0.9	1.8	–	mA
	1.5	–	15	3.3	3.2	2.5	2.2	3.0	6.0	–	mA
Output High Current P–Ch (Source) I_DP Min.	4.6	–	5	–0.5	–0.45	–0.36	–0.3	–0.4	–0.8	–	mA
	2.5	–	5	–2.0	–1.8	–1.3	–1.15	–1.6	–3.2	–	mA
	9.5	–	10	–1.1	–1.0	–0.75	–0.65	–0.9	–1.8	–	mA
	13.5	–	15	–3.3	–3.2	–2.5	–2.2	–3.0	–6.0	–	mA

Static Electrical Characteristics (Cont'd):

Characteristic	Conditions			Limits at Indicated Temperature (°C)							Units
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55°C	–40°C	+85°C	+125°C	+25°C			
								Min.	Typ.	Max.	
Output Voltage Low–Level V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	V
	–	0,15	15	0.05				–	0	0.05	V
Output Voltage High–Level V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	V
	–	0,10	10	9.95				9.95	10	–	V
	–	0,15	15	14.95				14.95	15	–	V
Noise Immunity Input Low V_{NL} Min.	4.2	–	5	1.5				1.5	2.25	–	V
	9	–	10	3.0				3.0	4.5	–	V
	13.5	–	15	4.5				4.5	6.75	–	V
Noise Immunity Inputs High V_{NH} Min.	0.8	–	5	1.5				1.5	2.25	–	V
	1.0	–	10	3.0				3.0	4.5	–	V
	1.5	–	15	4.5				4.5	6.75	–	V
Noise Margin Input Low V_{NML} Min.	4.5	–	5	1.0				1.0	–	–	V
	9	–	10	1.0				1.0	–	–	V
	13.5	–	15	1.0				1.0	–	–	V
Noise Margin Inputs High V_{NMH} Min.	0.5	–	5	1.0				1.0	–	–	V
	1.0	–	10	1.0				1.0	–	–	V
	1.5	–	15	1.0				1.0	–	–	V
Input Current, I_{IN} Max.	Any Input		20	±0.1	±0.1	±1.0	±1.0	–	$\pm 10^{-5}$	±0.1	µA

Dynamic Electrical Characteristics:

(T_A = +25°C, C_L = 50pF, R_L = 200kΩ, t_r and t_f = 20ns unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time	t_{PHL}, t_{PLH}	V_{DD} = 5V	–	250	500	ns
		V_{DD} = 10V	–	100	200	ns
		V_{DD} = 15V	–	75	150	ns
Set or Reset		V_{DD} = 5V	–	150	300	ns
		V_{DD} = 10V	–	75	150	ns
		V_{DD} = 15V	–	50	100	ns
Clock Rise or Fall Time	t_r, t_f	V_{DD} = 5V	–	–	15	µs
		V_{DD} = 10V	–	–	15	µs
		V_{DD} = 15V	–	–	15	µs
Transition Time	t_{THL} or t_{TLH}	V_{DD} = 5V	–	100	200	ns
		V_{DD} = 10V	–	50	100	ns
		V_{DD} = 15V	–	40	80	ns
Maximum Clock Input Frequency	f_{CL}	V_{DD} = 5V	3.5	7.0	–	MHz
		V_{DD} = 10V	8.0	16.0	–	MHz
		V_{DD} = 15V	12.0	24.0	–	MHz

Dynamic Electrical Characteristics (Cont'd): (T_A = +25°C, C_L = 50pF, R_L = 200kΩ, t_r and t_f = 20ns unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Minimum Clock Pulse Width	t_W	V_{DD} = 5V	–	70	140	ns
		V_{DD} = 10V	–	30	60	ns
		V_{DD} = 15V	–	20	40	ns
Minimum Set or Reset Pulse Width	t_W	V_{DD} = 5V	–	100	200	ns
		V_{DD} = 10V	–	50	100	ns
		V_{DD} = 15V	–	25	50	ns
Minimum Data Setup Time	t_S	V_{DD} = 5V	–	200	400	ns
		V_{DD} = 10V	–	80	160	ns
		V_{DD} = 15V	–	50	100	ns
Average Input Capacitance	C_I	Any Input	–	5.0	–	pF

Truth Table:

Synchronous Operation (S = 0, R = 0)

Inputs Before Positive Clock Transition		Outputs After Positive Clock Transition	
J	**K**	**Q**	$\overline{\mathbf{Q}}$
0	0	No Change	
0	1	0	1
1	0	1	0
1	1	No Change	

J = J1 • J2 • $\overline{J3}$
K = K1 • K2 • $\overline{K3}$

Asynchronous Operation (J & K – Don't Care)

S	R	Q	$\overline{\mathbf{Q}}$
0	0	No Change	
0	1	0	1
1	0	1	0
1	1	0	0

0 = V_{SS}, 1 = V_{DD}

Pin Connection Diagram