



## Product Change Notification - SYST-24RBCN444

---

**Date:**

25 Jul 2019

**Product Category:**

16-Bit - Microcontrollers and Digital Signal Controllers

**Affected CPNs:**



**Notification subject:**

ERRATA - PIC24FJ1024GA610/GB610 Family Silicon Errata and Data Sheet Clarification

**Notification text:**

SYST-24RBCN444

Microchip has released a new DeviceDoc for the PIC24FJ1024GA610/GB610 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these read the document located at [PIC24FJ1024GA610/GB610 Family Silicon Errata and Data Sheet Clarification](#).

**Notification Status:** Final

**Description of Change:**

- 1.) Added silicon revision A6
- 2.) Added silicon issue 18 (Oscillator).

**Impacts to Data Sheet:** None

**Reason for Change:** To Improve Productivity

**Change Implementation Status:** Complete

**Estimated First Ship Date:** 25 Jul 2019

NOTE: Please be advised that after the estimated first ship may receive pre and post change parts.

**Markings to Distinguish Revised from Unrevised Devices:** Traceability Code

**Attachment(s):**

[PIC24FJ1024GA610/GB610 Family Silicon Errata and Data Sheet Clarification](#)

Please contact your local [Microchip sales office](#) with questions or concerns regarding this notification.

**Terms and Conditions:**

If you wish to receive Microchip PCNs via email please register for our PCN email service at our [PCN home page](#) select register then fill in the required fields. You will find instructions about registering for Microchips PCN email service in the [PCN FAQ](#) section.

If you wish to change your PCN profile, including opt out, please go to the [PCN home page](#) select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

Affected Catalog Part Numbers (CPN)

PIC24FJ1024GA610-I/BG  
PIC24FJ1024GA610-I/PT  
PIC24FJ1024GA610-I/PTC01  
PIC24FJ1024GA610T-I/BG  
PIC24FJ1024GA610T-I/PT  
PIC24FJ1024GA610T-I/PTC01  
PIC24FJ1024GB610-I/BG  
PIC24FJ1024GB610-I/PT  
PIC24FJ1024GB610-I/PTREL  
PIC24FJ1024GB610T-I/BG  
PIC24FJ1024GB610T-I/PT



PIC24FJ1024GA610/GB610 Family Silicon Errata and Data Sheet Clarification

The PIC24FJ1024GA610/GB610 family devices conform functionally to the current Device Data Sheet (DS30010074F), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC24FJ1024GA610/GB610 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (A6).

Data Sheet clarifications and corrections start on page 10, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip’s programmers, debuggers and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

- 1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
a) For MPLAB IDE 8, select Programmer > Reconnect.
b) For MPLAB X IDE, select Window > Dashboard and click the Refresh Debug Tool Status icon.
5. Depending on the development tool used, the part number and Device Revision ID value appear in the Output window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24FJ1024GA610/GB610 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Table with 5 columns: Part Number, Device ID, and Revision ID for Silicon Revision (A2, A3, A4, A5, A6). Rows list various PIC24FJ1024GA610/GB610 family devices and their corresponding IDs.

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format “DEVID DEVREV”.

Note 2: Refer to the “PIC24FJ1024GA610/GB610 Family Flash Programming Specification” (DS30010057) for detailed information on Device and Revision IDs for your specific device.

# PIC24FJ1024GA610/GB610 FAMILY

---

TABLE 1: SILICON DEVREV VALUES (CONTINUED)

| Part Number      | Device ID <sup>(1)</sup> | Revision ID for Silicon Revision <sup>(2)</sup> |      |      |      |      |
|------------------|--------------------------|---|------|------|------|------|
|                  |                          | A2  | A3   | A4   | A5   | A6   |
| PIC24FJ512GB606  | 6014h                    | 0x02  | 0x03 | 0x04 | 0x05 | 0x06 |
| PIC24FJ1024GB606 | 601Ch                    |   |      |      |      |      |
| PIC24FJ128GB610  | 6005h                    |   |      |      |      |      |
| PIC24FJ256GB610  | 600Dh                    |   |      |      |      |      |
| PIC24FJ512GB610  | 6015h                    |   |      |      |      |      |
| PIC24FJ1024GB610 | 601Dh                    |   |      |      |      |      |

**Note 1:** The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format “DEVID DEVREV”.

**2:** Refer to the “*PIC24FJ1024GA610/GB610 Family Flash Programming Specification*” (DS30010057) for detailed information on Device and Revision IDs for your specific device.

# PIC24FJ1024GA610/GB610 FAMILY

**TABLE 2: SILICON ISSUE SUMMARY**

| Module                              | Feature                                 | Item Number | Issue Summary   | Affected Revisions <sup>(1)</sup> |    |    |    |    |   |
|-------------------------------------|---|-------------|---|-----------------------------------|----|----|----|----|---|
|                                     |   |             |   | A2                                | A3 | A4 | A5 | A6 |   |
| Power                               | Low-Voltage Retention Regulator         | 1.          | If a wake-up trigger occurs within 2 $\mu$ S of entering Retention Sleep, the part may not properly wake from Retention Sleep.  | X                                 |    |    |    |    |   |
| Power                               | CPU                                     | 2.          | Part fails to start from power-on when the temperature is below -10°C and V <sub>DD</sub> is $\leq$ 2.7V.   | X                                 |    |    |    |    |   |
| Power                               | Low-Voltage Retention Regulator         | 3.          | Repeated Wake Retention Sleep cycling can cause the internal LDO to exceed its maximum voltage output specification.  | X                                 |    |    |    |    |   |
| ADC                                 | Charge Injection                        | 4.          | At the beginning of conversion, a small current can be injected into the ADC input pin. This will cause a voltage spike dependent on the source resistance.   | X                                 | X  | X  | X  | X  | X |
| I <sup>2</sup> C                    | Slave Addressing                        | 5.          | When AHEN (I2CxCONH[1]) = 1, a slave interrupt is asserted for invalid address or software NACK (after 9th clock).  | X                                 | X  | X  | X  | X  | X |
| MCCP/SCCP                           | Output Compare                          | 6.          | Single Edge Output Compare Event Status bit (SCEVT) is not setting for MOD[3:0] = 0010.   | X                                 | X  | X  | X  | X  | X |
| Reset                               | Trap Conflict                           | 7.          | The TRAPR bit is not getting set when a hard trap conflict occurs.  | X                                 | X  | X  | X  | X  | X |
| I <sup>2</sup> C                    | Slave Mode                              | 8.          | In 10-Bit Addressing Slave mode, on receiving the upper address byte (A9 and A8 bits), the Acknowledge Time Status bit (ACKTIM) is not asserted during the Acknowledgment sequence.                               | X                                 | X  | X  | X  | X  | X |
| Primary XT and HS Oscillator (POSC) | Primary Oscillator Start-up Timer (OST) | 9.          | OST may indicate oscillator is ready for use too early.   | X                                 | X  | X  | X  | X  | X |
| Power                               | Sleep Mode                              | 10.         | Sleep current may exceed the value specified in the data sheet.   | X                                 | X  |    |    |    |   |
| Power                               | Retention Sleep Mode                    | 11.         | When the device wakes up from Retention Sleep mode (RETEN bit (RCON[12]) = 1, LPCFG bit (FPOR[2]) = 0), a device Reset may occur. The BOR, POR and EXTR bits in RCON register are set erroneously for this Reset. | X                                 | X  |    |    |    |   |
| I/O                                 | Schmitt Trigger                         | 12.         | Schmitt trigger may have glitches for slow signal rise/fall times.  | X                                 | X  | X  |    |    |   |
| SPI                                 | Slave Mode                              | 13.         | The SRMT bit may be set when the FIFO or Shift register is not empty.   | X                                 | X  | X  | X  | X  | X |
| ADC                                 | Electrical Characteristics              | 14.         | At cold temperatures, ADC characteristics may be beyond the data sheet specification.   | X                                 | X  | X  | X  |    |   |
| Power                               | BOR                                     | 15.         | The main BOR may not function.  | X                                 | X  | X  |    |    |   |
| I/O                                 | I/O                                     | 16.         | I/O is not tri-stated if TRISx bit is changed from '0' to '1'.  | X                                 | X  | X  | X  | X  | X |
| ADC                                 | Current                                 | 17.         | ADC draws additional current when enabled.  | X                                 | X  | X  | X  |    |   |
| Oscillator                          | 96 MHz PLL Mode                         | 18.         | PLL in 96 MHz mode may not operate under certain conditions.  | X                                 | X  | X  | X  |    |   |

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.

# PIC24FJ1024GA610/GB610 FAMILY

## Silicon Errata Issues

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A6**).

### 1. Module: Power

If a wake-up trigger occurs within 2  $\mu$ S of entering Retention Sleep, the part may not properly wake from Retention Sleep.

#### Work around

None.

#### Affected Silicon Revisions

| A2 | A3 | A4 | A5 | A6 |  |  |  |
|----|----|----|----|----|--|--|--|
| X  |    |    |    |    |  |  |  |

### 2. Module: Power

Part fails to start from power-on when the temperature is below  $-10^{\circ}\text{C}$  and  $V_{DD}$  is  $\leq 2.7\text{V}$ .

#### Work around

Ensure the  $V_{DD}$  and  $AV_{DD}$  are 2.75V or higher, or that the device will not be exposed to temperatures below  $-10^{\circ}\text{C}$ .

#### Affected Silicon Revisions

| A2 | A3 | A4 | A5 | A6 |  |  |  |
|----|----|----|----|----|--|--|--|
| X  |    |    |    |    |  |  |  |

### 3. Module: Power

Repeated Wake Retention Sleep cycling can cause the internal LDO to exceed its maximum voltage output specification if the VREGS bit ( $\text{RCON}[8]$ ) = 1.

#### Work around

The code must execute for 1 ms minimum before returning to Retention Sleep mode or VREGS can be set to '0' in the application.

#### Affected Silicon Revisions

| A2 | A3 | A4 | A5 | A6 |  |  |  |
|----|----|----|----|----|--|--|--|
| X  |    |    |    |    |  |  |  |

### 4. Module: ADC

At the beginning of conversion, a small current can be injected into the ADC input pin. This will cause a voltage spike dependent on the source resistance.

#### Work around

Any of the following solutions can be used:

- Use external buffer on transducer output if the source resistance is greater than 2 k $\Omega$ .
- Increase the TAD time to be 1  $\mu$ S or greater.
- Increase the sample time to be longer than 1  $\mu$ S.

#### Affected Silicon Revisions

| A2 | A3 | A4 | A5 | A6 |  |  |  |
|----|----|----|----|----|--|--|--|
| X  | X  | X  | X  | X  |  |  |  |

### 5. Module: I<sup>2</sup>C

When  $\text{AHEN} (\text{I2CxCONH}[1]) = 1$ , a slave interrupt is asserted for an invalid address or software NACK (after 9th clock).

#### Work around

User application should ignore the extra interrupt until a Stop condition is seen on the data bus.

#### Affected Silicon Revisions

| A2 | A3 | A4 | A5 | A6 |  |  |  |
|----|----|----|----|----|--|--|--|
| X  | X  | X  | X  | X  |  |  |  |

# PIC24FJ1024GA610/GB610 FAMILY

## 6. Module: MCCP/SCCP

The Single Edge Compare Event Status bit, SCEVT (CCPxSTATL[3]), may not set for Single Edge mode (drive output low on match (MOD[3:0] = 0010)). In this case, the comparator output is still driven low on the first CCPxRA match, but will not be reset by writing '0' to the SCEVT bit.

All MCCPs/SCCPs are affected.

### Work around

This mode may be used to trigger a single event before the module must be reinitialized by clearing and setting CCPON (CCP1CON1L[15]).

The Capture/Compare Interrupt Flag (CCPxIF) still occurs on a match with CCPxRA, and can be used to update the user that a compare event has been triggered and the module needs to be reset.

### Affected Silicon Revisions

| A2 | A3 | A4 | A5 | A6 |  |  |  |
|----|----|----|----|----|--|--|--|
| X  | X  | X  | X  | X  |  |  |  |

## 7. Module: Reset

If a lower priority address error trap occurs while a higher priority oscillator failure trap is being processed, the TRAPR bit (RCON[15]) is not set. A Trap Conflict Reset does not occur as expected and the device may stop executing code.

### Work around

None. However, a Reset (such as  $\overline{\text{MCLR}}$ , POR or WDT) will recover the device.

### Affected Silicon Revisions

| A2 | A3 | A4 | A5 | A6 |  |  |  |
|----|----|----|----|----|--|--|--|
| X  | X  | X  | X  | X  |  |  |  |

## 8. Module: I<sup>2</sup>C

In I<sup>2</sup>C Slave 10-Bit Addressing mode, on receiving the upper address byte (A9 and A8 bits), the Acknowledge Time Status bit, ACKTIM (I2CxSTAT[13]), is not asserted during an Acknowledgment sequence.

This issue is not seen during the reception of the lower address byte (A7 to A0) and data bytes. The hardware asserts the ACKTIM bit on the falling edge of the eighth clock and deasserts on the rising edge of the ninth clock. In this case, ACKTIM is not asserted on the upper address byte reception.

When AHEN (I2CxCONL[1]) = 1, the clock is stretched after the 8th falling edge and the ACKTIM bit is asserted until the clock is released. If AHEN = 0, the clock is not stretched and ACKTIM is asserted during the Acknowledgment sequence, which is of a very short duration.

Therefore, the user application can see this issue of the ACKTIM bit not getting asserted when AHEN = 1.

### Work around

Instead of polling for ACKTIM to be asserted, poll for the RBF flag (I2CxSTAT[1]).

### Affected Silicon Revisions

| A2 | A3 | A4 | A5 | A6 |  |  |  |
|----|----|----|----|----|--|--|--|
| X  | X  | X  | X  | X  |  |  |  |

# PIC24FJ1024GA610/GB610 FAMILY

---

## 9. Module: Primary XT and HS Oscillator (POSC)

The Primary Oscillator Start-up Timer (OST) may indicate the oscillator is ready for use too early. Clocking the device before the oscillator is ready may result in incorrect execution and exceptions. This issue exists when the POSC is requested at power-on, during clock switching, when waking from Sleep or when a peripheral module requests the POSC directly. This issue affects XT and HS modes only.

### Work around

Make sure that the Primary Oscillator clock is ready before using it by following these steps:

1. Running on a non-POSC source, request the POSC clock using a peripheral such as REFO.
2. Provide a delay to stabilize the POSC.
3. Switch to the POSC source.

[Example 1](#) shows a work around for the device power-on and [Example 2](#) explains the work around when the device wakes from Sleep.

### EXAMPLE 1: USING POSC AT POWER-ON

```
#pragma config FNOSC = FRC           // Oscillator Selection bits (Fast RC oscillator (FRC))
// Clock Switching Enabled (Fail-safe Clock Monitor can be enabled or disabled)
#pragma config FCKSM = CSECMD
-----
int main()
{
    // configure REFO to request POSC
    REFOCONLbits.ROSEL = 2;           // POSC
    REFOCONLbits.ROOUT = 0;           // disable output
    REFOCONLbits.ROEN = 1;           // enable module

    // wait for POSC stable clock
    // this delay may vary depending on different application conditions
    // such as voltage, temperature, layout, XT or HS mode and components
    { // delay for 9 ms
        unsigned int delaysms = 9;
        while(delaysms--) asm volatile("repeat #(8000000/1000/2) \n nop");
    }

    // switch to POSC = 2
    __builtin_write_OSCCONH(2);
    __builtin_write_OSCCONL(1);
    while(OSCCONbits.OSWEN == 1);    // wait for switch
```



# PIC24FJ1024GA610/GB610 FAMILY

## EXAMPLE 2: USING POSC WHEN WAKING FROM SLEEP

```
// Clock Switching Enabled (Failsafe Clock Monitor can be enabled or disabled)
#pragma config FCKSM = CSECMD
-----
// switch to FRC = 0 before entering sleep
__builtin_write_OSCCONH(0);
__builtin_write_OSCCONL(1);
while(OSCCONbits.OSWEN == 1);    // wait for switch

// enter sleep mode
Sleep();

// configure REFO to request POSC
REFOCONLbits.ROSEL = 2;          // POSC
REFOCONLbits.ROOUT = 0;          // disable output
REFOCONLbits.ROEN = 1;          // enable module

// wait for POSC stable clock
// this delay may vary depending on different application conditions
// such as voltage, temperature, layout, XT or HS mode and components
{ // delay for 9 ms
    unsigned int delay ms = 9;
    while(delayms--) asm volatile("repeat #(8000000/1000/2) \n nop");
}

// switch to POSC = 2
__builtin_write_OSCCONH(2);
__builtin_write_OSCCONL(1);
while(OSCCONbits.OSWEN == 1);    // wait for switch
```

### Affected Silicon Revisions

| A2 | A3 | A4 | A5 | A6 |  |  |  |
|----|----|----|----|----|--|--|--|
| X  | X  | X  | X  | X  |  |  |  |

# PIC24FJ1024GA610/GB610 FAMILY

## 10. Module: Power

The Sleep current may exceed a value specified in the data sheet. The issue affects regular (non-Retention) Sleep modes.

### Work around

Set the RETEN bit (RCON[12]) = 1 and disable the Retention Sleep mode by setting the LPCFG Configuration bit (FPOR[2]) = 1.

### Affected Silicon Revisions

| A2 | A3 | A4 | A5 | A6 |  |  |  |
|----|----|----|----|----|--|--|--|
| X  | X  |    |    |    |  |  |  |

## 11. Module: Power

When the device wakes up from Retention Sleep mode (RETEN bit (RCON[12]) = 1, LPCFG bit (FPOR[2]) = 0), occasionally a device Reset may occur. The BOR, POR and EXTR bits in the RCON register are set erroneously for this Reset.

### Work around

To provide a consistent behavior when the device wakes up from the Retention Sleep mode, the software RESET instruction should be inserted following the SLEEP instruction. In this case, a Reset will always be generated when the device wakes up from Retention Sleep. [Example 3](#) shows the software RESET instruction implementation:

### **EXAMPLE 3: SOFTWARE RESET AFTER SLEEP INSTRUCTION**

```
// ENTER SLEEP MODE.
asm volatile ("pwrsav #0");
// SOFTWARE RESET RIGHT AFTER SLEEP.
asm volatile ("reset");
```

### Affected Silicon Revisions

| A2 | A3 | A4 | A5 | A6 |  |  |  |
|----|----|----|----|----|--|--|--|
| X  | X  |    |    |    |  |  |  |

## 12. Module: I/O

If the input signal rise or fall time is greater than 200 nS, the I/O Schmitt trigger output may have glitches.

### Work around

The rise/fall times must be less than 200 nS.

### Affected Silicon Revisions

| A2 | A3 | A4 | A5 | A6 |  |  |  |
|----|----|----|----|----|--|--|--|
| X  | X  | X  |    |    |  |  |  |

## 13. Module: SPI

In SPI Slave mode, the SRMT bit may be set when the TX FIFO or Shift register is not empty.

### Work around

The following work arounds can be implemented in the application to detect when the FIFO and Shift register are empty:

1. Check the SPITBF bit before checking the SRMT bit. If the SPITBF flag is cleared and the SRMT flag is set, then all data were transmitted. [Example 4](#) demonstrates the SPITBF and SRMT bits polling.
2. Read the SRMT bit twice, back-to-back. If the SRMT bit is set two reads in a row, then the FIFO and Shift Register are empty. [Example 5](#) demonstrates the SRMT bit polling using double read.

### **EXAMPLE 4: EMPTY STATUS DETECTION USING SPITBF AND SRMT BITS POLLING**

```
// Both flags must indicate empty status.
while(SPI1STATLbits.SPITBF);
while(!SPI1STATLbits.SRMT);
```

### **EXAMPLE 5: EMPTY STATUS DETECTION USING SRMT BIT POLLING WITH BACK-TO-BACK READS**

```
// If SRMT bit is set two reads in a row then
it set correctly.
asm volatile("loop:\n"
            "btsc SPI1STATL, #7\n"
            "btss SPI1STATL, #7\n"
            "bra loop");
```

### Affected Silicon Revisions

| A2 | A3 | A4 | A5 | A6 |  |  |  |
|----|----|----|----|----|--|--|--|
| X  | X  | X  | X  | X  |  |  |  |

# PIC24FJ1024GA610/GB610 FAMILY

## 14. Module: ADC

When the ADC input voltage is above  $(AV_{DD} - 0.2)V$ , and the device operates in the temperature range of  $0^{\circ}C$  to  $-40^{\circ}C$ , the INL and Gain error can get bigger as the ADC input voltage increases, up to -11 LSB Gain and -13 LSB INL.

### Work around

Choose the ADC positive reference ( $V_{REF+}$ ) below  $(AV_{DD} - 0.2)V$ . This ensures the ADC input voltage will operate to ADC full scale without affecting the ADC specification.

### Affected Silicon Revisions

| A2 | A3 | A4 | A5 | A6 |  |  |  |
|----|----|----|----|----|--|--|--|
| X  | X  | X  | X  |    |  |  |  |

## 15. Module: Power

The main BOR may not occur when the operating voltage drops below the BOR trip voltage.

### Work around

Ensure the device operating voltage does not violate the specified values. Use an external supervisor circuit to reset the device if the operating voltage can be outside the specified values.

### Affected Silicon Revisions

| A2 | A3 | A4 | A5 | A6 |  |  |  |
|----|----|----|----|----|--|--|--|
| X  | X  | X  |    |    |  |  |  |

## 16. Module: I/O

5V tolerant I/Os may not be set to a high-impedance state if the corresponding TRISx bit is changed from '0' to '1'. The I/O state change from output to high-impedance may be delayed up to 100 mS, depending on external connections. On Silicon Revision A5 and later, only the following I/Os are affected by this issue: RA2, RA3, RA14, RA15, RD9, RD10, RE6, RE7, RF4, RF5, RG2 and RG3.

### Work around

Set I/O to low level ( $LATx$  bit = 0) before switching to input ( $TRISx$  bit = 1).

### Affected Silicon Revisions

| A2 | A3 | A4 | A5 | A6 |  |  |  |
|----|----|----|----|----|--|--|--|
| X  | X  | X  | X  | X  |  |  |  |

## 17. Module: ADC

On some devices, the current draw may increase when the ADC is enabled. This current draw is not affected by the device Power Save modes or ADC configuration. This additional current does not affect the ADC or device performance.

### Work around

Disable the ADC when it is not converting or not used in the application.

### Affected Silicon Revisions

| A2 | A3 | A4 | A5 | A6 |  |  |  |
|----|----|----|----|----|--|--|--|
| X  | X  | X  | X  |    |  |  |  |

## 18. Module: Oscillator

The PLL in 96 MHz mode may not function when the device starts up and the capacitor on the VCAP pin is discharged. This condition is applicable in both Two-Speed Oscillator Start-up and clock switching at run time.

### Work around

1. The 8x/6x/4x PLL modes are functional and available for use.
2. If 96 MHz PLL mode is required for application (ex: USB), connect a 1  $\mu F$  capacitor between VDD and VCAP to precharge the VCAP capacitor.

### Affected Silicon Revisions

| A2 | A3 | A4 | A5 | A6 |  |  |  |
|----|----|----|----|----|--|--|--|
| X  | X  | X  | X  |    |  |  |  |

# PIC24FJ1024GA610/GB610 FAMILY

---

## Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (30010074F):

**Note:** Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

### 1. Module: Electrical Characteristics

In [Table 33-8](#), the values for the DI30 and DI30A parameters (internal pull-up and pull-down currents) should be 150  $\mu\text{A}$  for Minimum and 500  $\mu\text{A}$  for Maximum, as shown in **bold** below.

**TABLE 33-8: I/O PIN INPUT SPECIFICATIONS**

| Standard Operating Conditions: $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (unless otherwise stated) |        |                       |            |            |               |   |
|--|--------|-----------------------|------------|------------|---------------|---|
| Param No.  | Symbol | Characteristic        | Min        | Max        | Units         | Conditions                                  |
| DI30   | ICNPU  | CNx Pull-up Current   | 150        | <b>500</b> | $\mu\text{A}$ | $V_{DD} = 3.3\text{V}$ , $V_{PIN} = V_{SS}$ |
| DI30A  | ICNPD  | CNx Pull-Down Current | <b>150</b> | 500        | $\mu\text{A}$ | $V_{DD} = 3.3\text{V}$ , $V_{PIN} = V_{DD}$ |

# PIC24FJ1024GA610/GB610 FAMILY

---

## APPENDIX A: DOCUMENT REVISION HISTORY

### Rev A Document (11/2015)

Initial release of this document; issued for Silicon Revision A2.

### Rev B Document (11/2015)

Added data sheet clarification 1 (Device Names and Peripherals).

### Rev C Document (3/2016)

Added silicon revision A3.

Removed data sheet clarification 1 (Device Names and Peripherals).

### Rev D Document (7/2016)

Added silicon issue 9 (Primary XT and HS Oscillator (POSC)) and silicon issue 10 (Power).

Added data sheet clarifications 1 and 2 (DC Characteristics).

### Rev E Document (12/2016)

Added silicon issue 11 (Power).

Removed data sheet clarifications 1 and 2 (DC Characteristics).

### Rev F Document (4/2017)

Added Silicon Revision A4.

Added silicon issue 12 (I/O) and silicon issue 13 (SPI).

Added data sheet clarification 1 (Electrical Characteristics).

### Rev G Document (7/2017)

Added silicon issues 14 (ADC) and 15 (Power).

Removed data sheet clarification 1 (Electrical Characteristics) because the issue was corrected in the latest data sheet revision.

### Rev H Document (3/2018)

Added Silicon Revision A5.

Added silicon issue 16 (I/O).

### Rev J Document (1/2019)

Added Silicon issue 17 (ADC).

Added data sheet clarification 1 (Electrical Characteristics).

### Rev K Document (7/2019)

Added silicon revision A6.

Added silicon issue 18 (Oscillator).

# PIC24FJ1024GA610/GB610 FAMILY

---

NOTES:

---

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

---

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

**Trademarks**

The Microchip name and logo, the Microchip logo, Adaptec, AnyRate, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, chipKIT, chipKIT logo, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Klear, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PackeTime, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TempTracker, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

APT, ClockWorks, The Embedded Control Solutions Company, EtherSynch, FlashTec, Hyper Speed Control, HyperLight Load, IntelliMOS, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet-Wire, SmartFusion, SyncWorld, Temux, TimeCesium, TimeHub, TimePictra, TimeProvider, Vite, WinPath, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BlueSky, BodyCom, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, INICnet, Inter-Chip Connectivity, JitterBlocker, KlearNet, KlearNet logo, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICKit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, SAM-ICE, Serial Quad I/O, SMART-I.S., SQI, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, and Symmcom are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2015-2019, Microchip Technology Incorporated, All Rights Reserved.

ISBN: 978-1-5224-4841-9

For information regarding Microchip's Quality Management Systems, please visit [www.microchip.com/quality](http://www.microchip.com/quality).



# MICROCHIP

## Worldwide Sales and Service

### AMERICAS

**Corporate Office**  
2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200  
Fax: 480-792-7277  
Technical Support:  
<http://www.microchip.com/support>  
Web Address:  
[www.microchip.com](http://www.microchip.com)

#### Atlanta

Duluth, GA  
Tel: 678-957-9614  
Fax: 678-957-1455

#### Austin, TX

Tel: 512-257-3370

#### Boston

Westborough, MA  
Tel: 774-760-0087  
Fax: 774-760-0088

#### Chicago

Itasca, IL  
Tel: 630-285-0071  
Fax: 630-285-0075

#### Dallas

Addison, TX  
Tel: 972-818-7423  
Fax: 972-818-2924

#### Detroit

Novi, MI  
Tel: 248-848-4000

#### Houston, TX

Tel: 281-894-5983

#### Indianapolis

Noblesville, IN  
Tel: 317-773-8323  
Fax: 317-773-5453  
Tel: 317-536-2380

#### Los Angeles

Mission Viejo, CA  
Tel: 949-462-9523  
Fax: 949-462-9608  
Tel: 951-273-7800

#### Raleigh, NC

Tel: 919-844-7510

#### New York, NY

Tel: 631-435-6000

#### San Jose, CA

Tel: 408-735-9110  
Tel: 408-436-4270

#### Canada - Toronto

Tel: 905-695-1980  
Fax: 905-695-2078

### ASIA/PACIFIC

**Australia - Sydney**  
Tel: 61-2-9868-6733

**China - Beijing**  
Tel: 86-10-8569-7000

**China - Chengdu**  
Tel: 86-28-8665-5511

**China - Chongqing**  
Tel: 86-23-8980-9588

**China - Dongguan**  
Tel: 86-769-8702-9880

**China - Guangzhou**  
Tel: 86-20-8755-8029

**China - Hangzhou**  
Tel: 86-571-8792-8115

**China - Hong Kong SAR**  
Tel: 852-2943-5100

**China - Nanjing**  
Tel: 86-25-8473-2460

**China - Qingdao**  
Tel: 86-532-8502-7355

**China - Shanghai**  
Tel: 86-21-3326-8000

**China - Shenyang**  
Tel: 86-24-2334-2829

**China - Shenzhen**  
Tel: 86-755-8864-2200

**China - Suzhou**  
Tel: 86-186-6233-1526

**China - Wuhan**  
Tel: 86-27-5980-5300

**China - Xian**  
Tel: 86-29-8833-7252

**China - Xiamen**  
Tel: 86-592-2388138

**China - Zhuhai**  
Tel: 86-756-3210040

### ASIA/PACIFIC

**India - Bangalore**  
Tel: 91-80-3090-4444

**India - New Delhi**  
Tel: 91-11-4160-8631

**India - Pune**  
Tel: 91-20-4121-0141

**Japan - Osaka**  
Tel: 81-6-6152-7160

**Japan - Tokyo**  
Tel: 81-3-6880-3770

**Korea - Daegu**  
Tel: 82-53-744-4301

**Korea - Seoul**  
Tel: 82-2-554-7200

**Malaysia - Kuala Lumpur**  
Tel: 60-3-7651-7906

**Malaysia - Penang**  
Tel: 60-4-227-8870

**Philippines - Manila**  
Tel: 63-2-634-9065

**Singapore**  
Tel: 65-6334-8870

**Taiwan - Hsin Chu**  
Tel: 886-3-577-8366

**Taiwan - Kaohsiung**  
Tel: 886-7-213-7830

**Taiwan - Taipei**  
Tel: 886-2-2508-8600

**Thailand - Bangkok**  
Tel: 66-2-694-1351

**Vietnam - Ho Chi Minh**  
Tel: 84-28-5448-2100

### EUROPE

**Austria - Wels**  
Tel: 43-7242-2244-39  
Fax: 43-7242-2244-393

**Denmark - Copenhagen**  
Tel: 45-4450-2828  
Fax: 45-4485-2829

**Finland - Espoo**  
Tel: 358-9-4520-820

**France - Paris**  
Tel: 33-1-69-53-63-20  
Fax: 33-1-69-30-90-79

**Germany - Garching**  
Tel: 49-8931-9700

**Germany - Haan**  
Tel: 49-2129-3766400

**Germany - Heilbronn**  
Tel: 49-7131-72400

**Germany - Karlsruhe**  
Tel: 49-721-625370

**Germany - Munich**  
Tel: 49-89-627-144-0  
Fax: 49-89-627-144-44

**Germany - Rosenheim**  
Tel: 49-8031-354-560

**Israel - Ra'anana**  
Tel: 972-9-744-7705

**Italy - Milan**  
Tel: 39-0331-742611  
Fax: 39-0331-466781

**Italy - Padova**  
Tel: 39-049-7625286

**Netherlands - Drunen**  
Tel: 31-416-690399  
Fax: 31-416-690340

**Norway - Trondheim**  
Tel: 47-7288-4388

**Poland - Warsaw**  
Tel: 48-22-3325737

**Romania - Bucharest**  
Tel: 40-21-407-87-50

**Spain - Madrid**  
Tel: 34-91-708-08-90  
Fax: 34-91-708-08-91

**Sweden - Gothenberg**  
Tel: 46-31-704-60-40

**Sweden - Stockholm**  
Tel: 46-8-5090-4654

**UK - Wokingham**  
Tel: 44-118-921-5800  
Fax: 44-118-921-5820