SAM E70/S70/V70/V71 Family

32-bit ARM Cortex-M7 MCUs with FPU, Audio and Graphics Interfaces, High-Speed USB, Ethernet, and Advanced Analog

Features

Core

- Arm® Cortex®-M7 running at up to 300 MHz
- 16 Kbytes of I-Cache and 16 Kbytes of D-Cache with Error Code Correction (ECC)
- Single-precision and double-precision HW Floating Point Unit (FPU)
- Memory Protection Unit (MPU) with 16 zones
- DSP Instructions, Thumb®-2 Instruction Set
- Embedded Trace Module (ETM) with instruction trace stream, including Trace Port Interface Unit (TPIU)

Memories

- Up to 2048 Kbytes embedded Flash with unique identifier and user signature for user-defined data
- Up to 384 Kbytes embedded Multi-port SRAM
- Tightly Coupled Memory (TCM)
- 16 Kbytes ROM with embedded Bootloader routines (UART0, USB) and IAP routines
- 16-bit Static Memory Controller (SMC) with support for SRAM, PSRAM, LCD module, NOR and NAND Flash with on-the-fly scrambling
- 16-bit SDRAM Controller (SDRAMC) interfacing up to 128 MB and with on-the-fly scrambling

System

- Embedded voltage regulator for single-supply operation
- Power-on-Reset (POR), Brown-out Detector (BOD) and Dual Watchdog for safe operation
- Quartz or ceramic resonator oscillators: 3 MHz to 20 MHz main oscillator with failure detection, 12 MHz or 16 MHz needed for USB operations. Optional low-power 32.768 kHz for RTC or device clock
- RTC with Gregorian calendar mode, waveform generation in low-power modes
- RTC counter calibration circuitry compensates for 32.768 kHz crystal frequency variations
- 32-bit low-power Real-time Timer (RTT)
- High-precision Main RC oscillator with 12 MHz default frequency
- 32.768 kHz crystal oscillator or Slow RC oscillator as source of low-power mode device clock (SLCK)
- One 500 MHz PLL for system clock, one 480 MHz PLL for USB high-speed operations
- Temperature Sensor
- One dual-port 24-channel central DMA Controller (XDMAC)

Low-Power Features

- Low-power sleep, wait and backup modes, with typical power consumption down to 1.1 µA in Backup mode with RTC, RTT and wakeup logic enabled
- Ultra low-power RTC and RTT
- 1 Kbyte of backup RAM (BRAM) with dedicated regulator

Peripherals

- One Ethernet MAC (GMAC) 10/100 Mbps in MII mode and RMII with dedicated DMA. IEEE® 1588 PTP frames and 802.3az Energy-efficiency support. Ethernet AVB support with IEEE802.1AS Timestamping and IEEE802.1Qav credit-based traffic-shaping hardware support.
- USB 2.0 Device/Mini Host High-speed (USBHS) at 480 Mbps, 4-Kbyte FIFO, up to 10 bidirectional endpoints, dedicated DMA
- 12-bit ITU-R BT. 601/656 Image Sensor Interface (ISI)
- Two master Controller Area Networks (MCAN) with Flexible Data Rate (CAN-FD) with SRAM-based mailboxes, time-triggered and event-triggered transmission
- MediaLB® device with 3-wire mode, up to 1024 x Fs speed, supporting MOST25 and MOST50 networks
- Three USARTs, USART0, USART1, USART2, support LIN mode, ISO7816, IrDA®, RS-485, SPI, Manchester and Modem modes; USART1 supports LON mode.
- Five 2-wire UARTs with SleepWalking™ support
- Three Two-Wire Interfaces (TWIHS) (I^2C-compatible) with SleepWalking support
- Quad I/O Serial Peripheral Interface (QSPI) interfacing up to 256 MB Flash and with eXecute-In-Place and on-the-fly scrambling
- Two Serial Peripheral Interfaces (SPI)
- One Serial Synchronous Controller (SSC) with I^2S and TDM support
- Two Inter-IC Sound Controllers (I2SC)
- One High-speed Multimedia Card Interface (HSMCI) (SDIO/SD Card/e.MMC)
- Four Three-Channel 16-bit Timer/Counters (TC) with Capture, Waveform, Compare and PWM modes, constant on time. Quadrature decoder logic and 2-bit Gray Up/Down Counter for stepper motor
- Two 4-channel 16-bit PWMs with complementary outputs, Dead Time Generator and eight fault inputs per PWM for motor control, two external triggers to manage power factor correction (PFC), DC-DC and lighting control
- Two Analog Front-End Controllers (AFEC), each supporting up to 12 channels with differential input mode and programmable gain stage, allowing dual sample-and-hold (S&H) at up to 1.7 Msps. Offset and gain error correction feature.
- One 2-channel, 12-bit, 1 Msps-per-channel Digital-to-Analog Controller (DAC) with Differential and Over Sampling modes
- One Analog Comparator Controller (ACC) with flexible input selection, selectable input hysteresis

Cryptography

- True Random Number Generator (TRNG)
- AES: 256-bit, 192-bit, 128-bit Key Algorithm, Compliant with FIPS PUB-197 Specifications
- Integrity Check Monitor (ICM). Supports Secure Hash Algorithm SHA1, SHA224 and SHA256.

I/O

- Up to 114 I/O lines with external interrupt capability (edge- or level-sensitivity), debouncing, glitch filtering and On-die Series Resistor Termination
- Five Parallel Input/Output Controllers (PIO)

Voltage

- Single supply voltage from 3.0V to 3.6V for Qualification AEC - Q100 Grade 2 Devices
- Single Supply voltage from 1.7V to 3.6V for Industrial Temperature Devices

Packages

- LQFP144, 144-lead LQFP, 20x20 mm, pitch 0.5 mm
- LFBGA144, 144-ball LFBGA, 10x10 mm, pitch 0.8 mm
- TFBGA144, 144-ball TFBGA, 10x10 mm, pitch 0.8 mm
- UFBGA144, 144-ball UFBGA, 6x6 mm, pitch 0.4 mm
- LQFP100, 100-lead LQFP, 14x14 mm, pitch 0.5 mm
- TFBGA100, 100-ball TFBGA, 9x9 mm, pitch 0.8 mm
- VFBGA100, 100-ball VFBGA, 7x7 mm, pitch 0.65 mm
- LQFP64, 64-lead LQFP, 10x10 mm, pitch 0.5 mm
- QFN64, 64-pad QFN 9x9 mm, pitch 0.5 mm with wettable flanks

1. Configuration Summary

The SAM E70/S70/V70/V71 devices differ in memory size, package and features. The following tables summarize the different configurations.

Table 1-1. SAM V71 Family Features (With CAN-FD, Ethernet AVB and Media LB)

Device	Flash Memory (KB)	Multi-port SRAM Memory (KB)	Pins	Packages	Digital Peripherals																						Analog		
					USB (see Note)	USART/UART	QSPI	USART/SPI	TWIHS	HSMCI port/bits	CAN-FD	Ethernet AVB	Media LB	Image Sensor Interface (ISI)	SPI0	SPI1	External Bus Interface (EBI)	SDRAM Interface	DMA Channels	SSC	ETM	Timer Counter Channels	Timer Counter Channels I/O	I2SC	I/O Pins	12-bit ADC Channels	Analog Comparators	DAC (Channels)
ATSAMV71Q19	512	256	144	LQFP, TFBGA	HS	3/5	Y	3	3	1/4	2	MII, RMII	Y	12 -bit	Y	Y	Y	Y	24	Y	Y	12	36	2	114	24	Y	2
ATSAMV71Q20	1024	384																										
ATSAMV71Q21	2048																											
ATSAMV71N19	512	256	100	LQFP, TFBGA	HS	3/5	Y	3	3	1/4	2	MII, RMII	Y	12 -bit	Y	N	N	N	24	Y	Y	12	9	1	75	10	Y	2
ATSAMV71N20	1024	384																										
ATSAMV71N21	2048																											
ATSAMV71J19	512	256	64	LQFP	-	2/3	SPI only	0	2	N	1	RMII	Y	8-bit	N	N	N	N	24	Y	Y	12	3	0	44	5	Y	1
ATSAMV71J20	1024	384																										
ATSAMV71J21	2048																											

Note: HS = High-Speed and FS = Full-Speed.

Table 1-2. SAM E70 Family Features (With CAN-FD and Ethernet AVB)

Device	Flash Memory (KB)	Multi-port SRAM Memory (KB)	Pins	Packages	Digital Peripherals																						Analog		
					USB (see Note)	USART/UART	QSPI	USART/SPI	TWIHS	HSMCI port/bits	CAN-FD	Ethernet AVB	Image Sensor Interface (ISI)	SPI0	SPI1	External Bus Interface (EBI)	SDRAM Interface	DMA Channels	SSC	ETM	Timer Counter Channels	Timer Counter Channels I/O	I2SC	I/O Pins	12-bit ADC Channels	Analog Comparators	DAC (Channels)
ATSAME70Q19	512	256	144	LQFP, LFBGA, UFBGA	HS	3/5	Y	3	3	1/4	2	MII, RMII	12 -bit	Y	Y	Y	Y	24	Y	Y	12	36	2	114	24	Y	2
ATSAME70Q20	1024	384																										
ATSAME70Q21	2048																											
ATSAME70N19	512	256	100	LQFP, TFBGA	HS	3/5	Y	3	3	1/4	2	MII, RMII	12 -bit	Y	N	N	N	24	Y	Y	12	9	1	75	10	Y	2
ATSAME70N20	1024	384																										
ATSAME70N21	2048																											
ATSAME70J19	512	256	64	LQFP	-	2/3	SPI only	0	2	N	1	RMII	8-bit	N	N	N	N	24	Y	Y	12	3	0	44	5	Y	1
ATSAME70J20	1024	384																										
ATSAME70J21	2048																											

Note: HS = High-Speed and FS = Full-Speed.

Table 1-3. SAM V70 Family Features (With CAN-FD, Without Ethernet Control)

Device	Flash Memory (KB)	Multi-port SRAM Memory (KB)	Pins	Packages	Digital Peripherals																				Analog		
					USB (see Note	USART/UART	QSPI	USART/SPI	TWIHS	HSMCI port/bits	Media LB	CAN-FD	Image Sensor Interface (ISI)	SPI0	SPI1	External Bus Interface (EBI)	SDRAM Interface	DMA Channels	SSC	ETM	Timer Counter Channels	Timer Counter Channels I/O	I2SC	I/O Pins	12-bit ADC Channels	Analog Comparators	DAC (Channels)
ATSAMV70Q19	512	256	144	LQFP, TFBGA	HS	3/5	Y	3	3	1/4	Y	2	12 -bit	Y	Y	Y	Y	24	Y	Y	12	36	2	114	24	Y	2
ATSAMV70Q20	1024	384																									
ATSAMV70N19	512	256	100	LQFP, TFBGA	HS	3/5	Y	3	3	1/4	Y	2	12 -bit	Y	N	N	N	24	Y	Y	12	9	1	75	10	Y	2
ATSAMV70N20	1024	384																									
ATSAMV70J19	512	256	64	LQFP	-	2/3	SPI only	0	2	N	N	1	8-bit	N	N	N	N	24	Y	Y	12	3	0	44	5	Y	1
ATSAMV70J20	1024	384																									

Note: HS = High-Speed and FS = Full-Speed.

Table 1-4. SAM S70 Family Features (Without CAN-FD, Ethernet AVB and Media LB)

Device	Flash Memory (KB)	Multi-port SRAM Memory (KB)	Pins	Packages	Digital Peripherals																			Analog		
					USB (see Note)	USART/UART	QSPI	USART/SPI	TWIHS	HSMCI port/bits	Image Sensor Interface (ISI)	SPI0	SPI1	External Bus Interface (EBI)	SDRAM Interface	DMA Channels	SSC	ETM	Timer Counter Channels	Timer Counter Channels I/O	I2SC	I/O Pins	12-bit ADC Channels	Analog Comparators	DAC Channels
ATSAMS70Q19	512	256	144	LQFP, LFBGA, UFBGA	HS	3/5	Y	3	3	1/4	12 -bit	Y	Y	Y	Y	24	Y	Y	12	36	2	114	24	Y	2
ATSAMS70Q20	1024	384																								
ATSAMS70Q21	2048																									
ATSAMS70N19	512	256	100	LQFP, TFBGA, VFBGA	HS	3/5	Y	3	3	1/4	12 -bit	Y	N	N	N	24	Y	Y	12	9	1	75	10	Y	2
ATSAMS70N20	1024	384																								
ATSAMS70N21	2048																									
ATSAMS70J19	512	256	64	LQFP, QFN	HS (for QFN only)	0/5	SPI only	0	2	N	8-bit	N	N	N	N	24	Y	Y	12	3	0	44	5	Y	1
ATSAMS70J20	1024	384																								
ATSAMS70J21	2048																									

Note: HS = High-Speed and FS = Full-Speed.

2. Ordering Information

ATSAM V71 Q 21 B - AAB

Product Family
SAM = SMART ARM Microcontroller

Product Series
V71 = Cortex-M7 + Advanced Feature Set + Ethernet + 2x CAN-FD + Media LB
V70 = Cortex-M7 + Advanced Feature Set +1 or 2x CAN-FD + Media LB
E70 = Cortex-M7 + Advanced Feature Set + Ethernet + 2x CAN-FD
S70 = Cortex-M7 + Advanced Feature Set

Pin Count
J = 64 pins
N = 100 pins
Q = 144 pins

Flash Memory Density
21 = 2048 KB
20 = 1024 KB
19 = 512 KB

Package Carrier (If Applicable)
T = Tape and Reel

Temperature Operating Range
N = Industrial (-40 - +105°C)
B = Grade 2 (-40 - +105°C)

Package Type
A = LQFP
AA = LQFP (1)
C = LFBGA/TFBGA
CF = UFBGA/VFBGA
M = QFN

Device Variant
A = Revision A, legacy version
B = Revision B, current variant

Note:
1. LQFP package type for Grade 2 variants.