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NTE74154
Integrated Circuit
Transistor Transistor Logic (TTL)
4–Line–to–16–Line Decoder/Demultiplexer

Description:

The NTE74154 is a monolithic 4–line–to–16–line decoder in a 24–Lead DIP type package and utilizes TTL circuitry to decode four binary–coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. This device is ideally suited for implementing high–performance memory decoders.

The NTE74154 is fully compatible for use with most other TTL and DTL circuits. All inputs are buffered and input clamping diodes are provided to minimize transmission–line effects and thereby simplify system design.

Features:

- Ideal for High–Performance Memory Decoding
- Designed for Power–Critical Applications
- Decodes 4 Binary–Coded Inputs into One of 16 Mutually Exclusive Outputs
- Performs the Demultiplexing Functions by Distributing Data From One Input Line to Any One of 16 Outputs
- Input–Clamping Diodes Simplify System Design
- High Fan–Out, Low–Impedance, Totem–Pole Outputs
- Fully Compatible with most TTL, DTL, and MSI Circuits

Absolute Maximum Ratings: (T_A = 0° to +70°C unless otherwise specified)

Supply Voltage (Note 1), V_{CC} 7V
Input Voltage, V_I 5.5V
Operating Ambient Temperature Range, T_A . . . . . 0° to +70°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C

Note 1. Voltage values are with respect to network GND terminal.

Recommended Operation Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High–Level Output Current	I_{OH}	–	–	–800	μA
Low–Level Output Current	I_{OL}	–	–	16	mA
Operating Ambient Temperature	T_A	0	–	70	°C

Electrical Characteristics: (T_A = 0° to +70°C, Note 2 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High−Level Input Voltage	V_{IH}		2	–	–	V
Low−Level Input Voltage	V_{IL}		–	–	0.8	V
Low−Level Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −12mA	–	–	−1.5	V
High−Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −800μA	2.4	3.4	–	V
Low−Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA	–	0.2	0.4	V
Input Current at Max Input Voltage	I_I	V_{CC} = MAX, V_I = 5.5V	–	–	1	mA
High−Level Input Current	I_{IH}	V_{CC} = MAX, V_I = 2.4V	–	–	40	μA
Low−Level Input Current	I_{IL}	V_{CC} = MAX, V_I = 0.4V	–	–	−1.6	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 3	−18	–	−57	mA
Supply Current	I_{CC}	V_{CC} = MAX, Note 4	–	34	56	mA

Note 2. All typical values at V_{CC} = 5V, T_A = +25°C. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

Note 3. Not more than one output should be shorted at a time.

Note 4. I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics: (T_A = +25°C, V_{CC} = 5V unless otherwise specified)

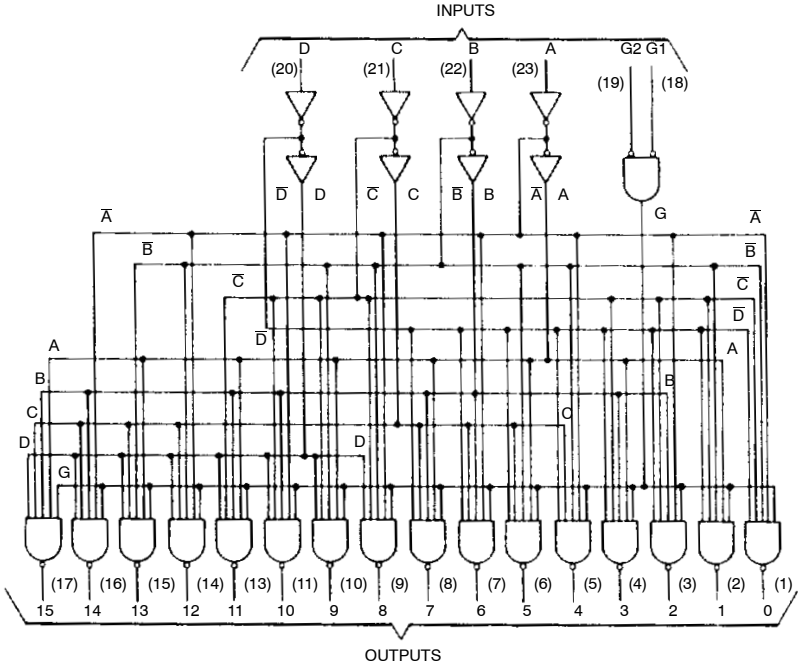
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time, Low−to−High−Level Output, from A, B, C, or D Inputs Through 3 Levels of Logic	t_{PLH}	C_L = 15pF, R_L = 400Ω	–	24	36	ns
Propagation Delay Time, High−to−Low−Level Output, from A, B, C, or D Inputs Through 3 Levels of Logic	t_{PHL}		–	22	33	ns
Propagation Delay Time, Low−to−High−Level Output, from Either Strobe Input	t_{PLH}		–	20	30	ns
Propagation Delay Time, High−to−Low−Level Output, from Either Strobe Input	t_{PHL}		–	18	27	ns

Function Table:

INPUTS						OUTPUTS															
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

Note 5. H = High level, L = Low level, X = Irrelevant

Functional Block Diagram:



Pin Connection Diagram: