Product Change Notification / SYST-11YIGT439

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15-Dec-2020

Product Category:

16-Bit - Microcontrollers and Digital Signal Controllers

PCN Type:

Document Change

Notification Subject:

ERRATA - PIC24FJ64GP205/GU205 Family Silicon Errata and Data Sheet Clarification

Affected CPNs:

SYST-11YIGT439_Affected_CPN_12152020.pdf
SYST-11YIGT439_Affected_CPN_12152020.csv

Notification Text:

SYST-11YIGT439

Microchip has released a new Product Documents for the PIC24FJ64GP205/GU205 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at PIC24FJ64GP205/ GU205 Family Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change: Initial release of this document; issued for Silicon Revision A0.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 15 Dec 2020

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

PIC24FJ64GP205/ GU205 Family Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

PIC24FJ64GP205-E/M4
PIC24FJ64GP205-E/PT
PIC24FJ64GP205-I/M4
PIC24FJ64GP205-I/PT
PIC24FJ64GP205T-I/M4
PIC24FJ64GP205T-I/PT
PIC24FJ64GU205-E/M4
PIC24FJ64GU205-E/PT
PIC24FJ64GU205-I/M4
PIC24FJ64GU205-I/PT
PIC24FJ64GU205T-I/M4
PIC24FJ64GU205T-I/PT

PIC24FJ64GP205/GU205 Family Silicon Errata and Data Sheet Clarification

The PIC24FJ64GP205/GU205 family devices conform functionally to the current Device Data Sheet (DS30010221**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC24FJ64GP205/GU205 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A0**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24FJ64GP205/GU205 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)
		A0
PIC24FJ64GU205	0x9A19	0x00
PIC24FJ32GU205	0x9A09	
PIC24FJ64GU203	0x9A15	
PIC24FJ32GU203	0x9A05	
PIC24FJ64GU202	0x9A11	
PIC24FJ32GU202	0x9A01	
PIC24FJ64GP205	0x9A18	
PIC24FJ32GP205	0x9A08	
PIC24FJ64GP203	0x9A14	
PIC24FJ32GP203	0x9A04	
PIC24FJ64GP202	0x9A10	
PIC24FJ32GP202	0x9A00	

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC24FJ64GP205/GU205 Family Flash Programming Specification"* (DS30010202) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				A0
I^2C	Multiple Slave Mode	1.	In applications with multiple I^2C Slaves and General Call enabled, unexpected behavior is observed in the unaddressed Slave.	X
I^2C	Slave Mode	2.	In Slave mode, an address cannot be received when the device is in Idle and the module is set for discontinue in Idle (I2CSIDL = 1).	X
I^2C	Slave Transmit	3.	Slave transmits 0xFF if the ACKDT bit is set prior to transmission.	X
UART	Break Character Transmission	4.	The Transmit Shift Register Empty (TRMT) bit is unreliable when there are back-to-back Break character transmissions.	X
Oscillator	FSCM	5.	RESET instruction in oscillator trap locks up device.	X
Flash Program Memory	Double Error Trap	6.	Using software breakpoints in the last page of program memory can lead to an ECC double error trap getting generated.	X
I/O	POR	7.	Voltage on RB10 and RB11 pins at POR.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A0**).

1. Module: I²C

In applications with multiple I²C Slaves and General Call (GCEN (I2CxCONL[7]) = 1) is enabled, unexpected behavior is observed in the unaddressed Slave when the data payload of the addressed Slave matches the general call address (00h).

When the issue occurs, unexpected data might be received in the unaddressed Slave. If Address Hold is enabled (AHEN (I2CxCONH[1]) = 1), then I²C will erroneously ACK the byte.

Work around

If Address Hold is enabled (I2CxCONH[1] = 1), Acknowledge Data (ACKDT (I2CxCONL[5]) = 1) should be set during initialization.

Instead of a Slave interrupt, poll the Receive Buffer Full Status bit and read the receive buffer to clear the unwanted data.

Affected Silicon Revisions

A0							
X							

2. Module: I²C

When I²C is in Slave mode, an address cannot be received when the device is in Idle and the module is set for discontinue in Idle (I2CSIDL = 1).

Work around

None.

Affected Silicon Revisions

A0							
X							

3. Module: I²C

When the Slave is transmitting data, if Acknowledge Data (ACKDT (I2CxCONL[5]) = 1) is set before the Slave starts transmission, then the second data transmitted will be 0xFF, irrespective of the actual data in I2CxTRN.

Work around

Clear the ACKDT bit before Slave transmission.

Affected Silicon Revisions

A0							
X							

4. Module: UART

The Transmit Shift Register Empty (TRMT) bit is unreliable when there are back-to-back Break character transmissions. For back-to-back Break characters, the TRMT bit may not reflect the actual status. If user software is polling for this bit to be set, it may result in dummy bytes getting transmitted instead of Break characters.

Work around

Poll the UARTx Transmit Break bit, UTXBRK (UxSTA[11]), to be cleared instead of the TRMT bit (UxSTA[8]) to be set. The UTXBRK status bit will be cleared after a Break character transmission.

Affected Silicon Revisions

A0							
X							

5. Module: Oscillator

When the device is clocked from the Primary Oscillator with PLL (XT+PLL, HS+PLL or EC+PLL), it may not recover from the oscillator failure (Fail-Safe Clock Monitor event) if a RESET instruction is executed in the oscillator trap. The device will lock up.

Work around

In the application code, the device should be started from FRC (defined in the Configuration bits). Then, the clock should be switched to the Primary Oscillator with PLL.

Affected Silicon Revisions

A0							
X							

6. Module: Flash Program Memory

Using software breakpoints in the last page of program memory can lead to an ECC double error trap getting generated.

Work around

Avoid using software breakpoints in the last page; use hardware breakpoints instead.

Affected Silicon Revisions

A0							
X							

7. Module: I/O

At device power-up, the RB10 and RB11 pins may drive a pulse up to 1.5V for a duration of up to 2 µs in the PIC24FJXXGUXXX devices.

Work around

It is recommended to ensure the circuitry that is connected to these pins can endure this pulse.

Example applications affected may include complementary power switches, where a transient current shoot-through might occur.

High-voltage applications with complementary switches should power the high-voltage 200 µSec later than powering the PIC® MCU to avoid the issue.

Small C-R circuitry can be used to reduce this voltage spike for GPIO operations.

Behavior is specific to each part and not affected by aging.

Affected Silicon Revisions

A0							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (30010221**C**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Electrical Characteristics

Note 3 in TABLE 30-29: A/D Module Specifications has been added as shown below in bold:

Note 3: Codes 511, 1023, 1535, 2559 and 3583 can have a DNL error of -1 LSB to < +1 LSB; code 2047 can have a DNL error of -1 LSB to < +2 LSB, and code 3071 can have a DNL error of -1 LSB to < +2.5 LSB.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (11/2020)

Initial release of this document; issued for Silicon Revision A0.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
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