



# PRODUCT/PROCESS CHANGE NOTIFICATION

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PCN IPG-PWR/14/8674  
Dated 02 Sep 2014

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**TO-247 and Max247 packages Back-End Capacity Extension  
- Nantong Fujitsu Microelectronics (China)**

**Table 1. Change Implementation Schedule**

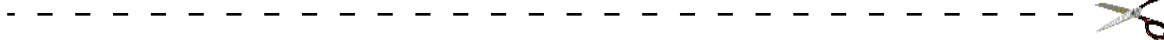
Forecasted implementation date for change	26-Aug-2014
Forecasted availability date of samples for customer	26-Aug-2014
Forecasted date for <b>STMicroelectronics</b> change Qualification Plan results availability	26-Aug-2014
Estimated date of changed product first shipment	02-Dec-2014

**Table 2. Change Identification**

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Package assembly location change, Testing location change
Reason for change	Improve service to Customers
Description of the change	Following the continuous improvement of our service and in order to increase the productivity, this document is announcing that TO-247 and Max247 products, listed in this PCN, will be also produced in Subcontractor Nantong Fujitsu Microelectronics (China). Nantong Fujitsu Microelectronics subcontractor is our preferred partner for power packages since long time. Devices used for qualification are available as samples. Max247 package will be actually produced only in Nantong Fujitsu Microelectronics (China), so for this package, this PCN is intended as Back-End Capacity relocation.
Change Product Identification	"GF" marked on the package and box label
Manufacturing Location(s)	

**Table 3. List of Attachments**

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt		PCN IPG-PWR/14/8674
Please sign and return to STMicroelectronics Sales Office		Dated 02 Sep 2014
<input type="checkbox"/> Qualification Plan Denied <input type="checkbox"/> Qualification Plan Approved  <input type="checkbox"/> Change Denied <input type="checkbox"/> Change Approved	Name:	
	Title:	
	Company:	
	Date:	
	Signature:	
Remark ..... ..... ..... ..... ..... ..... ..... ..... ..... .....		

## DOCUMENT APPROVAL

Name	Function
Mottese, Anna	Marketing Manager
Aleo, Mario-Antonio	Product Manager
Falcone, Giuseppe	Q.A. Manager

**WHAT:**

Following the continuous improvement of our service and in order to increase the productivity, this document is announcing that TO-247 and Max247™ products, listed in this PCN, will be also produced in Subcontractor Nantong Fujitsu Microelectronics (China).

Nantong Fujitsu Microelectronics subcontractor is our preferred partner for power packages since long time. Devices used for qualification are available as samples.

Max247™ package will be actually produced only in Nantong Fujitsu Microelectronics (China), so for this package, this PCN is intended as Back-End Capacity relocation.

For the complete list of the part numbers affected by these changes, please refer to the attached Products List.

**Samples** of the test vehicle are available right now upon request for immediate customer qualification, while the full availability of products will be granted from wk 35 2014 onwards. Any other sample request will be granted upon request

Product Family	Test Vehicle	Package	1 <sup>st</sup> Shipment
Power MOSFET	STW18NM60N STW43NM60ND STW88N65M5	TO-247	Wk 48
	STY145N65M5 STY60NM50 STY80NM60N	Max247™	Wk 48
Power Bipolar	TIP35C	TO-247	Wk 48
IGBT	STGY40NC60VD	Max247™	Wk 48

**WHY:**

To improve service to ST Customers and standardize manufacturing processes for the power packages typology.

**HOW:**

By adding Nantong Fujitsu Microelectronics as production site for products housed in: TO-247 and Max247™.

The changed here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant product's datasheets.

Packing and delivery quantities are the same as per STMicroelectronics STD for these packages.

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### **Qualification program and results:**

The qualification program consists mainly of comparative electrical characterization and reliability tests. Please refer to Appendix 1 for all the details.

### **WHEN:**

Production start and first shipments will occur as per the scheduling indicated in the tables below.

### **Marking and traceability:**

Unless otherwise stated by customer specific requirement, the traceability of the parts produced in Nantong Fujitsu Microelectronics will be ensured by the Q.A. number and plant code identification “GF” marked on the package, as illustrated in the below picture:

Package marking example



Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).

In any case, first shipments may start earlier with customer's written agreement.

## INTERIM Reliability Report

*TO-247 and Max247™ packages Back-End Capacity Extension - Nantong Fujitsu Microelectronics (China)*

General Information		Locations	
<b>Product Lines:</b>	M5F9 – M264 – 2F6B – MD5N – 2M6N - BA21 – IV6B+E61L – M5FR	<b>Wafer Diffusion Plants:</b>	Ang Mo Kio (Singapore) Catania (Italy)
<b>Product Families:</b>	Power MOSFET (M5F9 – M264 – 2F6B – MD5N – 2M6N – M5FR)  Power BIPOLAR (BA21)  IGBT (IV6B+E61L)	<b>EWS Plants:</b>	Ang Mo Kio (Singapore) Catania (Italy)
<b>P/Ns:</b>	STW88N65M5 (M5F9) STW18NM60N (M264) STW43NM60ND (2F6B) STY60NM50 (MD5N) STY80NM60N (2M6N) TIP35C (BA21) STGY40NC60VD (IV6B+E61L) STY145N65M5 (M5FR)	<b>Assembly plant:</b>	Nantong Fujitsu Microelectronics (China)
<b>Product Group:</b>	IPG	<b>Reliability Lab:</b>	IPG-PTD Catania Reliability Lab.
<b>Product division:</b>	Power Transistor Division		
<b>Package:</b>	TO-247 (M5F9 – M264 – 2F6B – BA21)  MAX247 (MD5N – 2M6N - IV6B + E61L)		
<b>Silicon Process techn.:</b>	MDmesh™ V Power MOSFET MDmesh™ II Power MOSFET FDmesh™ II Power MOSFET Power BIPOLAR IGBT		

### DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	August 2014	14	A. Settineri	C. Cappello	First issue: Interim results and Plan

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.  
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## **1 APPLICABLE AND REFERENCE DOCUMENTS**

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

## **2 GLOSSARY**

DUT	Device Under Test
SS	Sample Size
HF	Halogen Free

## **3 RELIABILITY EVALUATION OVERVIEW**

### **3.1 Objectives**

Capacity expansion activities of the TO-247 and Max247™ packages, graded Molding Compound manufactured in Nantong Fujitsu Microelectronics (NFME) Subcontractor factory located in China.

### **3.2 INTERIM Conclusion**

Preliminary qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

## **4 DEVICE CHARACTERISTICS**

### **4.1 Device description**

N-channel Power MOSFET.  
 Power Bipolar.  
 IGBT.

### **4.2 Construction note**

**D.U.T.: STW88N65M5      LINE: M5F9      PACKAGE: TO-247**

<b>Wafer/Die fab. Information</b>	
Wafer fab manufacturing location	Catania (Italy)
Technology	Power MOSFET MDmesh V Technology
Die finishing back side	Ti/NiV/Ag
Die size	10410 x 6810 $\mu\text{m}^2$
Metal	AlCu/Ti/TiNi
Passivation type	Nitride

<b>Wafer Testing (EWS) information</b>	
Electrical testing manufacturing location	Catania (Italy)
Test program	WPIS

<b>Assembly information</b>	
Assembly site	Nantong Fujitsu Microelectronics (China)
Package description	TO-247
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	5 mils Al/Mg Gate – Ribbon 60x8 mils Al Source
Lead finishing/bump solder material	Pure Tin

<b>Final testing information</b>	
Testing location	Nantong Fujitsu Microelectronics (China)
Tester	IPTest

**D.U.T.: STW18NM60N      LINE: M264      PACKAGE: TO-247**

<b>Wafer/Die fab. Information</b>	
Wafer fab manufacturing location	Ang Mo Kio (Singapore)
Technology	Power MOSFET MDmesh II Technology
Die finishing back side	Ti/Ni/Ag
Die size	4400 x 3200 $\mu\text{m}^2$
Metal	Al/Si
Passivation type	Nitride

<b>Wafer Testing (EWS) information</b>	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

<b>Assembly information</b>	
Assembly site	Nantong Fujitsu Microelectronics (China)
Package description	TO-247
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	5 mils Al/Mg Gate – 10 mils Al Source
Lead finishing/bump solder material	Pure Tin

<b>Final testing information</b>	
Testing location	Nantong Fujitsu Microelectronics (China)
Tester	IPTest

**D.U.T.: STW43NM60ND      LINE: 2F6B      PACKAGE: TO-247**

<b>Wafer/Die fab. Information</b>	
Wafer fab manufacturing location	Catania (Italy)
Technology	Power MOSFET MDmesh II Technology
Die finishing back side	Ti/Ni/Ag
Die size	8800 x 5760 $\mu\text{m}^2$
Metal	Al/Si
Passivation type	Nitride

<b>Wafer Testing (EWS) information</b>	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

<b>Assembly information</b>	
Assembly site	Nantong Fujitsu Microelectronics (China)
Package description	TO-247
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	5 mils Al/Mg Gate – Ribbon 40x 6 mils Al Source
Lead finishing/bump solder material	Pure Tin

<b>Final testing information</b>	
Testing location	Nantong Fujitsu Microelectronics (China)
Tester	IPTest

**D.U.T.: TIP35C**
**LINE: BA21**
**PACKAGE: TO-247**

<b>Wafer/Die fab. Information</b>	
Wafer fab manufacturing location	Ang Mo Kio (Singapore)
Technology	Power Bipolar
Die finishing back side	Ti/Ni/Ag
Die size	4030 x 3680 $\mu\text{m}^2$
Metal	Al/Si
Passivation type	PSG

<b>Wafer Testing (EWS) information</b>	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

<b>Assembly information</b>	
Assembly site	Nantong Fujitsu Microelectronics (China)
Package description	TO-247
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	7 mils Al Base – 15 mils Al Emitter
Lead finishing/bump solder material	Pure Tin

<b>Final testing information</b>	
Testing location	Nantong Fujitsu Microelectronics (China)
Tester	IPTest

**D.U.T.: STY60NM50    LINE: MD5N    PACKAGE: Max247™**

<b>Wafer/Die fab. Information</b>	
Wafer fab manufacturing location	Ang Mo Kio (Singapore)
Technology	Power MOSFET MDmesh II Technology
Die finishing back side	Ti/Ni/Ag
Die size	9610 x 12640 $\mu\text{m}^2$
Metal	Al/Si
Passivation type	Nitride

<b>Wafer Testing (EWS) information</b>	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

<b>Assembly information</b>	
Assembly site	Nantong Fujitsu Microelectronics (China)
Package description	Max247™
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	5 mils Al/Mg Gate – 15 mils Al Source
Lead finishing/bump solder material	Pure Tin

<b>Final testing information</b>	
Testing location	Nantong Fujitsu Microelectronics (China)
Tester	IPTest

**D.U.T.: STGY40NC60VD    LINE: IV6B + E61L(Diode)    PACKAGE: Max247™**

<b>Wafer/Die fab. Information</b>	
Wafer fab manufacturing location	Ang Mo Kio (Singapore)
Technology	Irradiated IGBT
Die finishing back side	Cr/Ni/Ag
Die size	6670 x 7610 $\mu\text{m}^2$
Metal	Al/Si
Passivation type	Nitride

<b>Wafer Testing (EWS) information</b>	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

<b>Assembly information</b>	
Assembly site	Nantong Fujitsu Microelectronics (China)
Package description	TO-247
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	5 mils Al/Mg Gate – 15 mils Al Source
Lead finishing/bump solder material	Pure Tin

<b>Final testing information</b>	
Testing location	Nantong Fujitsu Microelectronics (China)
Tester	IPTest

**D.U.T.: STY80NM60N**
**LINE: 2M6N**
**PACKAGE: Max247™**

<b>Wafer/Die fab. Information</b>	
Wafer fab manufacturing location	Catania (Italy)
Technology	Power MOSFET MDmesh II Technology
Die finishing back side	Ti/Ni/Ag
Die size	9640 x 12780 $\mu\text{m}^2$
Metal	Al/Si
Passivation type	Nitride

<b>Wafer Testing (EWS) information</b>	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

<b>Assembly information</b>	
Assembly site	Nantong Fujitsu Microelectronics (China)
Package description	Max247™
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	5 mils Al/Mg Gate – Ribbon 80x10 mils Al Source
Lead finishing/bump solder material	Pure Tin

<b>Final testing information</b>	
Testing location	Nantong Fujitsu Microelectronics (China)
Tester	IPTest



**D.U.T.: STY145N65M5      LINE: M5FR      PACKAGE: Max247™**

<b>Wafer/Die fab. Information</b>	
Wafer fab manufacturing location	Catania (Italy)
Technology	Power MOSFET MDmesh V Technology
Die finishing back side	Ti/Ni/Ag
Die size	10180 x 13770 $\mu\text{m}^2$
Metal	AlCu/Ti/TiNi
Passivation type	Nitride

<b>Wafer Testing (EWS) information</b>	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

<b>Assembly information</b>	
Assembly site	Nantong Fujitsu Microelectronics (China)
Package description	Max247™
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	5 mils Al/Mg Gate – 15 mils Al Source
Lead finishing/bump solder material	Pure Tin

<b>Final testing information</b>	
Testing location	Nantong Fujitsu Microelectronics (China)
Tester	IPTest

## 5 TESTS RESULTS SUMMARY

### 5.1 Test vehicle

Lot #	Process/ Package	Product Line	Package	Comments
1	STW88N65M5	M5F9	TO-247	Power MOSFET
2	STW18NM60N	M264		Power MOSFET
3	STW43NM60ND	2F6B		Power MOSFET
4	TIP35C	BA21		Power BIPOLAR
5	STY60NM50	MD5N	Max247™	Power MOSFET
6	STGY40NC60VD	IV6B + E61L(Diode)		IGBT + Diode
7	STY80NM60N	2M6N		Power MOSFET
8	STY145N65M5	M5FR		Power MOSFET

### 5.2 Reliability test plan summary: INTERIM Results and Plan

Lot. 1 - D.U.T.: STW88N65M5	LINE: M5F9	PACKAGE: TO-247
Lot. 2 - D.U.T.: STW18NM60N	LINE: M264	PACKAGE: TO-247
Lot. 3 - D.U.T.: STW43NM60ND	LINE: 2F6B	PACKAGE: TO-247
Lot. 4 - D.U.T.: TIP35C	LINE: BA21	PACKAGE: TO-247

Test	Std ref.	Conditions	SS	Steps	Failure/SS				
					Lot 1	Lot 2	Lot 3	Lot 4	
<b>Die Oriented Tests</b>									
HTRB	JESD22 A-108	T.A.=150°C Vdss=520V (M5F9) Vdss=480V (M264) Vdss=480V (2F6B) Vdss=80V (BA21)	45	168 H	0/45	0/45	0/45	0/45	
				500 H	0/45	0/45	0/45	0/45	
				1000 H	<i>Wk36</i>	<i>Wk36</i>	<i>Wk36</i>	<i>Wk36</i>	
HTGB	JESD22 A-108	TA = 150°C Vgss= 30V	45	168 H	0/45	0/45	0/45	Not applicable	
				500 H	0/45	0/45	0/45		
				1000 H	<i>Wk36</i>	<i>Wk36</i>	<i>Wk36</i>		
HTSL	JESD22 A-103	TA = 150°C	45	168 H	0/45	0/45	0/45	0/45	
				500 H	0/45	0/45	0/45	0/45	
				1000 H	<i>Wk36</i>	<i>Wk36</i>	<i>Wk36</i>	<i>Wk36</i>	
<b>Package Oriented Tests</b>									
H3TRB	JESD22 A-101	Ta=85°C Rh=85%, Vdss=100V	25	168 H	0/25	0/25	0/25	0/25	
				500 H	0/25	0/25	0/25	0/25	
				1000 H	<i>Wk36</i>	<i>Wk36</i>	<i>Wk36</i>	<i>Wk36</i>	
TC	JESD22 A-104	TA=-65°C TO 150°C (1 HOUR/CYCLE)	25	100 cy	0/25	0/25	0/25	0/25	
				300 cy	0/25	0/25	0/25	0/25	
				500 cy	<i>Wk36</i>	<i>Wk36</i>	<i>Wk36</i>	<i>Wk36</i>	
TF/IOL	Mil-STD 750D Method 1037	ΔTc=+105°C	25	5K cy	0/25	0/25	0/25	0/25	
				10K cy	0/25	0/25	0/25	0/25	
AC	JESD22 A-102	TA=121°C – PA=2 ATM	25	96 H	<i>running</i>	<i>running</i>	<i>running</i>	<i>running</i>	

Lot. 5 - D.U.T.: STY60NM50

LINE: MD5N

PACKAGE: Max247™

Lot. 6 - D.U.T.: STGY40NC60VD

LINE: IV6B + E61L

PACKAGE: Max247™

Lot. 7 - D.U.T.: STY80NM60N

LINE: 2M6N

PACKAGE: Max247™

Lot. 8 - D.U.T.: STY145N65M5

LINE: M5FR

PACKAGE: Max247™

Test	Std ref.	Conditions	SS	Steps	Failure/SS			
					Lot 5	Lot 6	Lot 7	Lot 8
<b>Die Oriented Tests</b>								
HTRB	JESD22 A-108	T.A.=150°C Vdss=400V (MD5N) Vdss=480V (IV6B) Vdss=480V (2M6N) Vdss=480V (M5FR)	45	168 H	0/45		0/45	0/45
				500 H	0/45		0/45	0/45
				1000 H	<i>Wk36</i>	<i>Wk36</i>	<i>Wk36</i>	<i>Wk36</i>
HTGB	JESD22 A-108	TA = 150°C Vgss= 30V	45	168 H	0/45	0/45	0/45	0/45
				500 H	0/45	0/45	0/45	0/45
				1000 H	<i>Wk36</i>	<i>Wk36</i>	<i>Wk36</i>	<i>Wk36</i>
HTSL	JESD22 A-103	TA = 150°C	45	168 H	0/45	0/45	0/45	0/45
				500 H	0/45	0/45	0/45	0/45
				1000 H	<i>Wk36</i>	<i>Wk36</i>	<i>Wk36</i>	<i>Wk36</i>
<b>Package Oriented Tests</b>								
H3TRB	JESD22 A-101	Ta=85°C Rh=85%, Vdss=100V	25	168 H	0/25	0/25	0/25	0/25
				500 H	0/25	0/25	0/25	0/25
				1000 H	<i>Wk36</i>	<i>Wk36</i>	<i>Wk36</i>	<i>Wk36</i>
TC	JESD22 A-104	TA=-65°C TO 150°C (1 HOUR/CYCLE)	25	100 cy	0/25	0/25	0/25	0/25
				300 cy	0/25	0/25	0/25	0/25
				500 cy	<i>Wk36</i>	<i>Wk36</i>	<i>Wk36</i>	<i>Wk36</i>
TF/IOL	Mil-STD 750D Method 1037	ΔTc=+105°C	25	5K cy	0/25	0/25	0/25	0/25
				10K cy	0/25	0/25	0/25	0/25
AC	JESD22 A-102	TA=121°C – PA=2 ATM	25	96 H	0/25	0/25	0/25	0/25

## 6 ANNEXES 6.0

### 6.1 Tests Description

Test name	Description	Purpose
<b>Die Oriented Tests</b>		
<b>HTRB</b> High Temperature Reverse Bias  <b>HTGB</b> High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: <ul style="list-style-type: none"> <li>• low power dissipation;</li> <li>• max. supply voltage compatible with diffusion process and internal circuitry limitations;</li> </ul>	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way.  To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
<b>HTSL</b> High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
<b>Package Oriented Tests</b>		
<b>AC</b> Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
<b>TC</b> Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
<b>TF / IOL</b> Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
<b>H3TRB</b> Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

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