



PRODUCT INFORMATION LETTER

PIL MMS-MIC/13/7803
Dated 26 Apr 2013

**Addendum PIL7759 - New die revision for STM32F10x
(128K, 512K) products**

Sales Type/product family label	STM32F10x (128K, 512K) products listed below
Type of change	Product design change
Reason for change	Yield improvement
Description	The yield will be improved thanks to minor design changes and mask optimization, leading to better service for our customers. More details concerning the change are indicated in the document.
Forecasted date of implementation	14-Aug-2013
Forecasted date of samples for customer	03-Jul-2013
Forecasted date for STMicroelectronics change Qualification Plan results availability	03-Jun-2013
Involved ST facilities	TSMC Taiwan fab 3 and TSMC USA fab 11

DOCUMENT APPROVAL

Name	Function
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PRODUCT INFORMATION LETTER

Addendum PIL7759 - New die revision for STM32F10x (128K, 512K) products

MMS - Microcontrollers Division (MCD)

Dear Customer,

In order to sustain the strong demand on STM32F10x (128K, 512K) products and to provide a better service to our customers, ST MCD division is working continuously to improve yield in production. For this reason, a new die revision is being introduced.

This has already been notified in the PIL 7759 "New die revision for STM32F10x (128K, 512K) products" that remains valid.

The purpose of this addendum is to give complementary information about the improvement that has been performed.

Why the change?

The main yield detractors are linked to the Flash.

ST strongly recommends switching to this new silicon to benefit from the quality improvement. This new revision guarantees supply in line with industry standards thanks to more predictable yield.

What is the change?

The yield will be improved thanks to minor design changes and mask optimization, leading to better service for our customers.

Silicon revisions change as indicated below:

Fab diffusion	Previous silicon revision	New silicon revision
TSMC Taiwan fab 3	Y	X
TSMC USA fab 11	1	2

Programming current:

Thanks to the continuous review of our processes, we analyzed a variation of the internal programming current from device to device. This current is internally controlled by STM32 design.

Some parts have a lower programming current than others and thus fail our testing conditions.

The change allows the programming current to be increased in order to improve the behavior during testing and therefore the yield. Change only activates a metal option already available by design and implemented with single metal mask modification.

Depending on the product, this change can be either managed by software adjustment of internal registers during the test or by a metal option. For this STM32 product family, programming current is adjustable by metal option.

It does not have any impact on the electrical parameters specified in the datasheet.

Devices delivered before and after the change are following exactly the same test flow. Full compliance with the product datasheet is maintained.

Mask optimization:

Some steps previously done in 2 stages are now optimized by merging them into a single step. This leads to improve cycle time.

None of the above changes is expected to affect fit, form and function or reliability of the device.

Nevertheless, we performed some assessments on the impact of the changes:

- Preliminary electrical characterization does not show any regression of performance (final results will be provided as indicated above in June 2013),
- Yield assessment confirms the expected improvement with a 5 000 ppm recovery observed on several batches,
- Preliminary reliability trials show positive results (final results will be provided as indicated above in June 2013).

The risk assessment confirms: no impact on form, fit, function, quality or reliability of the product.

What is the impact of the change?

- **Form:** no change
- **Fit:** no change
- **Function:** no change

Why a PIL?

According to JEDEC Standard JESD-46 major changes must be communicated by PCN. Major changes are defined as follows:

“A major change is a change that may affect the form, fit, or function of the product or adversely affect the quality or reliability of the product.”

In addition to JEDEC requirements, ST may notify customers about some minor changes through Product Information Letter (PIL).

When?

As indicated in PIL 7759, the production with the new die revision will start **week 33 2013**.

How will the change be qualified?

This change will be qualified using the standard STMicroelectronics Corporate Procedures for Quality and Reliability, in full compliancy with the JESD-47 international standard. You can find the qualification plan below.

How can the change be seen?

Traceability of the change can be seen with the die revision character marked on the package.

We remain available to discuss any concern you may have regarding this product information.

With our sincere regards.

Michel Buffa

Microcontrollers division General Manager

Commercial Products impacted

STM32F100RCT6	STM32F103C8T7	STM32F103VCH6
STM32F100RCT6TR	STM32F103CBT6	STM32F103VCT6
STM32F100VCT6	STM32F103CBT6TR	STM32F103VCT6TR
STM32F100VDT6	STM32F103CBT7	STM32F103VDH6
STM32F100VET6	STM32F103CBT7TR	STM32F103VDH6TR
STM32F101C8GAL	STM32F103CBU6	STM32F103VDT6
STM32F101C8T6	STM32F103EDIE1	STM32F103VDT6TR
STM32F101C8T6TR	STM32F103R8H6	STM32F103VDT7
STM32F101C8U6	STM32F103R8H7	STM32F103VEH6
STM32F101C8U6TR	STM32F103R8T6	STM32F103VEH7
STM32F101CBT6	STM32F103R8T6TR	STM32F103VET6
STM32F101CBT6TR	STM32F103R8T7	STM32F103VET6TR
STM32F101CBU6	STM32F103RBH6	STM32F103VET7
STM32F101R8T6	STM32F103RBH7	STM32F103VET7TR
STM32F101R8T6TR	STM32F103RBT6	STM32F103ZCCINTR
STM32F101RBH6	STM32F103RBT6TR	STM32F103ZCH6
STM32F101RBT6	STM32F103RBT7	STM32F103ZCT6
STM32F101RBT6TR	STM32F103RBT7TR	STM32F103ZCT7
STM32F101RCT6	STM32F103RCACETR	STM32F103ZDH6
STM32F101RCT6TR	STM32F103RCDELTR	STM32F103ZDT6
STM32F101RDT6	STM32F103RCT6	STM32F103ZEH6
STM32F101RDT6TR	STM32F103RCT6TR	STM32F103ZEH6TR
STM32F101RDWOWTR	STM32F103RCT7	STM32F103ZEH7
STM32F101RET6	STM32F103RCUVWTR	STM32F103ZET6
STM32F101T8U6	STM32F103RCY6CTR	STM32F103ZET6TR
STM32F101T8U6TR	STM32F103RCY6TR	STM32F103ZET7
STM32F101TBU6	STM32F103RDT6	STM32P101C8MBHTR
STM32F101V8T6	STM32F103RDT6TR	STM32P101C8MBKTR
STM32F101V8T6TR	STM32F103RDY6TR	STM32P101CBMBD
STM32F101VBT6	STM32F103RET6	STM32P102C8MAPTR
STM32F101VBT6TR	STM32F103RET6TR	STM32P103C8MBCTR
STM32F101VCT6	STM32F103RET7	STM32P103CBMAZTR
STM32F101VCT6TR	STM32F103REY6TR	STM32P103CBSAMTR
STM32F101VDT6	STM32F103T8U6	STM32P103RBDDELTR
STM32F101VDT6TR	STM32F103T8U6TR	STM32P103RDMBITR
STM32F101VET6	STM32F103T8U7	STM32P103T8ABC
STM32F101ZCT6	STM32F103T8U7TR	STM32P103ZEMBL
STM32F101ZDT6	STM32F103TBU6	STM32P103ZEMBLTR
STM32F101ZET6	STM32F103TBU7	STM32P103ZEXFI
STM32F102C8T6	STM32F103V8H6	
STM32F102C8T6TR	STM32F103V8T6	
STM32F102CBT6	STM32F103V8T6TR	
STM32F102CBT6TR	STM32F103VBH6	
STM32F102R8T6	STM32F103VBH7	
STM32F102RBT6	STM32F103VBI6	
STM32F102RBT6TR	STM32F103VBT6	
STM32F102RCT6	STM32F103VBT6TR	
STM32F102T8U6TR	STM32F103VBT7	
STM32F103BDIE1	STM32F103VBT7TR	
STM32F103C8T6	STM32F103VBXFI	
STM32F103C8T6TR	STM32F103VCH6	



RELIABILITY PLAN

Qualification items :

New Die revision for STM32F10x, STM32P10x products

Diffusion Plant:

TSMC waferfab 3 & 11

Devices:

STM32F10x / STM32P10x

Issued on:

Mar 12, 2013

**Purpose**

- ✓ Qualification of the new revision X for waferfab3 (Taiwan) and revision 2 for waferfab11 (USA) for products STM32F10x & STM32P10x

Test Vehicles :

Device : **Die 410 / LQFP100**
Die 414 / LQFP100

These new revision aim to increase the yield through process optimization and design changes.

Based on these changes according to our “Reliability tests and criteria for qualifications” specification (ADCS 0061692), the following reliability strategy is:

- 2 qualification lots on the product drivers : die 410 & die 414 used for reliability trials described in below table :

Reliability Trial		Test Conditions	Pass Criteria	Unit per Lot	Lot nb
EDR	Memory cycling endurance & Retention	10Kcycles at 125°C + 672hrs bake 175°C	No reject	77	1 (410) 1 (414)
	JESD22-A117				
EDR	Memory cycling endurance & Retention	10Kcycles at 25°C + 72hrs bake 175°C	No reject	77	1 (410) 1 (414)
	JESD22-A117				
EDR	Memory cycling endurance & Retention	10Kcycles at -40°C + 72hrs bake 175°C	No reject	77	1 (410) 1 (414)
	JESD22-A117				
ESD	ESD Human Body Model	2KV (except Vbat 1KV)	2KV	3	1 (410) 1 (414)
	AEC-Q100-002				
ESD	ESD Charge Device Model	750V corners 500V all other pins	750V / 500V	3	1 (410) 1 (414)
	JESD22-C101				
LU	Latch Up	125°C	no LU	6	1 (410) 1 (414)
	EIA/JESD78				

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