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Operational Amplifier, Rail-to-Rail Output, 3 MHz BW

TLV271, TLV272, NCV272, TLV274, NCV274

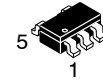
The TLV/NCV27x operational amplifiers provide rail-to-rail output operation. The output can swing within 320 mV to the positive rail and 50 mV to the negative rail. This rail-to-rail operation enables the user to make optimal use of the entire supply voltage range while taking advantage of 3 MHz bandwidth. The opamp can operate on supply voltage as low as 2.7 V over the temperature range of -40°C to 125°C. The high bandwidth provides a slew rate of 2.4 V/μs while only consuming 550 μA of quiescent current. Likewise the opamp can run on a supply voltage as high as 16 V (single) and 36 V (dual quad) making it ideal for a broad range of battery-operated applications. Since this is a CMOS device it has high input impedance and low bias currents making it ideal for interfacing to a wide variety of signal sensors. In addition it comes in a variety of compact packages with different pinout styles allowing for use in high-density PCB's.

Features

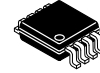
- Rail-To-Rail Output
- Wide Bandwidth: 3 MHz
- High Slew Rate: 2.4 V/μs
- Wide Power-Supply Range: 2.7 V to 16 V (TLV271), 36 V (TLV/NCV272/274)
- Low Supply Current: 550 μA
- Low Input Bias Current: 45 pA
- Wide Temperature Range: -40°C to 125°C
- TSOP-5, Micro-8, SOIC-8, SOIC-14, TSSOP-14 Packages
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Notebook Computers
- Portable Instruments
- Signal Conditioning
- Automotive
- Power Supplies
- Current Sensing



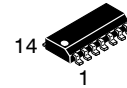
TSOP-5
 CASE 483



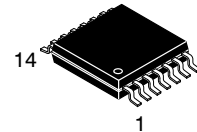
Micro8
 CASE 846A



SOIC-8
 CASE 751



SOIC-14 NB
 CASE 751A



TSSOP-14
 CASE 948G

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 2 of this data sheet.

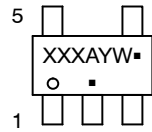
ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

TLV271, TLV272, NCV272, TLV274, NCV274

MARKING DIAGRAMS

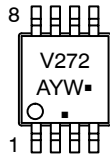
Single Channel Configuration TLV271



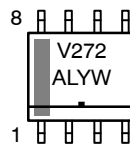
**TSOP-5
CASE 483**

XXX = ADG (TLV271SN1T1G)
 = ADH (TLV271SN2T1G)
 A = Assembly Location
 Y = Year
 W = Work Week
 ■ = Pb-Free Package
 (Note: Microdot may be in either location)

Dual Channel Configuration TLV272, NCV272

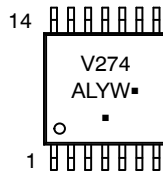


**Micro8
CASE 846A**

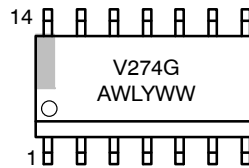


**SOIC-8
CASE 751**

Quad Channel Configuration TLV274, NCV274



**TSSOP-14
CASE 948G**



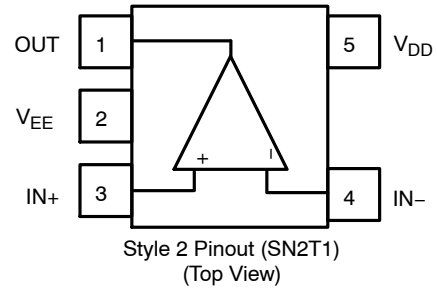
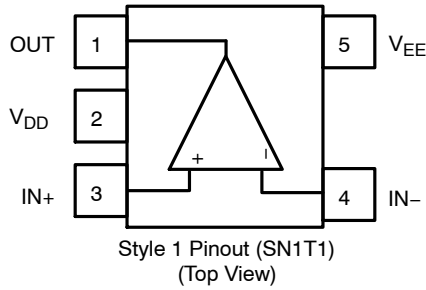
**SOIC-14 NB
CASE 751A**

XXXXX = Specific Device Code
 A = Assembly Location
 WL, L = Wafer Lot
 Y = Year
 WW, W = Work Week
 G or ■ = Pb-Free Package
 (Note: Microdot may be in either location)

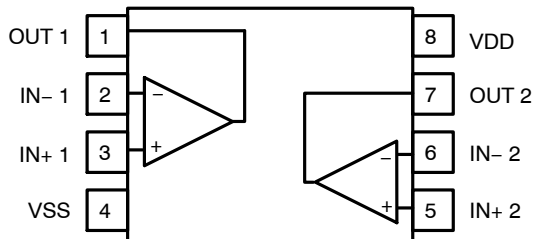
TLV271, TLV272, NCV272, TLV274, NCV274

PIN CONNECTIONS

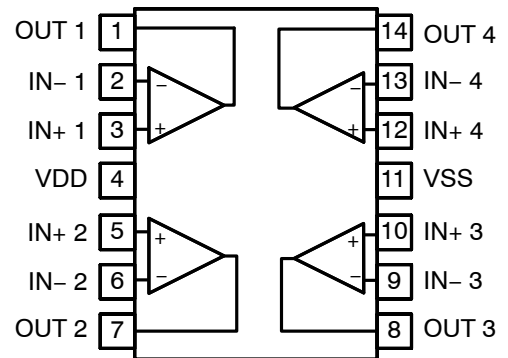
Single Channel Configuration TLV271



Dual Channel Configuration TLV272, NCV272



Quadruple Channel Configuration TLV274, NCV274



ORDERING INFORMATION

| Device | Configuration | Automotive | Marking | Package | Shipping† | |
|----------------------------------|---------------|------------|---------|----------------|----------------------|----------------------|
| TLV271SN1T1G (Style 1 Pinout) | Single | No | ADG | TSOP-5 | 3000 / Tape and Reel | |
| TLV271SN2T1G (Style 2 Pinout) | | | ADH | | 3000 / Tape and Reel | |
| TLV272DR2G | Dual | | V272 | SOIC-8 | 2500 / Tape and Reel | |
| TLV272DMR2G | | | V272 | Micro-8/MSOP-8 | 4000 / Tape and Reel | |
| TLV274DR2G | Quad | | V274 | SOIC-14 | 2500 / Tape and Reel | |
| TLV274DTBR2G | | | V274 | TSSOP-14 | 2500 / Tape and Reel | |
| NCV272DR2G* | Dual | | Yes | V272 | SOIC-8 | 2500 / Tape and Reel |
| NCV272DMR2G* | | | | V272 | Micro-8/MSOP-8 | 4000 / Tape and Reel |
| NCV274DR2G* | Quad | V274 | | SOIC-14 | 2500 / Tape and Reel | |
| NCV274DTBR2G* | | V274 | | TSSOP-14 | 2500 / Tape and Reel | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

TLV271, TLV272, NCV272, TLV274, NCV274

MAXIMUM RATINGS

| Symbol | Rating | Value | Unit |
|--------------------|--------------------------------------------------------|-------------------------------------|------|
| V _{DD} | Supply Voltage (Note 1) | TLV271 | 16.5 |
| | | TLV/NCV272/274 | 36 |
| V _{ID} | Input Differential Voltage | ± Supply Voltage | V |
| V _I | Input Common Mode Voltage Range (Note 1) | -0.2 V to (V _{DD} + 0.2 V) | V |
| I _I | Maximum Input Current | ± 10 | mA |
| I _O | Output Current Range | ± 100 | mA |
| | Continuous Total Power Dissipation (Note 1) | 200 | mW |
| T _J | Maximum Junction Temperature | 150 | °C |
| T _A | Operating Ambient Temperature Range (free-air) | -40 to 125 | °C |
| T _{STG} | Storage Temperature Range | -65 to 150 | °C |
| ESD _{HBM} | ESD Capability, Human Body Model | 2 | kV |
| ESD _{CDM} | ESD Capability, Charged Device Model | TLV271 | TBD |
| | | TLV/NCV272 | 2 |
| | | TLV/NCV274 | 1 |
| | Mounting Temperature (Infrared or Convection – 20 sec) | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Continuous short-circuit operation to ground at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45 mA over long term may adversely affect reliability. Shorting output to either V+ or V- will adversely affect reliability.

THERMAL INFORMATION

| Parameter | Symbol | Package | Single Layer Board (Note 2) | Multi-Layer Board (Note 3) | Unit |
|---------------------|-----------------|------------------|-----------------------------|----------------------------|------|
| Junction-to-Ambient | θ _{JA} | TSOP-5 | 333 | 195 | °C/W |
| | | Micro-8 / MSOP-8 | 236 | 167 | |
| | | SOIC-8 | 190 | 131 | |
| | | SOIC-14 | 142 | 101 | |
| | | TSSOP-14 | 179 | 128 | |

2. Values based on a 1S standard PCB according to JEDEC51-3 with 1.0 oz copper and a 300 mm² copper area

3. Values based on a 1S2P standard PCB according to JEDEC51-7 with 1.0 oz copper and a 100 mm² copper area

TLV271, TLV272, NCV272, TLV274, NCV274

TLV271 DC ELECTRICAL CHARACTERISTICS

($V_{DD} = 2.7V, 3.3V, 5V$ & $\pm 5V$ (Note 4), $T_A = 25^\circ C$, $R_L \geq 10 k\Omega$ unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit | |
|---------------------------------------|------------|------------------------------------------------------------------------|---------------------|------|-----|------------------|----|
| Input Offset Voltage | V_{IO} | $V_{IC} = V_{DD}/2, V_O = V_{DD}/2, R_L = 10 k\Omega, R_S = 50 \Omega$ | | 0.5 | 5 | mV | |
| | | $T_A = -40^\circ C$ to $+105^\circ C$ | | | 7 | | |
| Offset Voltage Drift | ICV_{OS} | $V_{IC} = V_{DD}/2, V_O = V_{DD}/2, R_L = 10 k\Omega, R_S = 50 \Omega$ | | 2 | | $\mu V/^\circ C$ | |
| Common Mode Rejection Ratio | CMRR | $0 V \leq V_{IC} \leq V_{DD} - 1.35 V, R_S = 50 \Omega$ | $V_{DD} = 2.7 V$ | 58 | 70 | dB | |
| | | $T_A = -40^\circ C$ to $+105^\circ C$ | | 55 | | | |
| | | $0 V \leq V_{IC} \leq V_{DD} - 1.35 V, R_S = 50 \Omega$ | $V_{DD} = 5 V$ | 65 | 130 | | |
| | | $T_A = -40^\circ C$ to $+105^\circ C$ | | 62 | | | |
| | | $0 V \leq V_{IC} \leq V_{DD} - 1.35 V, R_S = 50 \Omega$ | $V_{DD} = \pm 5 V$ | 69 | 140 | | |
| $T_A = -40^\circ C$ to $+105^\circ C$ | 66 | | | | | | |
| Power Supply Rejection Ratio | PSRR | $V_{DD} = 2.7 V$ to $16 V, V_{IC} = V_{DD}/2, \text{No Load}$ | | 70 | 135 | dB | |
| | | $T_A = -40^\circ C$ to $+105^\circ C$ | | 65 | | | |
| Large Signal Voltage Gain | A_{VD} | $V_{O(pp)} = V_{DD}/2, R_L = 10 k\Omega$ | $V_{DD} = 2.7 V$ | 97 | 106 | dB | |
| | | $T_A = -40^\circ C$ to $+105^\circ C$ | | 76 | | | |
| | | $V_{O(pp)} = V_{DD}/2, R_L = 10 k\Omega$ | $V_{DD} = 3.3 V$ | 97 | 123 | | |
| | | $T_A = -40^\circ C$ to $+105^\circ C$ | | 76 | | | |
| | | $V_{O(pp)} = V_{DD}/2, R_L = 10 k\Omega$ | $V_{DD} = 5 V$ | 100 | 127 | | |
| | | $T_A = -40^\circ C$ to $+105^\circ C$ | | 86 | | | |
| | | $V_{O(pp)} = V_{DD}/2, R_L = 10 k\Omega$ | $V_{DD} = \pm 5 V$ | 100 | 130 | | |
| $T_A = -40^\circ C$ to $+105^\circ C$ | 90 | | | | | | |
| Input Bias Current | I_B | $V_{DD} = 5 V, V_{IC} = V_{DD}/2, V_O = V_{DD}/2, R_S = 50 \Omega$ | $T_A = 25^\circ C$ | | 45 | 150 | pA |
| | | | $T_A = 105^\circ C$ | | | 1000 | |
| Input Offset Current | I_{IO} | $V_{DD} = 5 V, V_{IC} = V_{DD}/2, V_O = V_{DD}/2, R_S = 50 \Omega$ | $T_A = 25^\circ C$ | | 45 | 150 | pA |
| | | | $T_A = 105^\circ C$ | | | 1000 | |
| Differential Input Resistance | $r_{i(d)}$ | | | 1000 | | G Ω | |
| Common-mode Input Capacitance | C_{IC} | $f = 21 \text{ kHz}$ | | 8 | | pF | |

4. $V_{DD} = \pm 5 V$ is shorthand for $V_{DD} = +5 V$ and $V_{EE} = -5 V$.

TLV271, TLV272, NCV272, TLV274, NCV274

TLV271 DC ELECTRICAL CHARACTERISTICS

($V_{DD} = 2.7V, 3.3V, 5V$ & $\pm 5V$ (Note 4), $T_A = 25^\circ C$, $R_L \geq 10\text{ k}\Omega$ unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit | | |
|--------------------------------------------|---------------------------|---------------------------------------------------------|---------------------------|------|------|------|---|---|
| Output Swing (High-level) | V_{OH} | $V_{IC} = V_{DD}/2, I_{OH} = -1\text{ mA}$ | $V_{DD} = 2.7\text{ V}$ | 2.55 | 2.58 | | V | |
| | | $T_A = -40^\circ C$ to $+105^\circ C$ | | 2.48 | | | | |
| | | $V_{IC} = V_{DD}/2, I_{OH} = -1\text{ mA}$ | $V_{DD} = 3.3\text{ V}$ | 3.15 | 3.21 | | | |
| | | $T_A = -40^\circ C$ to $+105^\circ C$ | | 3.00 | | | | |
| | | $V_{IC} = V_{DD}/2, I_{OH} = -1\text{ mA}$ | $V_{DD} = 5\text{ V}$ | 4.8 | 4.93 | | | |
| | | $T_A = -40^\circ C$ to $+105^\circ C$ | | 4.75 | | | | |
| | | $V_{IC} = V_{DD}/2, I_{OH} = -1\text{ mA}$ | $V_{DD} = \pm 5\text{ V}$ | 4.92 | 4.96 | | | |
| | | $T_A = -40^\circ C$ to $+105^\circ C$ | | 4.9 | | | | |
| | | $V_{IC} = V_{DD}/2, I_{OH} = -5\text{ mA}$ | $V_{DD} = 2.7\text{ V}$ | 1.9 | 2.1 | | | V |
| | | $T_A = -40^\circ C$ to $+105^\circ C$ | | 1.5 | | | | |
| | | $V_{IC} = V_{DD}/2, I_{OH} = -5\text{ mA}$ | $V_{DD} = 3.3\text{ V}$ | 2.5 | 2.89 | | | |
| | | $T_A = -40^\circ C$ to $+105^\circ C$ | | 2.1 | | | | |
| | | $V_{IC} = V_{DD}/2, I_{OH} = -5\text{ mA}$ | $V_{DD} = 5\text{ V}$ | 4.5 | 4.68 | | | |
| | | $T_A = -40^\circ C$ to $+105^\circ C$ | | 4.35 | | | | |
| $V_{IC} = V_{DD}/2, I_{OH} = -5\text{ mA}$ | $V_{DD} = \pm 5\text{ V}$ | 4.7 | 4.78 | | | | | |
| $T_A = -40^\circ C$ to $+105^\circ C$ | | 4.65 | | | | | | |
| Output Swing (Low-level) | V_{OL} | $V_{IC} = V_{DD}/2, I_{OL} = -1\text{ mA}$ | $V_{DD} = 2.7\text{ V}$ | | 0.1 | 0.15 | V | |
| | | $T_A = -40^\circ C$ to $+105^\circ C$ | | | | 0.22 | | |
| | | $V_{IC} = V_{DD}/2, I_{OL} = -1\text{ mA}$ | $V_{DD} = 3.3\text{ V}$ | | 0.03 | 0.15 | | |
| | | $T_A = -40^\circ C$ to $+105^\circ C$ | | | | 0.22 | | |
| | | $V_{IC} = V_{DD}/2, I_{OL} = -1\text{ mA}$ | $V_{DD} = 5\text{ V}$ | | 0.03 | 0.1 | | |
| | | $T_A = -40^\circ C$ to $+105^\circ C$ | | | | 0.15 | | |
| | | $V_{IC} = V_{DD}/2, I_{OL} = -1\text{ mA}$ | $V_{DD} = \pm 5\text{ V}$ | | 0.05 | 0.08 | | |
| | | $T_A = -40^\circ C$ to $+105^\circ C$ | | | | 0.1 | | |
| | | $V_{IC} = V_{DD}/2, I_{OL} = -5\text{ mA}$ | $V_{DD} = 2.7\text{ V}$ | | 0.5 | 0.7 | | V |
| | | $T_A = -40^\circ C$ to $+105^\circ C$ | | | | 1.1 | | |
| | | $V_{IC} = V_{DD}/2, I_{OL} = -5\text{ mA}$ | $V_{DD} = 3.3\text{ V}$ | | 0.13 | 0.7 | | |
| | | $T_A = -40^\circ C$ to $+105^\circ C$ | | | | 1.1 | | |
| | | $V_{IC} = V_{DD}/2, I_{OL} = -5\text{ mA}$ | $V_{DD} = 5\text{ V}$ | | 0.13 | 0.4 | | |
| | | $T_A = -40^\circ C$ to $+105^\circ C$ | | | | 0.5 | | |
| $V_{IC} = V_{DD}/2, I_{OL} = -5\text{ mA}$ | $V_{DD} = \pm 5\text{ V}$ | | 0.16 | 0.3 | | | | |
| $T_A = -40^\circ C$ to $+105^\circ C$ | | | | 0.35 | | | | |
| Output Current | I_O | $V_O = 0.5\text{ V}$ from rail, $V_{DD} = 2.7\text{ V}$ | Positive rail | 4.0 | | mA | | |
| | | | Negative rail | 5.0 | | | | |
| | | $V_O = 0.5\text{ V}$ from rail, $V_{DD} = 5\text{ V}$ | Positive rail | 7.0 | | | | |
| | | | Negative rail | 8.0 | | | | |
| | | $V_O = 0.5\text{ V}$ from rail, $V_{DD} = 10\text{ V}$ | Positive rail | 13 | | | | |
| | | | Negative rail | 12 | | | | |

4. $V_{DD} = \pm 5\text{ V}$ is shorthand for $V_{DD} = +5\text{ V}$ and $V_{EE} = -5\text{ V}$.

TLV271, TLV272, NCV272, TLV274, NCV274

TLV271 DC ELECTRICAL CHARACTERISTICS

($V_{DD} = 2.7V, 3.3V, 5V$ & $\pm 5V$ (Note 4), $T_A = 25^\circ C$, $R_L \geq 10 k\Omega$ unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit | |
|--------------------------------|----------|---------------------------------------|------------------|-----|-----|------|---------|
| Power Supply Quiescent Current | I_{DD} | $V_O = V_{DD}/2$ | $V_{DD} = 2.7 V$ | | 380 | 560 | μA |
| | | | $V_{DD} = 3.3 V$ | | 385 | 620 | |
| | | | $V_{DD} = 5 V$ | | 390 | 660 | |
| | | | $V_{DD} = 10 V$ | | 400 | 800 | |
| | | $T_A = -40^\circ C$ to $+105^\circ C$ | | | | 1000 | |

4. $V_{DD} = \pm 5 V$ is shorthand for $V_{DD} = +5 V$ and $V_{EE} = -5 V$.

TLV271 AC ELECTRICAL CHARACTERISTICS

($V_{DD} = 2.7 V, 5 V$, & $\pm 5 V$ (Note 5), $T_A = 25^\circ C$, and $R_L \geq 10 k\Omega$ unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit | |
|---------------------------------------|------------|----------------------------------------------------------------------------|--------------------------|---------------------------------------|----------------|-----------|-----|
| Unity Gain Bandwidth | UGBW | $R_L = 2 k\Omega, C_L = 10 pF$ | $V_{DD} = 2.7 V$ | | 3.2 | MHz | |
| | | | $V_{DD} = 5 V$ to $10 V$ | | 3.5 | | |
| Slew Rate at Unity Gain | SR | $V_{O(pp)} = V_{DD}/2, R_L = 10 k\Omega, C_L = 50 pF$ | $V_{DD} = 2.7 V$ | | 1.35 | $V/\mu S$ | |
| | | | | $T_A = -40^\circ C$ to $+105^\circ C$ | | | 1 |
| | | $V_{O(pp)} = V_{DD}/2, R_L = 10 k\Omega, C_L = 50 pF$ | $V_{DD} = 5 V$ | | 1.45 | | 2.3 |
| | | | | $T_A = -40^\circ C$ to $+105^\circ C$ | | | 1.2 |
| | | $V_{O(pp)} = V_{DD}/2, R_L = 10 k\Omega, C_L = 50 pF$ | $V_{DD} = \pm 5 V$ | | 1.8 | | 2.6 |
| $T_A = -40^\circ C$ to $+105^\circ C$ | | | | 1.3 | | | |
| Phase Margin | θ_m | $R_L = 2 k\Omega, C_L = 10 pF$ | | 45 | | $^\circ$ | |
| Gain Margin | | $R_L = 2 k\Omega, C_L = 10 pF$ | | 14 | | dB | |
| Settling Time to 0.1% | t_S | V -step(pp) = 1 V, AV = -1, $R_L = 2 k\Omega, C_L = 10 pF$ | $V_{DD} = 2.7 V$ | | 2.9 | μS | |
| | | V -step(pp) = 1 V, AV = -1, $R_L = 2 k\Omega, C_L = 47 pF$ | $V_{DD} = 5 V, \pm 5 V$ | | 2.0 | | |
| Total Harmonic Distortion plus Noise | THD+N | $V_{DD} = 2.7 V, V_{O(pp)} = V_{DD}/2, R_L = 2 k\Omega, f = 10 kHz$ | AV = 1 | | 0.004 | % | |
| | | | AV = 10 | | 0.04 | | |
| | | | AV = 100 | | 0.3 | | |
| | | $V_{DD} = 5 V, \pm 5 V, V_{O(pp)} = V_{DD}/2, R_L = 2 k\Omega, f = 10 kHz$ | AV = 1 | | 0.004 | | |
| | | | AV = 10 | | 0.04 | | |
| Input-Referred Voltage Noise | e_n | f = 1 kHz | | 30 | nV/\sqrt{Hz} | | |
| | | f = 10 kHz | | 20 | | | |
| Input-Referred Current Noise | i_n | f = 1 kHz | | 0.6 | fA/\sqrt{Hz} | | |

5. $V_{DD} = \pm 5 V$ is shorthand for $V_{DD} = +5 V$ and $V_{EE} = -5 V$.

TLV271, TLV272, NCV272, TLV274, NCV274

TLV/NCV 272/274 DC ELECTRICAL CHARACTERISTICS

($V_{DD} = 2.7\text{ V}, 5\text{ V}, 10\text{ V}, 36\text{ V}$), $T_A = 25^\circ\text{C}$, $R_L \geq 10\text{ k}\Omega$ unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--------------------------------------------------------------------------------|------------|----------------------------------------------------------------------------------------|--------------------------|-----|-------------|------------------------------|
| Input Offset Voltage | V_{IO} | $V_{IC} = V_{DD}/2$, $V_O = V_{DD}/2$, $R_L = 10\text{ k}\Omega$ | | 1.3 | ± 3 | mV |
| | | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | | | ± 4 | |
| Offset Voltage Drift | ICV_{OS} | $V_{IC} = V_{DD}/2$, $V_O = V_{DD}/2$, $R_L = 10\text{ k}\Omega$ | | 2 | | $\mu\text{V}/^\circ\text{C}$ |
| Common Mode Rejection Ratio | CMRR | $V_{CM} = V_{SS} + 0.2\text{ V}$ to $V_{DD} - 1.35\text{ V}$ | $V_{DD} = 2.7\text{ V}$ | 90 | 110 | dB |
| | | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | | 69 | | |
| | | $V_{CM} = V_{SS} + 0.2\text{ V}$ to $V_{DD} - 1.35\text{ V}$ | $V_{DD} = 5\text{ V}$ | 102 | 125 | |
| | | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | | 80 | | |
| | | $V_{CM} = V_{SS} + 0.2\text{ V}$ to $V_{DD} - 1.35\text{ V}$ | $V_{DD} = 10\text{ V}$ | 110 | 130 | |
| | | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | | 87 | | |
| | | $V_{CM} = V_{SS} + 0.2\text{ V}$ to $V_{DD} - 1.35\text{ V}$ | $V_{DD} = 36\text{ V}$ | 120 | 145 | |
| $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ (TLV/NCV272) (TLV/NCV274) | 95 85 | | | | | |
| Power Supply Rejection Ratio | PSRR | $V_{DD} = 2.7\text{ V}$ to 36 V , $V_{IC} = V_{DD}/2$, No Load | 114 | 135 | | dB |
| | | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | 100 | | | |
| Large Signal Voltage Gain | A_{VD} | $V_{O(pp)} = V_{DD}/2$, $R_L = 10\text{ k}\Omega$ | $V_{DD} = 2.7\text{ V}$ | 96 | 118 | dB |
| | | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | | 86 | | |
| | | $V_{O(pp)} = V_{DD}/2$, $R_L = 10\text{ k}\Omega$ | $V_{DD} = 5\text{ V}$ | 96 | 120 | |
| | | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | | 86 | | |
| | | $V_{O(pp)} = V_{DD}/2$, $R_L = 10\text{ k}\Omega$ | $V_{DD} = 10\text{ V}$ | 98 | 120 | |
| | | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | | 88 | | |
| | | $V_{O(pp)} = V_{DD}/2$, $R_L = 10\text{ k}\Omega$ | $V_{DD} = 36\text{ V}$ | 98 | 120 | |
| $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | 88 | | | | | |
| Input Bias Current | I_B | $V_{DD} = 5\text{ V}$, $V_{IC} = V_{DD}/2$, $V_O = V_{DD}/2$ | $T_A = 25^\circ\text{C}$ | 5 | 200 | pA |
| | | $V_{DD} = 2.7$ to 36 V , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | TLV/NCV272 | | 2000 | |
| | | | TLV/NCV274 | | 1500 | |
| Input Offset Current | I_{IO} | $V_{DD} = 5\text{ V}$, $V_{IC} = V_{DD}/2$, $V_O = V_{DD}/2$, $R_S = 50\ \Omega$ | $T_A = 25^\circ\text{C}$ | 2 | 75 | pA |
| | | $V_{DD} = 2.7$ to 36 V , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | TLV/NCV272 | | 500 | |
| | | | TLV/NCV274 | | 200 | |
| Channel Separation | XTLK | DC | TLV/NCV272 | | 100 | dB |
| | | | TLV/NCV274 | | 115 | dB |
| Differential Input Resistance | $R_{i(d)}$ | | | 5 | | G Ω |
| Common-mode Input Capacitance | C_{IC} | | | 3.5 | | pF |

TLV271, TLV272, NCV272, TLV274, NCV274

TLV/NCV 272/274 DC ELECTRICAL CHARACTERISTICS

($V_{DD} = 2.7\text{ V}, 5\text{ V}, 10\text{ V}, 36\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L \geq 10\text{ k}\Omega$ unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit | |
|--------------------------------------------------|----------|--------------------------------------------------|-------------------------|-------------|------------|-------------|---------------|
| Output Swing (High-level) | V_{OH} | $V_{IC} = V_{DD}/2$ | $V_{DD} = 2.7\text{ V}$ | | 0.006 | 0.15 | V |
| | | $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ | | | | 0.22 | |
| | | $V_{IC} = V_{DD}/2$ | $V_{DD} = 5\text{ V}$ | | 0.013 | 0.20 | |
| | | $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ | | | | 0.25 | |
| | | $V_{IC} = V_{DD}/2$ | $V_{DD} = 10\text{ V}$ | | 0.023 | 0.08 | |
| | | $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ | | | | 0.10 | |
| | | $V_{IC} = V_{DD}/2$ | $V_{DD} = 36\text{ V}$ | | 0.074 | 0.10 | |
| $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ | | | | 0.15 | | | |
| Output Swing (Low-level) | V_{OL} | $V_{IC} = V_{DD}/2$ | $V_{DD} = 2.7\text{ V}$ | | 0.005 | 0.15 | V |
| | | $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ | | | | 0.22 | |
| | | $V_{IC} = V_{DD}/2$ | $V_{DD} = 5\text{ V}$ | | 0.01 | 0.10 | |
| | | $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ | | | | 0.15 | |
| | | $V_{IC} = V_{DD}/2$ | $V_{DD} = 10\text{ V}$ | | 0.022 | 0.3 | |
| | | $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ | | | | 0.35 | |
| | | $V_{IC} = V_{DD}/2$ | $V_{DD} = 36\text{ V}$ | | 0.065 | 0.3 | |
| $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ | | | | 0.35 | | | |
| Output Current | I_O | $V_{DD} = 2.7\text{ V}$ | Positive rail | | 50 | | mA |
| | | | Negative rail | | 70 | | |
| | | $V_{DD} = 5\text{ V}$ | Positive rail | | 60 | | |
| | | | Negative rail | | 50 | | |
| | | $V_{DD} = 10\text{ V}$ | Positive rail | | 65 | | |
| | | | Negative rail | | 50 | | |
| | | $V_{DD} = 36\text{ V}$ | Positive rail | | 65 | | |
| | | | Negative rail | | 50 | | |
| Power Supply Quiescent Current | I_{DD} | $V_O = V_{DD}/2$, Per channel, no load | $V_{DD} = 2.7\text{ V}$ | | 405 | 525 | μA |
| | | | $V_{DD} = 5\text{ V}$ | | 410 | 530 | |
| | | | $V_{DD} = 10\text{ V}$ | | 416 | 540 | |
| | | | $V_{DD} = 36\text{ V}$ | | 465 | 600 | |
| | | $T_A = -40^\circ\text{C to } +105^\circ\text{C}$ | | | 700 | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Power dissipation must be limited to prevent junction temperature from exceeding 150°C . See Absolute Maximum Ratings for more information.

TLV271, TLV272, NCV272, TLV274, NCV274

TLV/NCV 272/274 AC ELECTRICAL CHARACTERISTICS

(($V_{DD} = 2.7\text{ V}, 5\text{ V}, 10\text{ V}, 36\text{ V}$), $T_A = 25^\circ\text{C}$, and $R_L \geq 10\text{ k}\Omega$ unless otherwise noted)

| Parameter | Symbol | Conditions | | Min | Typ | Max | Unit |
|--------------------------------------|------------|----------------------------------------------------------------|-------------------------|-----|-------|-----|------------------------|
| Unity Gain Bandwidth | UGBW | $C_L = 25\text{ pF}$ | $V_{DD} = 2.7\text{ V}$ | | 3 | | MHz |
| Slew Rate at Unity Gain | SR | $C_L = 20\text{ pF}, R_L = 2\text{ k}\Omega$ | $V_{DD} = 2.7\text{ V}$ | | 2.8 | | V/ μS |
| | | | $V_{DD} = 5\text{ V}$ | | 2.7 | | |
| | | | $V_{DD} = 10\text{ V}$ | | 2.6 | | |
| | | | $V_{DD} = 36\text{ V}$ | | 2.4 | | |
| Phase Margin | θ_m | $C_L = 25\text{ pF}$ | | | 50 | | $^\circ$ |
| Gain Margin | | $C_L = 25\text{ pF}$ | | | 14 | | dB |
| Settling Time to 0.1% | t_S | $V_O = 1\text{ V}_{pp}, \text{Gain} = 1, C_L = 20\text{ pF}$ | $V_{DD} = 2.7\text{ V}$ | | 0.6 | | μS |
| | | $V_O = 3\text{ V}_{pp}, \text{Gain} = 1, C_L = 20\text{ pF}$ | $V_{DD} = 5\text{ V}$ | | 1.2 | | |
| | | $V_O = 8.5\text{ V}_{pp}, \text{Gain} = 1, C_L = 20\text{ pF}$ | $V_{DD} = 10\text{ V}$ | | 3.4 | | |
| | | $V_O = 10\text{ V}_{pp}, \text{Gain} = 1, C_L = 20\text{ pF}$ | $V_{DD} = 36\text{ V}$ | | 3.2 | | |
| Total Harmonic Distortion plus Noise | THD+N | $V_{IN} = 0.5\text{ V}_{pp}, f = 1\text{ kHz}, A_v = 1$ | $V_{DD} = 2.7\text{ V}$ | | 0.05 | | % |
| | | $V_{IN} = 2.5\text{ V}_{pp}, f = 1\text{ kHz}, A_v = 1$ | $V_{DD} = 5\text{ V}$ | | 0.009 | | |
| | | $V_{IN} = 7.5\text{ V}_{pp}, f = 1\text{ kHz}, A_v = 1$ | $V_{DD} = 10\text{ V}$ | | 0.004 | | |
| | | $V_{IN} = 28.5\text{ V}_{pp}, f = 1\text{ kHz}, A_v = 1$ | $V_{DD} = 36\text{ V}$ | | 0.001 | | |
| Input-Referred Voltage Noise | e_n | $f = 1\text{ kHz}$ | | | 30 | | nV/ $\sqrt{\text{Hz}}$ |
| | | $f = 10\text{ kHz}$ | | | 20 | | |
| Input-Referred Current Noise | i_n | $f = 1\text{ kHz}$ | | | 90 | | fA/ $\sqrt{\text{Hz}}$ |

TYPICAL CHARACTERISTICS

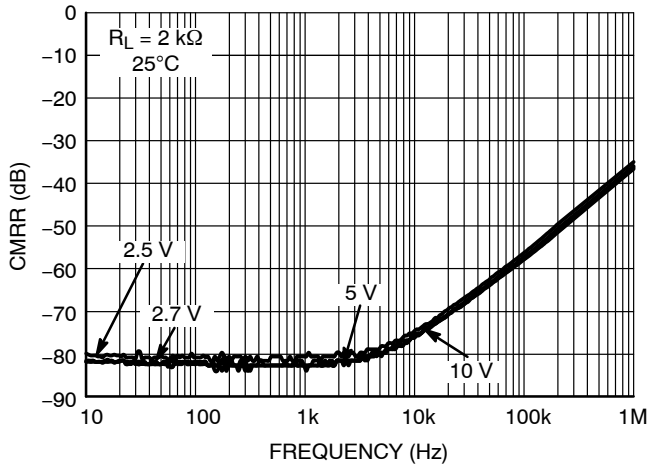


Figure 1. CMRR vs. Frequency for TLV271

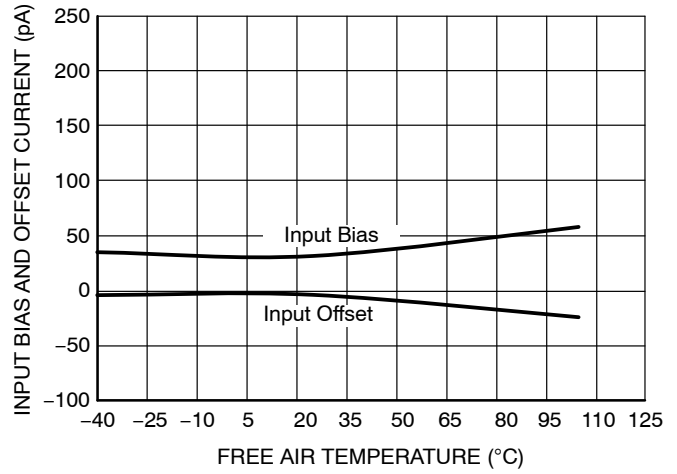


Figure 2. Input Bias and Offset Current vs. Temperature for TLV271

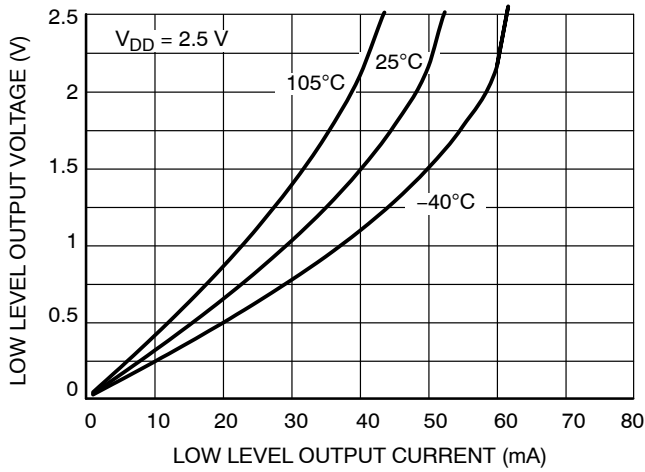


Figure 3. 2.5 V V_{OL} vs. I_{out}

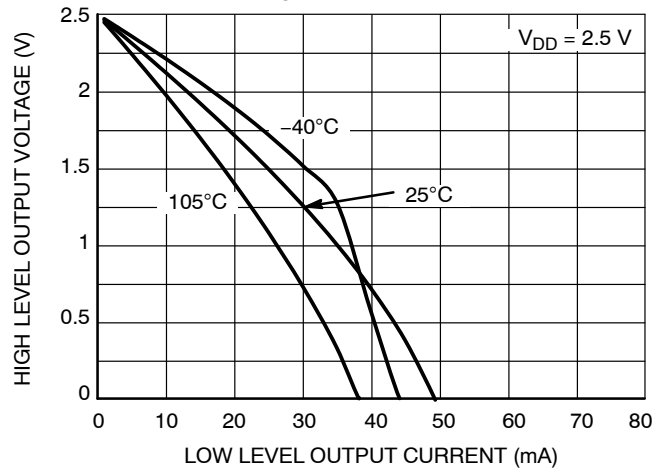


Figure 4. 2.5 V V_{OH} vs. I_{out}

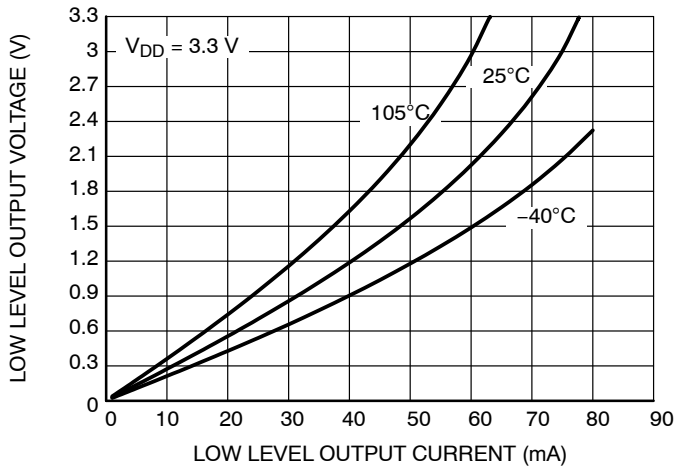


Figure 5. 3.3 V V_{OL} vs. I_{out}

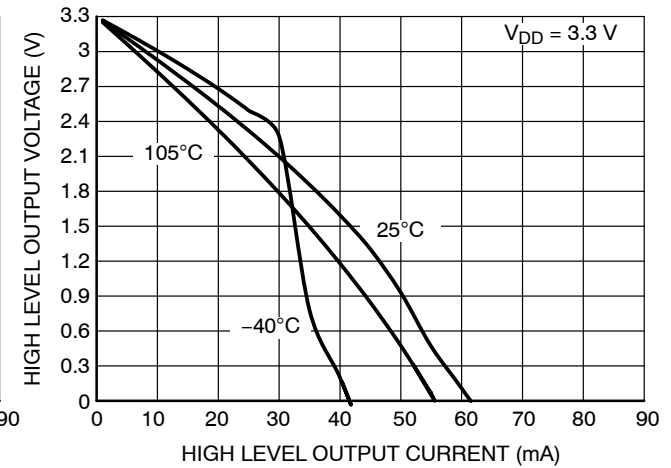


Figure 6. 3.3 V V_{OH} vs. I_{out}

TYPICAL CHARACTERISTICS

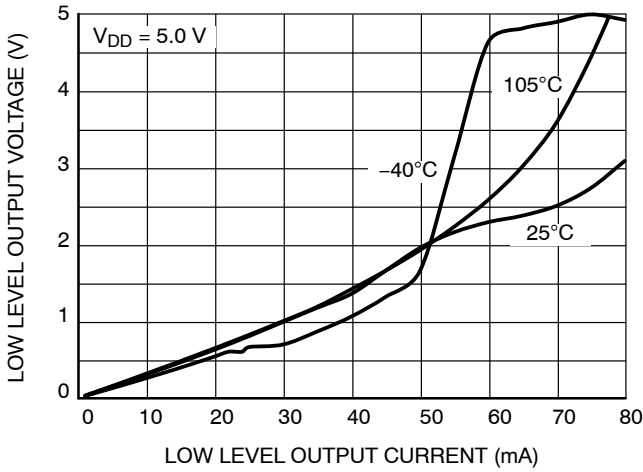


Figure 7. V_{OL} vs. I_{out}

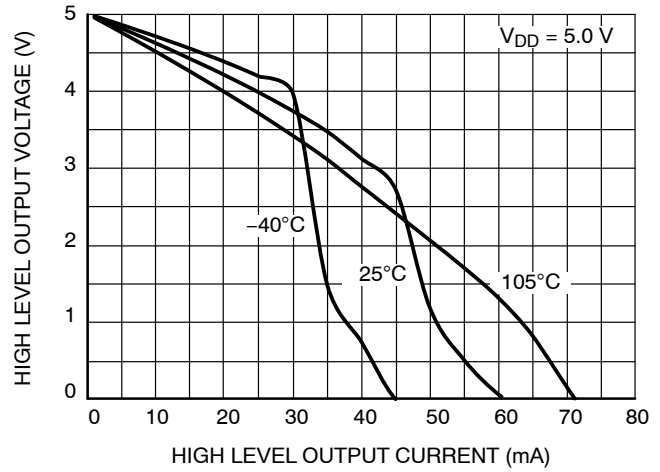


Figure 8. V_{OH} vs. I_{out}

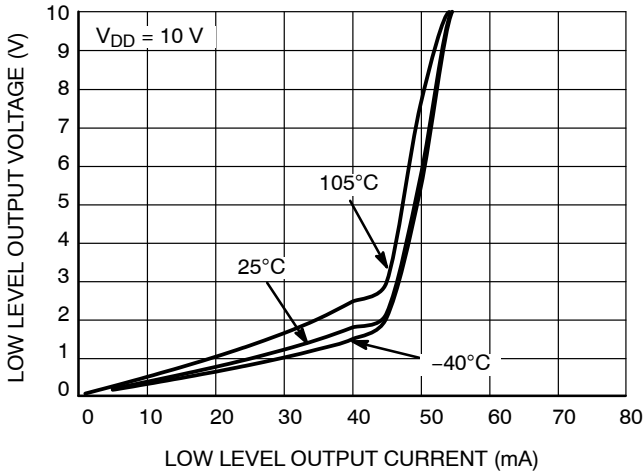


Figure 9. 10 V V_{OL} vs. I_{out}

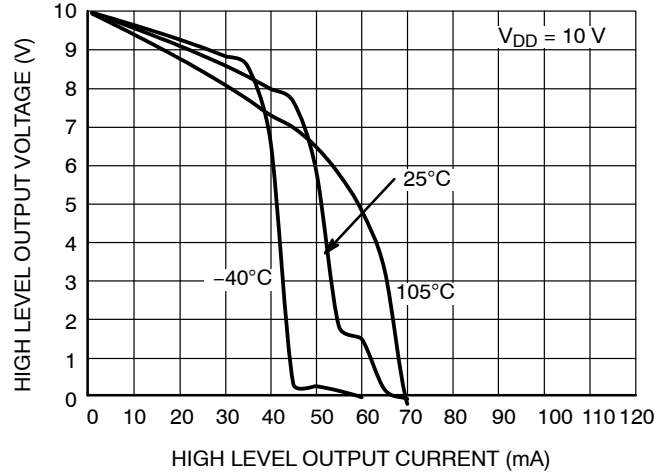


Figure 10. 10 V V_{OH} vs. I_{out}

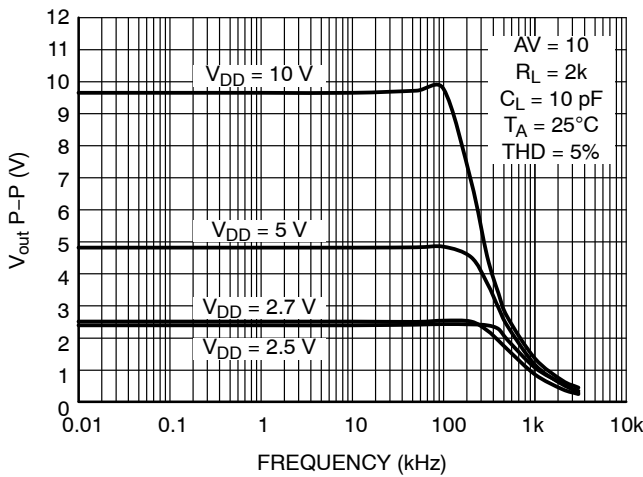


Figure 11. Peak-to-Peak Output vs. Supply vs. Frequency

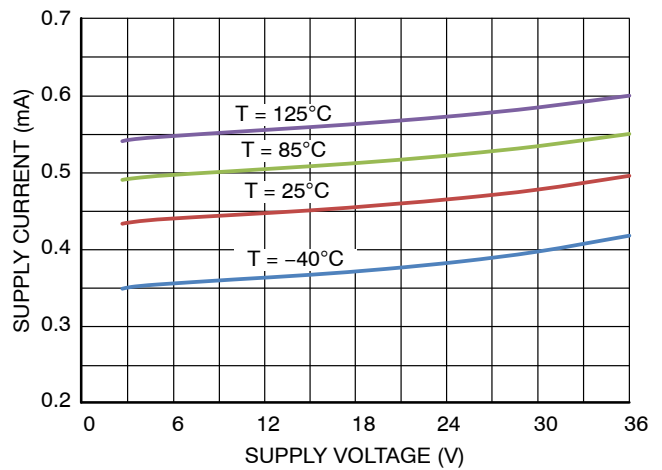


Figure 12. Quiescent Current Per Channel vs. Supply Voltage for TLV/NCV272/274

TLV271, TLV272, NCV272, TLV274, NCV274

TYPICAL CHARACTERISTICS

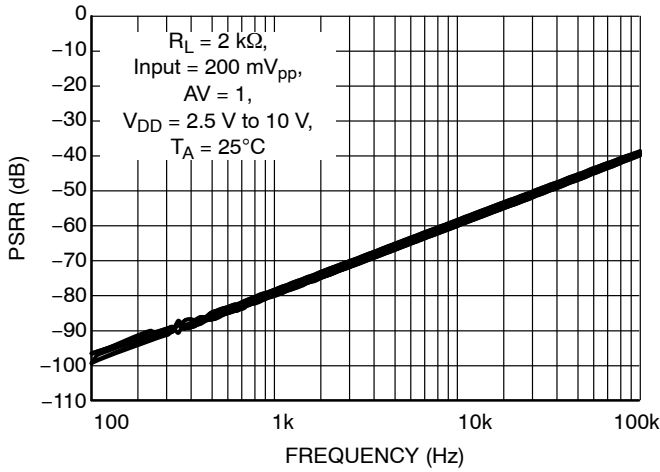


Figure 13. PSRR vs. Frequency for TLV271

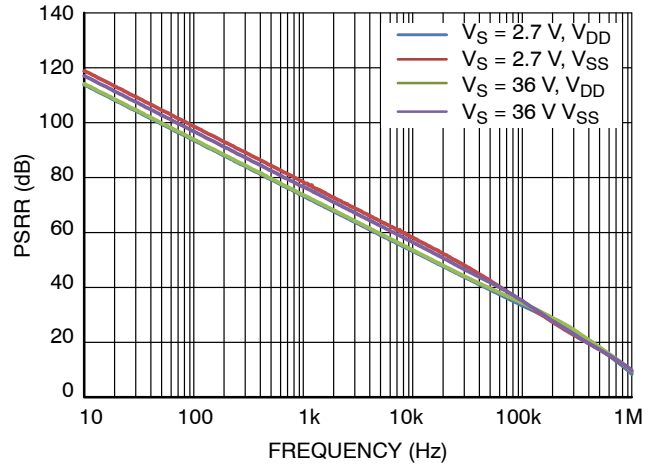


Figure 14. PSRR vs. Frequency for TLV/NCV272/274

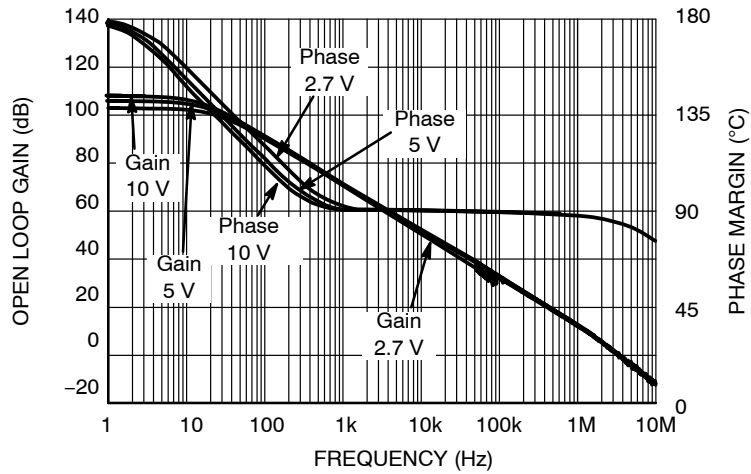


Figure 15. Open Loop Gain and Phase vs. Frequency

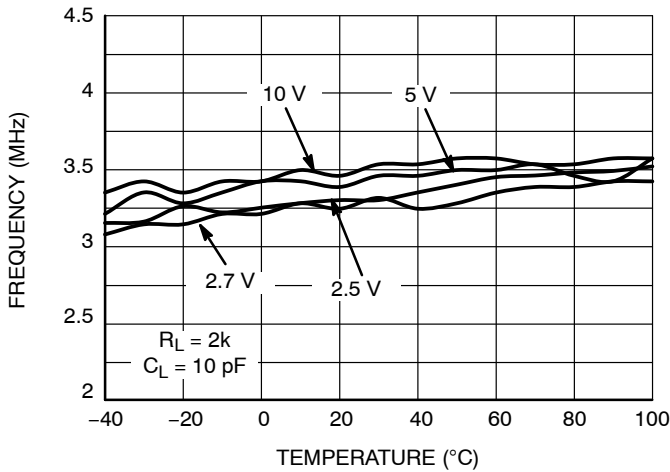


Figure 16. Gain Bandwidth Product vs. Temperature

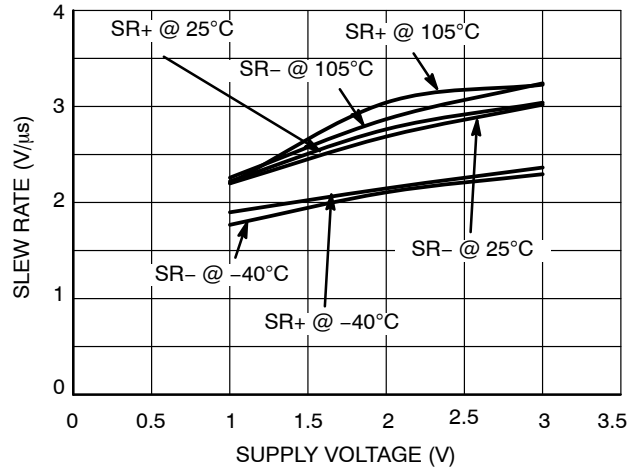


Figure 17. Slew Rate vs. Supply Voltage

TYPICAL CHARACTERISTICS

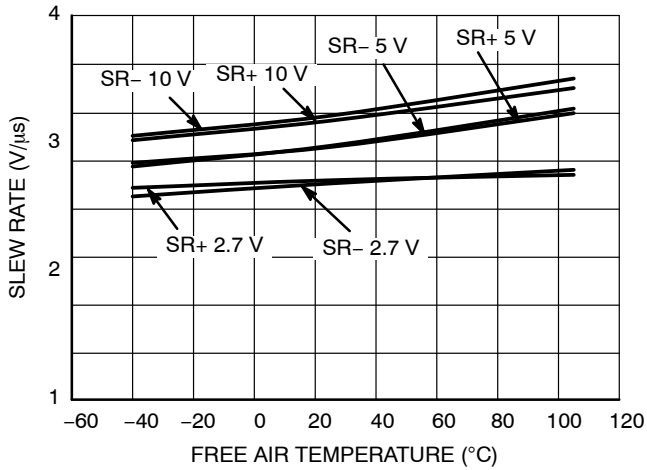


Figure 18. Slew Rate vs. Temperature

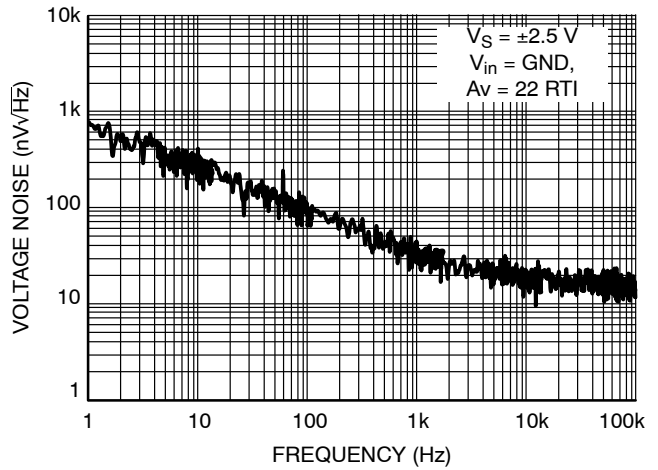


Figure 19. Voltage Noise vs. Frequency

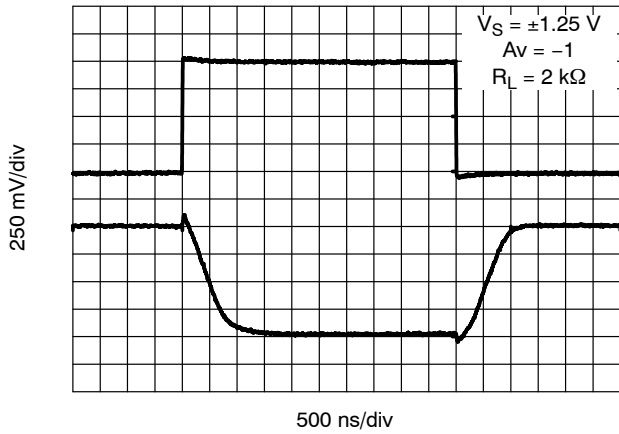


Figure 20. 2.5 V Inverting Large Signal Pulse Response

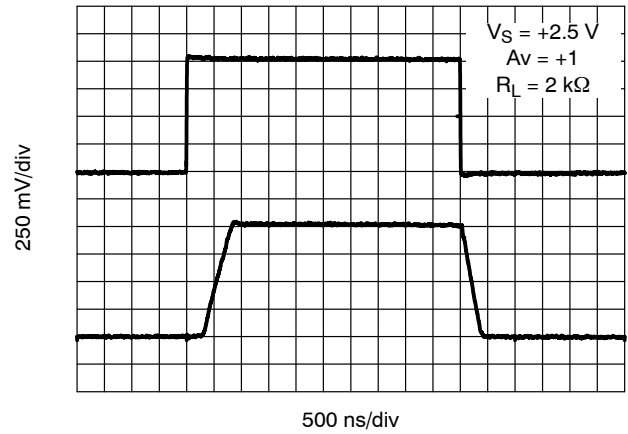


Figure 21. 2.5 V Non-Inverting Large Signal Pulse Response

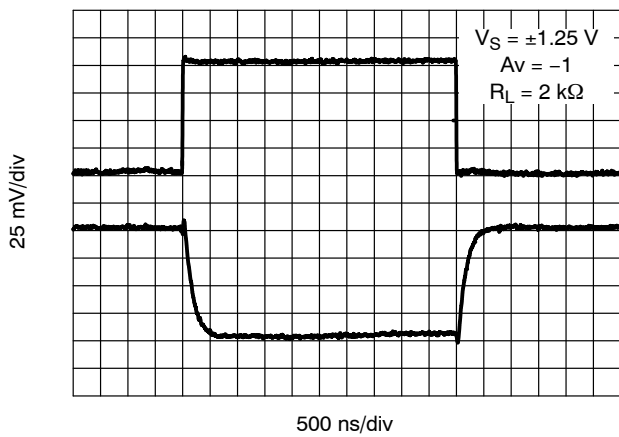


Figure 22. 2.5 V Inverting Small Signal Pulse Response

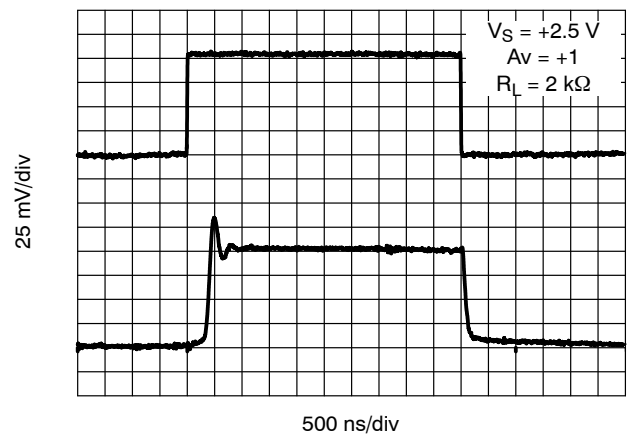
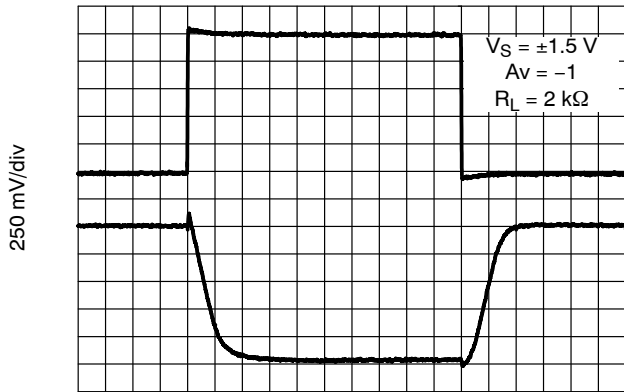


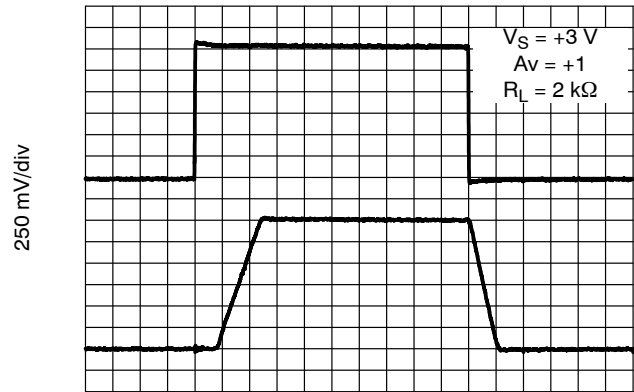
Figure 23. 2.5 V Non-Inverting Small Signal Pulse Response

TYPICAL CHARACTERISTICS



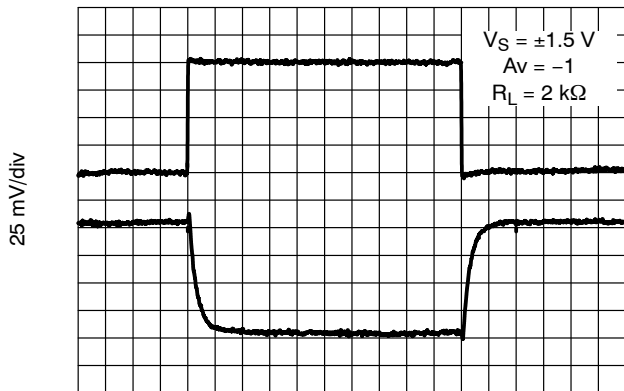
500 ns/div

Figure 24. 3 V Inverting Large Signal Pulse Response



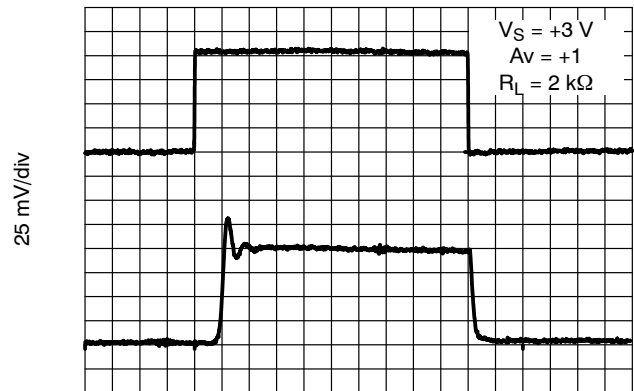
500 ns/div

Figure 25. 3 V Non-Inverting Large Signal Pulse Response



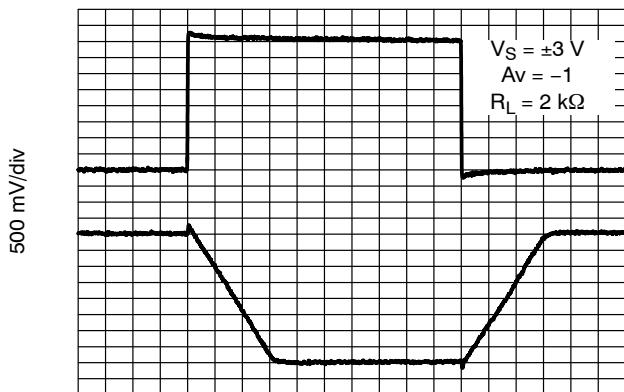
500 ns/div

Figure 26. 3 V Inverting Small Signal Pulse Response



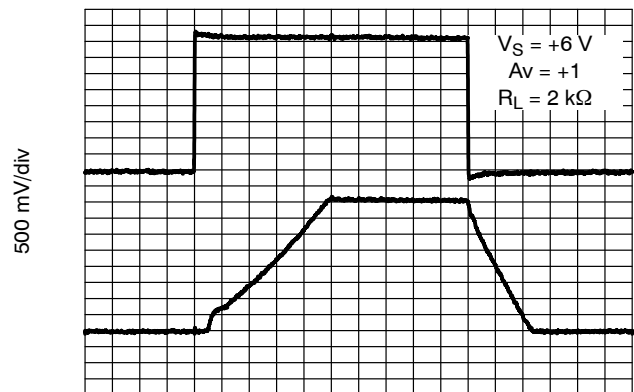
500 ns/div

Figure 27. 3 V Non-Inverting Small Signal Pulse Response



500 ns/div

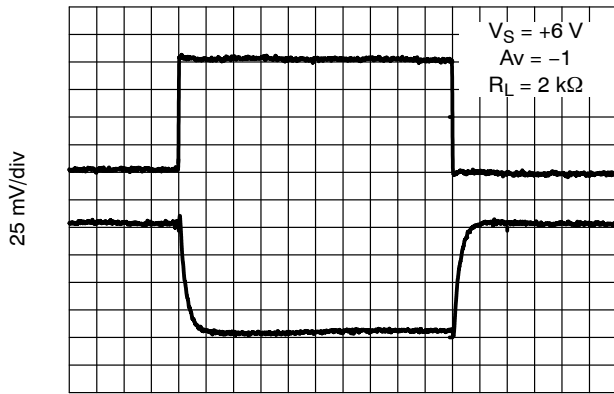
Figure 28. 6 V Inverting Large Signal Pulse Response



500 ns/div

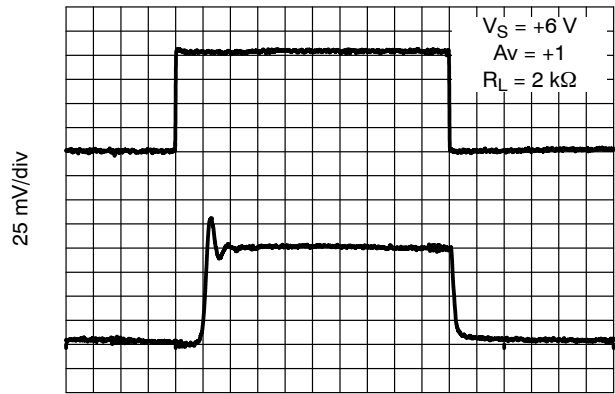
Figure 29. 6 V Non-Inverting Large Signal Pulse Response

TYPICAL CHARACTERISTICS



500 ns/div

Figure 30. 6 V Inverting Small Signal Pulse Response



500 ns/div

Figure 31. 6 V Non-Inverting Small Signal Pulse Response

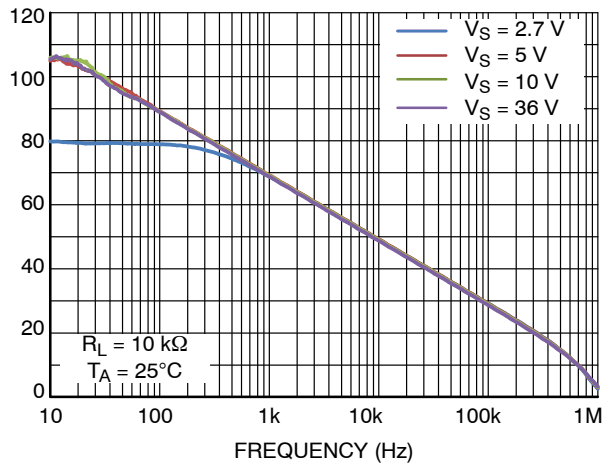


Figure 32. CMRR vs. Frequency for TLV/NCV272/274

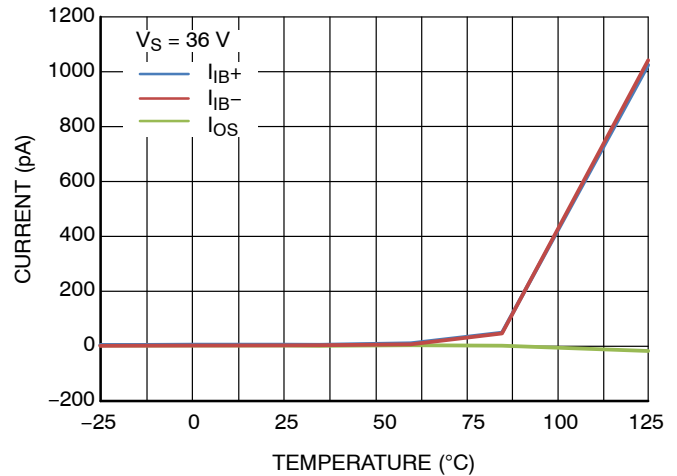


Figure 33. Input Bias and Offset Current vs. Temperature for TLV/NCV272/274

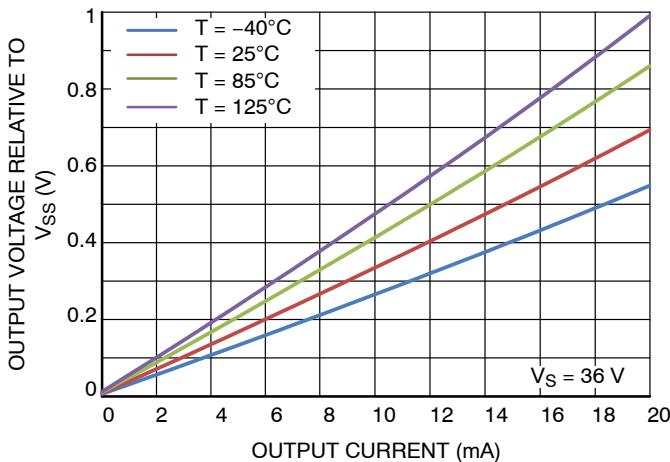


Figure 34. Low Level Output vs. Output Current for TLV/NCV272/274

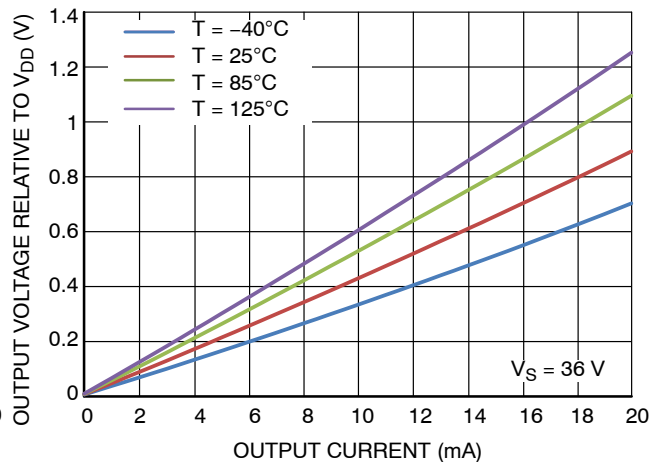


Figure 35. High Level Output vs. Output Current for TLV/NCV272/274

TYPICAL CHARACTERISTICS

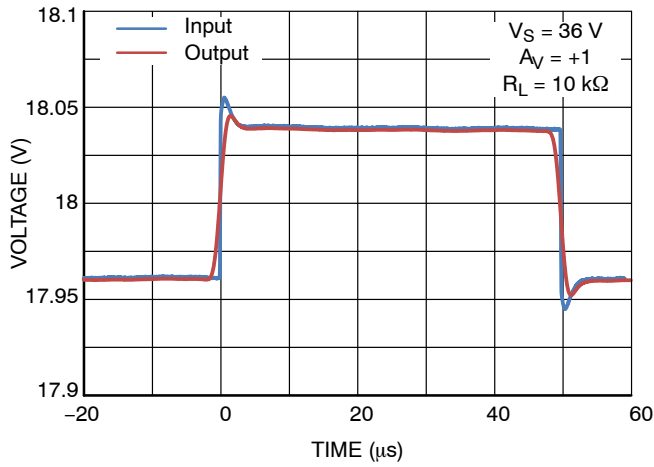


Figure 36. Non-inverting Small Signal Transient Response for TLV/NCV272/274

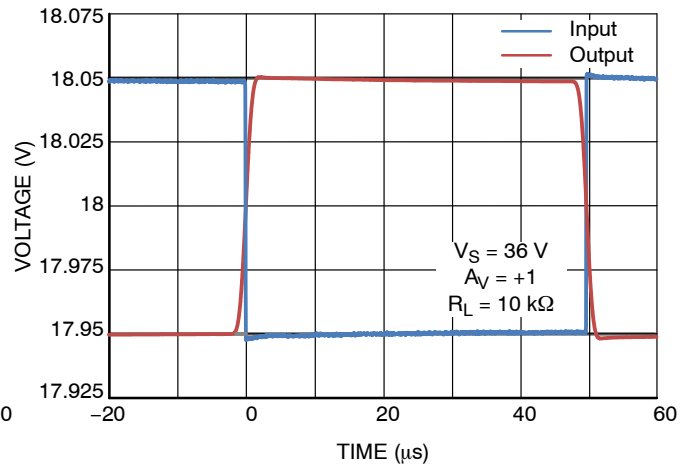


Figure 37. Inverting Small Signal Transient Response for TLV/NCV272/274

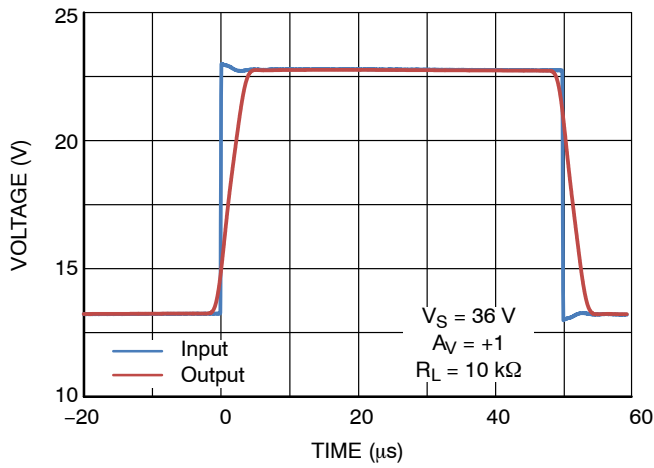


Figure 38. Non-inverting Large Signal Transient Response for TLV/NCV272/274

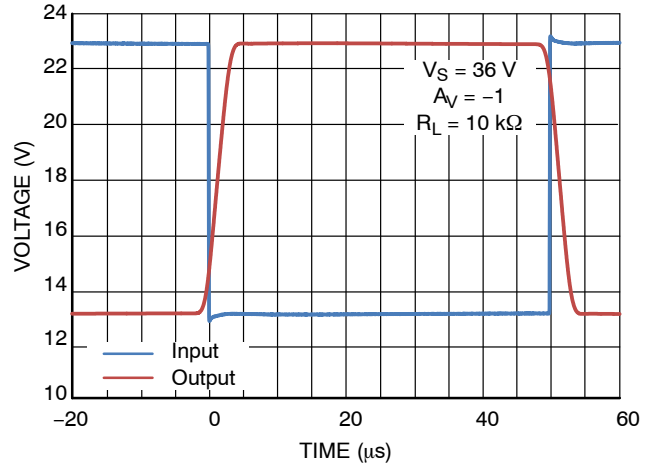


Figure 39. Inverting Large Signal Transient Response for TLV/NCV272/274

APPLICATIONS

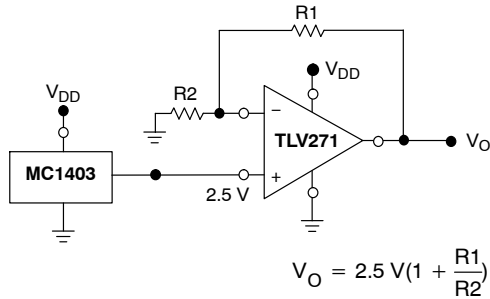


Figure 40. Voltage Reference

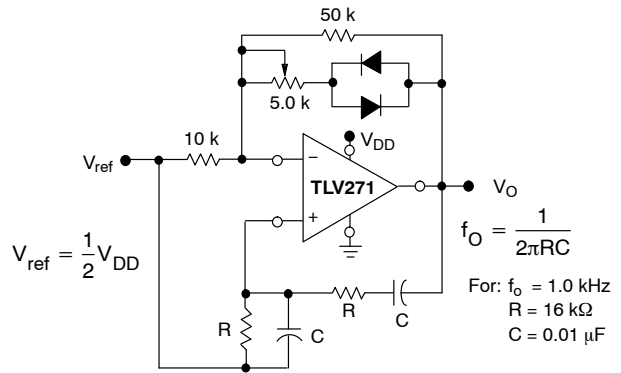


Figure 41. Wien Bridge Oscillator

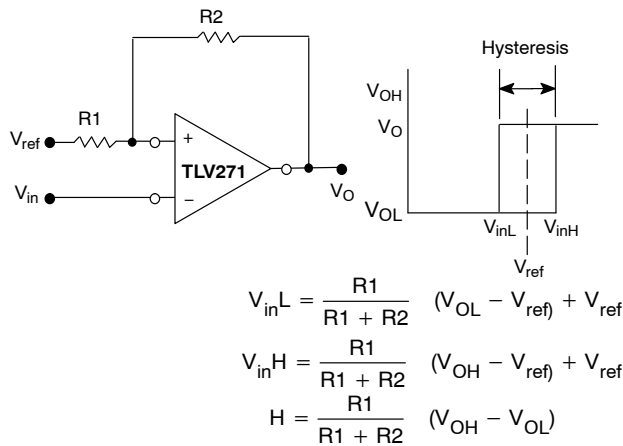
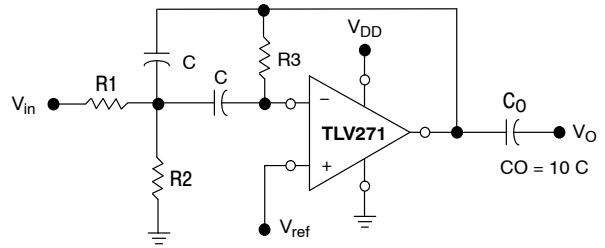


Figure 42. Comparator with Hysteresis



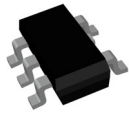
Given: f_o = center frequency
 $A(f_o)$ = gain at center frequency

Choose value f_o, C
 Then: $R3 = \frac{Q}{\pi f_o C}$
 $R1 = \frac{R3}{2 A(f_o)}$
 $R2 = \frac{R1 R3}{4Q^2 R1 - R3}$

For less than 10% error from operational amplifier,
 $((Q_o f_o)/BW) < 0.1$ where f_o and BW are expressed in Hz.
 If source impedance varies, filter may be preceded with
 voltage follower buffer to stabilize filter parameters.

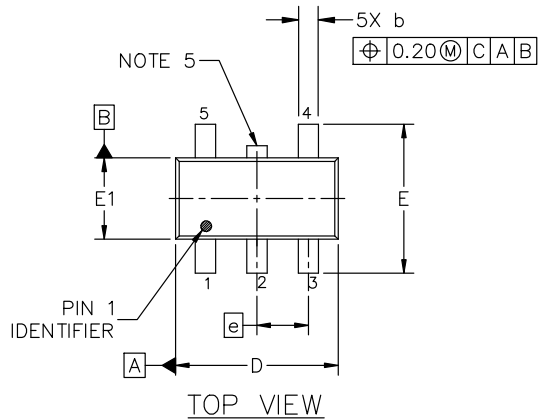
Figure 43. Multiple Feedback Bandpass Filter

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



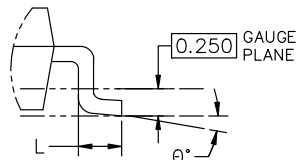
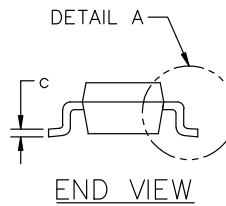
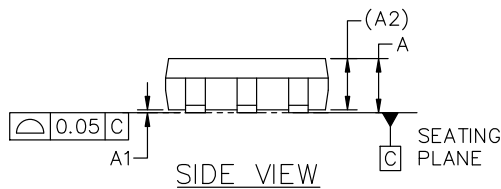
TSOP-5 3.00x1.50x0.95, 0.95P CASE 483 ISSUE P

DATE 01 APR 2024



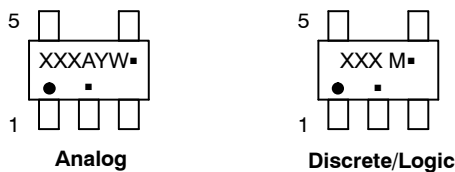
NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.



SCALE 2:1

GENERIC MARKING DIAGRAM*

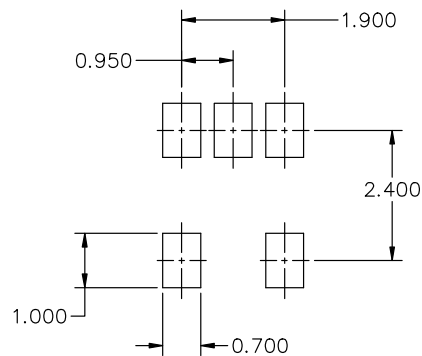


- XXX = Specific Device Code XXX = Specific Device Code
 A = Assembly Location M = Date Code
 Y = Year ▪ = Pb-Free Package
 W = Work Week

▪ = Pb-Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| DIM | MILLIMETERS | | |
|-----|-------------|-------|-------|
| | MIN. | NOM. | MAX. |
| A | 0.900 | 1.000 | 1.100 |
| A1 | 0.010 | 0.055 | 0.100 |
| A2 | 0.950 REF. | | |
| b | 0.250 | 0.375 | 0.500 |
| c | 0.100 | 0.180 | 0.260 |
| D | 2.850 | 3.000 | 3.150 |
| E | 2.500 | 2.750 | 3.000 |
| E1 | 1.350 | 1.500 | 1.650 |
| e | 0.950 BSC | | |
| L | 0.200 | 0.400 | 0.600 |
| θ | 0° | 5° | 10° |



* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

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| DESCRIPTION: | TSOP-5 3.00x1.50x0.95, 0.95P | PAGE 1 OF 1 |

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

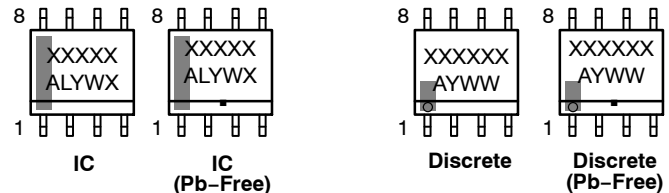
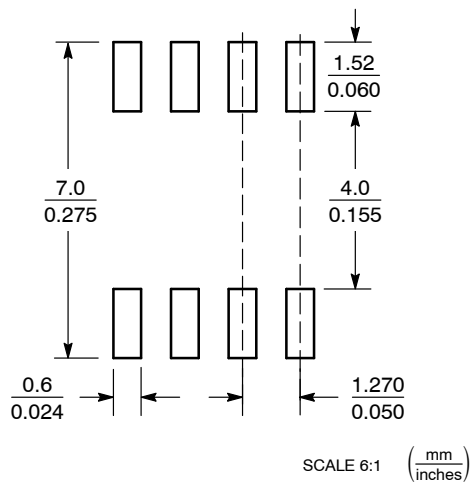


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

GENERIC MARKING DIAGRAM*

SOLDERING FOOTPRINT*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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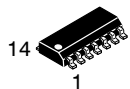
SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER</p> | <p>STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1</p> | <p>STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1</p> | <p>STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE</p> |
| <p>STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE</p> | <p>STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE</p> | <p>STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd</p> | <p>STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1</p> |
| <p>STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON</p> | <p>STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND</p> | <p>STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1</p> | <p>STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> |
| <p>STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> | <p>STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN</p> | <p>STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON</p> | <p>STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC</p> | <p>STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE</p> | <p>STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1</p> | <p>STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> |
| <p>STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6</p> | <p>STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND</p> | <p>STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT</p> | <p>STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT</p> | <p>STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC</p> | <p>STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN</p> | <p>STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN</p> |
| <p>STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1</p> | <p>STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1</p> | | |

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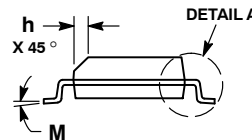
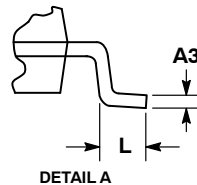
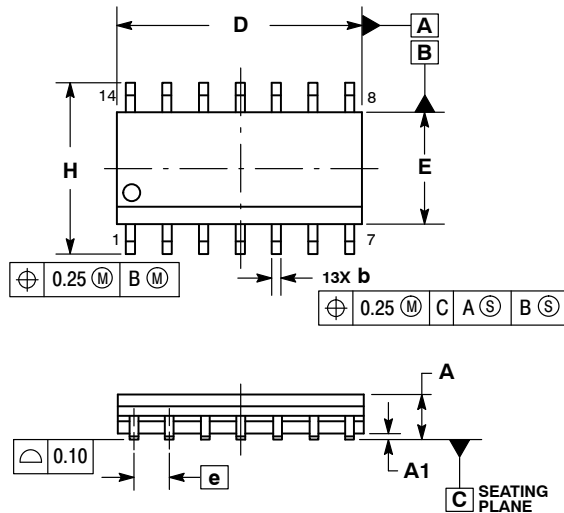
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SCALE 1:1

SOIC-14 NB
CASE 751A-03
ISSUE L

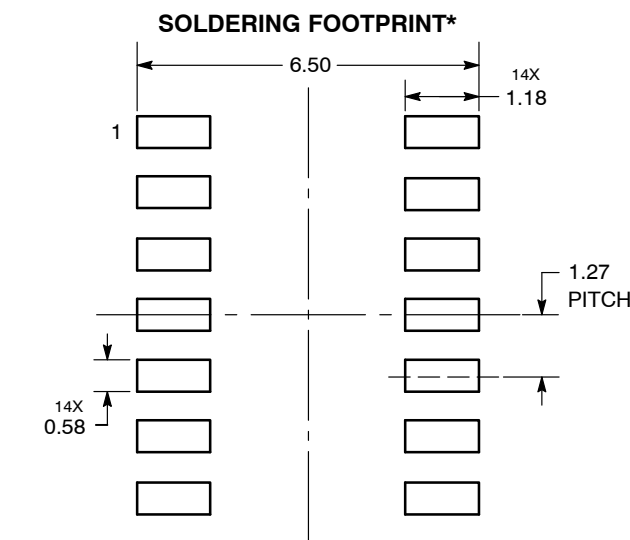
DATE 03 FEB 2016



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

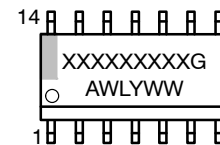
| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.054 | 0.068 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |
| b | 0.35 | 0.49 | 0.014 | 0.019 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.019 |
| L | 0.40 | 1.25 | 0.016 | 0.049 |
| M | 0° | 7° | 0° | 7° |



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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SOIC-14
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. NO CONNECTION
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 2:
 CANCELLED

STYLE 3:
 PIN 1. NO CONNECTION
 2. ANODE
 3. ANODE
 4. NO CONNECTION
 5. ANODE
 6. NO CONNECTION
 7. ANODE
 8. ANODE
 9. ANODE
 10. NO CONNECTION
 11. ANODE
 12. ANODE
 13. NO CONNECTION
 14. COMMON CATHODE

STYLE 4:
 PIN 1. NO CONNECTION
 2. CATHODE
 3. CATHODE
 4. NO CONNECTION
 5. CATHODE
 6. NO CONNECTION
 7. CATHODE
 8. CATHODE
 9. CATHODE
 10. NO CONNECTION
 11. CATHODE
 12. CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 5:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. COMMON ANODE
 8. COMMON CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 6:
 PIN 1. CATHODE
 2. CATHODE
 3. CATHODE
 4. CATHODE
 5. CATHODE
 6. CATHODE
 7. CATHODE
 8. ANODE
 9. ANODE
 10. ANODE
 11. ANODE
 12. ANODE
 13. ANODE
 14. ANODE

STYLE 7:
 PIN 1. ANODE/CATHODE
 2. COMMON ANODE
 3. COMMON CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. COMMON CATHODE
 12. COMMON ANODE
 13. ANODE/CATHODE
 14. ANODE/CATHODE

STYLE 8:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. COMMON ANODE
 8. COMMON ANODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. NO CONNECTION
 12. ANODE/CATHODE
 13. ANODE/CATHODE
 14. COMMON CATHODE

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

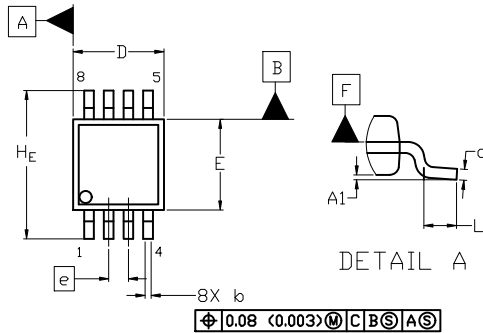
ON Semiconductor®



SCALE 2:1

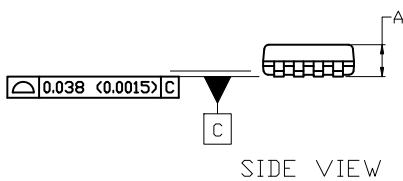
Micro8 CASE 846A-02 ISSUE K

DATE 16 JUL 2020

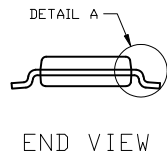


TOP VIEW

NOTE 3



SIDE VIEW

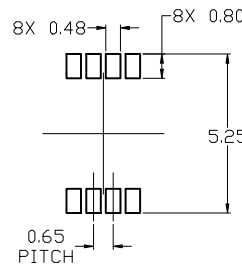


END VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS *D* AND *E* DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION *E* DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS *D* AND *E* ARE DETERMINED AT DATUM *F*.
5. DATUMS *A* AND *B* ARE TO BE DETERMINED AT DATUM *F*.
6. *A1* IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

$\phi 0.08$ (0.003) M C B S A S

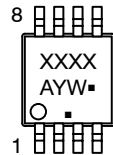


RECOMMENDED MOUNTING FOOTPRINT

| DIM | MILLIMETERS | | |
|----------------------|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | --- | --- | 1.10 |
| A1 | 0.05 | 0.08 | 0.15 |
| <i>b</i> | 0.25 | 0.33 | 0.40 |
| <i>c</i> | 0.13 | 0.18 | 0.23 |
| <i>D</i> | 2.90 | 3.00 | 3.10 |
| <i>E</i> | 2.90 | 3.00 | 3.10 |
| <i>e</i> | 0.65 BSC | | |
| <i>H_E</i> | 4.75 | 4.90 | 5.05 |
| <i>L</i> | 0.40 | 0.55 | 0.70 |

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:

1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

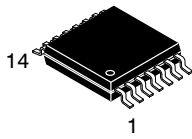
STYLE 3:

1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

| | | |
|-------------------------|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
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| DESCRIPTION: | MICRO8 | PAGE 1 OF 1 |

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TSSOP-14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016

SCALE 2:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

GENERIC MARKING DIAGRAM*

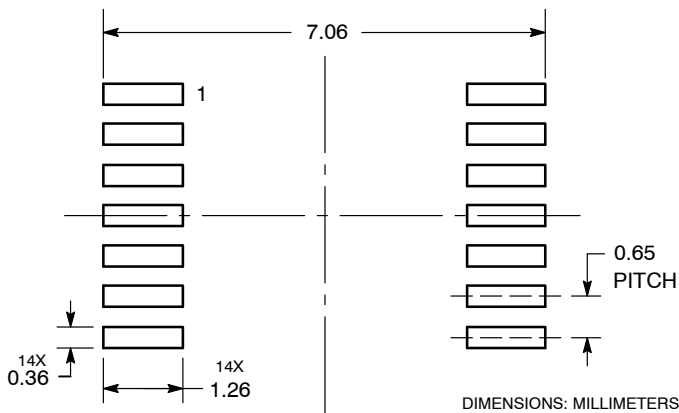


- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT



| | | |
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