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NTE74195
Integrated Circuit
TTL – 4–Bit Parallel Access Shift Register

Description:

The NTE74195 is a 4–bit parallel access shift register in a 16–Lead plastic DIP type package and features parallel inputs, parallel outputs, J–$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The register has two distinct modes of operation:

Parallel (Broadside) Load
Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip–flop and appears at the outputs after the positive transition of the clock input.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J–$\overline{K}$ inputs. These inputs permit the first stage to perform as a J–$\overline{K}$, D–, or T–type flip–flop as shown in the function table.

Features:

- Synchronous Parallel Load
- Positive Edge–Triggered Clock
- Parallel Inputs and Outputs from Each Flip–Flop
- Direct Overriding Clear
- J and $\overline{K}$ Inputs to First Stage
- Complementary Outputs from Last Stage

Applications:

- Accumulators/Processors
- Serial–to–Parallel, Parallel–to–Serial Converter

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
DC Input Voltage, V_{IN} 5.5V
Power Dissipation, P_D 195mW
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High−Level Output Current	I_{OH}	–	–	−800	μA
Low−Level Output Current	I_{OL}	–	–	16	mA
Clock Frequency	f_{clock}	0	–	30	MHz
Width of Clock or Clear Pulse	$t_{w(clock)}$	16	–	–	ns
Width of Clear Input Pulse	$t_{w(clear)}$	12	–	–	ns
Shift/Load Setup Time	t_{su}	25	–	–	ns
Serial and Parallel Data Setup Time	t_{su}	20	–	–	ns
Clear Inactive−State Setup Time	t_{su}	25	–	–	ns
Shift/Load Release Time	$t_{release}$	–	–	10	ns
Serial and Parallel Data Hold Time	t_h	0	–	–	ns
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High−Level Input Voltage	V_{IH}		2	–	–	V
Low−Level Input Voltage	V_{IL}		–	–	0.8	V
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −12mA	–	–	−1.5	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −800μA	2.4	3.4	–	V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA	–	0.2	0.4	V
Input Current	I_I	V_{CC} = MAX, V_I = 5.5V	–	–	1	mA
High Level Input Current	I_{IH}	V_{CC} = MAX, V_I = 2.4V	–	–	40	μA
Low Level Input Current	I_{IL}	V_{CC} = MAX, V_I = 0.4V	–	–	−1.6	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 4	−18	–	−57	mA
Supply Current	I_{CC}	V_{CC} = MAX, Note 5	–	39	63	mA

Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 3. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 4. Not more than one output should be shorted at a time and duration of short−circuit should not exceed one second.

Note 5. With all outputs open, shift/load grounded, and 4.5V applied to the J, $\overline{K}$, and data inputs, I_{CC} is measured by applying a momentary GND, followed by 4.5V to clear and then applying a momentary ground, followed by 4.5V to clock.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Clock Frequency	f_{max}	R_L = 400Ω, C_L = 15pF	30	39	–	MHz
Propagation Delay Time (from Clear)	t_{PHL}		–	19	30	ns
Propagation Delay Time (from Clock)	t_{PLH}		–	14	22	ns
	t_{PHL}		–	17	26	ns

Function Table:

Inputs									Outputs				
			Serial		Parallel								
Clear	Shift/ Load	Clock	J	$\overline{K}$	A	B	C	D	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = HIGH Level (Steady State)

L = LOW Level (Steady State)

X = Irrelevant (Any input, including transitional)

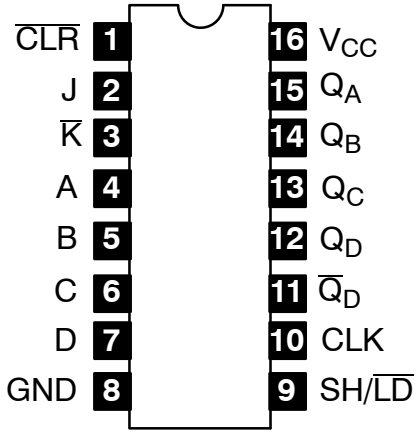
↑ = Transition from LOW to HIGH Level

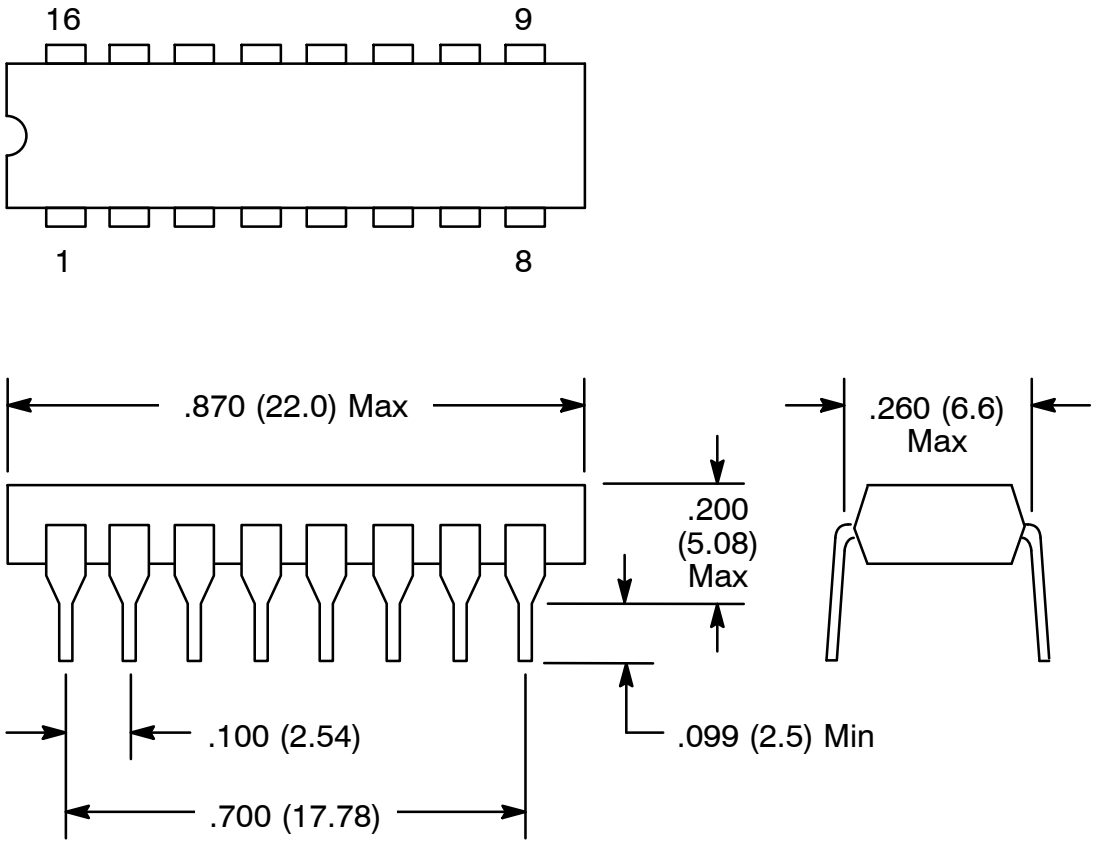
a, b, c, d = The level of steady−state input at inputs A, B, C, or D respectively

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D respectively, before the indicated steady−state input conditions were established

Q_{An}, Q_{Bn}, Q_{Cn} = The level of Q_A, Q_B, Q_C respectively, before the most recent transition of the clock.

Pin Connection Diagram




16
9
1
8
.870 (22.0) Max
.260 (6.6)
Max
.200
(5.08)
Max
.100 (2.54)
.099 (2.5) Min
.700 (17.78)