

High-Performance WVGA Display Module with maXTouch[®] Information Sheet

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Sweden - Gothenberg - 46-31-704-60-40
Sweden - Stockholm - 46-8-5090-4654
UK - Wokingham - 44-118-921-5800

The High-Performance WVGA Display Module with maXTouch (AC320005-5) is designed for evaluating the Microchip graphics display solution and graphics library for 32-bit microcontrollers. This board is compatible with both versions of the Multimedia Expansion Board II (DM320005-2 or DM320005-5), as well as with Xplained Pro and Xplained Ultra evaluation kits. This board has a TFT 800 x 480 display with a 24-bit parallel RGB interface with a maXTouch capacitive touch interface.

Features

- 800 x 480 TFT display
- maXTouch MXT640
- QTouch[®] QT1070 (with four navigation keys)
- 4 K-bit 1-wire EEPROM
- Integrated Projective Capacitive Touch (PCAP) panel

Running the High-Performance WVGA Display Module with maXTouch Demonstration Code

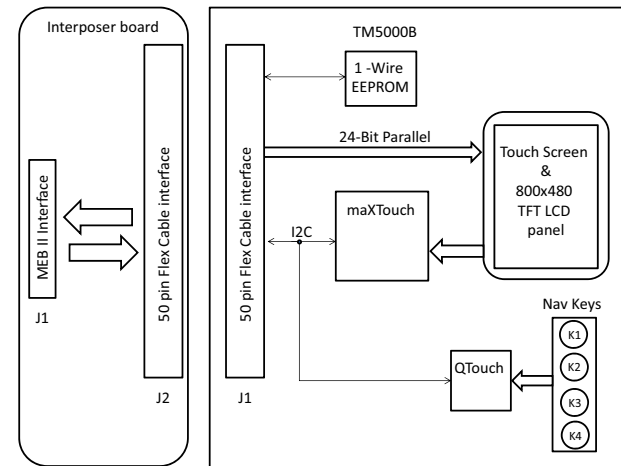
For free Microchip demonstration code and additional information, visit the MPLAB[®] Harmony web page at www.microchip.com/harmony.

After MPLAB Harmony is installed, refer to the following MPLAB Harmony installation folder for demonstration purposes:

```
C:\microchip\harmony\<<version_number>\apps\gfx
```

To work with older Xplained Pro and Xplained Ultra evaluation kits, disconnect the ribbon connector from the adapter board and connect it to the GFX port (50 flex) of the Xplained Pro or Xplained Ultra.

FIGURE 1: WVGA DISPLAY MODULE BLOCK DIAGRAM



10/25/17

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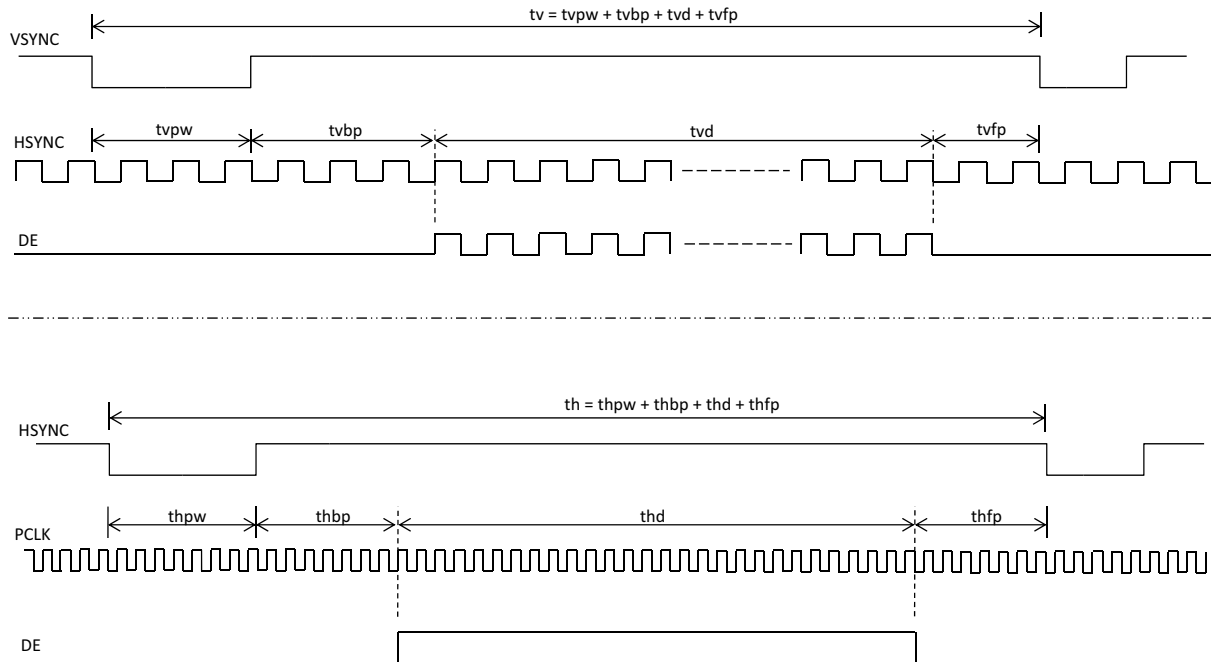
DS50002681B



High-Performance WVGA Display Module with maXTouch® Board Timing Specifications

TABLE 1: TIMING SPECIFICATION VALUES

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Clock Cycle	1/PCLK	-	30	40	MHz
Hsync Cycle	1/th	-	10.7	-	kHz
Vsync Cycle	1/tv	-	19	-	Hz
Horizontal Signal					
Horizontal Cycle	th	-	928	-	CLK
Horizontal Display Period	thd	800	800	800	CLK
Horizontal Front Porch	thfp	-	40	-	CLK
Horizontal Pulse width	thpw	1	48	-	CLK
Horizontal Back Porch	thbp	-	40	-	CLK
Vertical Signals					
Vertical Cycle	tv	-	525	-	Hsync
Vertical Display Period	tvd	480	480	480	Hsync
Vertical Front Porch	tvfp	-	13	-	Hsync
Vertical Pulse Width	tpw	1	3	-	Hsync
Vertical Back Porch	tvbp	-	29	-	Hsync



Bottom Contacts Use Type 1 FFC

Xplained Interface

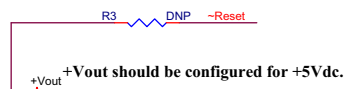
J2	1	ONE_WIRE
	2	GND
	3	LCDDAT0
	4	LCDDAT1
	5	LCDDAT2
	6	LCDDAT3
	7	GND
	8	LCDDAT4
	9	LCDDAT5
	10	LCDDAT6
	11	LCDDAT7
	12	GND
	13	LCDDAT8
	14	LCDDAT9
	15	LCDDAT10
	16	LCDDAT11
	17	GND
	18	LCDDAT12
	19	LCDDAT13
	20	LCDDAT14
	21	LCDDAT15
	22	GND
	23	LCDDAT16
	24	LCDDAT17
	25	LCDDAT18
	26	LCDDAT19
	27	GND
	28	LCDDAT20
	29	LCDDAT21
	30	LCDDAT22
	31	LCDDAT23
	32	GND
	33	PCLK
	34	VSYNC
	35	HSYNC
	36	DE
	37	SCK
	38	MOSI
	39	MISO
	40	~SS
	41	DISP
	42	SDA
	43	SCL
	44	~CHG_mxt
	45	~CHG_QT
	46	LCD_PWM
	47	~Reset_IN
	48	+Vout
	49	+Vout
	50	GND

CON50



~CHG_QT is connected to Pin 53 for future use if desired.

SCK, MOSI, MISO and ~SS are connected to Pins 54, 56, 58 and 57 (respectively) for future use if desired.



Debug Header

J3	1	GND
	2	~CHG_QT
	3	~CHG_mxt
	4	SCL
	5	SDA
	6	DE
	7	HSYNC
	8	VSYNC
	9	PCLK
	10	GND

CON10

MEB II Interface

	11				
GND	1	2	GND		
GND	3	4	GND		
+3.3Vdc	5	6	+3.3Vdc		
LCDDAT12	7	8	LCDDAT8		
LCDDAT13	9	10	LCDDAT9		
LCDDAT14	11	12	LCDDAT10		
LCDDAT15	13	14	LCDDAT11		
LCDDAT16	15	16	LCDDAT0		
LCDDAT17	17	18	LCDDAT1		
LCDDAT18	19	20	LCDDAT2		
LCDDAT19	21	22	LCDDAT3		
LCDDAT20	23	24	LCDDAT4		
GND	25	26	GND		
+3.3Vdc	27	28	+3.3Vdc		
LCDDAT21	29	30	LCDDAT5		
LCDDAT22	31	32	LCDDAT6		
LCDDAT23	33	34	LCDDAT7		
PCLK	35	36	ONE_WIRE		
VSYNC	37	38	HSYNC		
DE	39	40			
~CHG_mxt	41	42	SCL		
	43	44	SDA		
LCD_PWM	45	46	DISP		
GND	47	48	GND		
+5Vdc	49	50	+5Vdc		
~CHG_QT	51	52	SCK		
~Reset	53	54	MOSI		
~SS	55	56	MISO		
GND	57	58	GND		
GND	59	60	GND		

DF12 (3.0)-60DS-05V (86)

ONE_WIRE is connected to Pin 38 for future use if desired.

Microchip "LCD_CS" is not used by PDA LCD interface

Microchip "LCD_Reset" is connected to PDA "DISP". When DISP is low the LCD is in standby mode. When DISP is high the LCD is in normal display mode.

Mounting Holes

