



**PRELIMINARY**

**CY62187G30 MoBL**

## 64-Mbit (4M words × 16-bit) Static RAM with Error-Correcting Code (ECC)

### Features

- Ultra-low standby current
  - Typical standby current: 6  $\mu$ A
  - Maximum standby current: 38  $\mu$ A
- High speed: 55 ns
- Embedded error-correcting code (ECC) for single-bit error correction<sup>[1]</sup>
- Operating voltage range: 2.2 V to 3.6 V
- 1.0-V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Error indication (ERR) pin to indicate 1-bit error detection and correction
- Available in Pb-free 48-ball VFPGA package

### Functional Description

CY62187G30 is a high-performance CMOS, low-power (MoBL<sup>®</sup>) SRAM device with embedded ECC<sup>[2]</sup>. This device is offered in Dual Chip Enable option.

To access a Dual Chip Enable device, assert both Chip Enable inputs –  $\overline{CE}_1$  as LOW and  $CE_2$  as HIGH.

To perform data writes, assert the Write Enable ( $\overline{WE}$ ) input LOW, and provide the data and address on the device data pins ( $I/O_0$  through  $I/O_{15}$ ) and address pins ( $A_0$  through  $A_{21}$ ) respectively. The Byte High Enable ( $\overline{BHE}$ ) and Byte Low Enable ( $\overline{BLE}$ ) inputs control byte writes and write data on the corresponding I/O lines to the memory location specified.  $\overline{BHE}$  controls  $I/O_8$  through  $I/O_{15}$  and  $\overline{BLE}$  controls  $I/O_0$  through  $I/O_7$ .

To perform data reads, assert the Output Enable ( $\overline{OE}$ ) input and provide the required address on the address lines. You can access the read data on the I/O lines ( $I/O_0$  through  $I/O_{15}$ ). To perform byte accesses, assert the required byte enable signal ( $\overline{BHE}$  or  $\overline{BLE}$ ) to read either the upper byte or the lower byte of the data from the specified address location.

All I/Os ( $I/O_0$  through  $I/O_{15}$ ) are placed in a High-Z state when the device is deselected ( $\overline{CE}_1$  HIGH /  $CE_2$  LOW for a Dual Chip Enable device), or the control signals are deasserted ( $\overline{OE}$ ,  $\overline{BLE}$ ,  $\overline{BHE}$ ).

These devices have a unique byte power-down feature where, when both Byte Enables ( $\overline{BHE}$  and  $\overline{BLE}$ ) are disabled, the devices seamlessly switch to the standby mode irrespective of the state of the Chip Enables, thereby saving power.

CY62187G30 is available in a Pb-free 48-ball VFPGA package. See [Logic Block Diagram – CY62187G30 on page 2](#).

For a complete list of related documentation, click [here](#).

### Product Portfolio

| Product    | Features and Options<br>(see <a href="#">Pin Configuration – CY62187G30</a> ) | Range      | $V_{CC}$ Range (V) | Speed (ns) | Current Consumption       |     |                               |     |
|------------|---|------------|--------------------|------------|---------------------------|-----|-------------------------------|-----|
|            |   |            |                    |            | Operating $I_{CC}$ , (mA) |     | Standby, $I_{SB2}$ ( $\mu$ A) |     |
|            |   |            |                    |            | $f = f_{max}$             |     |                               |     |
|            |   |            |                    |            | Typ <sup>[3]</sup>        | Max | Typ <sup>[3]</sup>            | Max |
| CY62187G30 | Dual Chip Enable  | Industrial | 2.2 V–3.6 V        | 55         | 40                        | 55  | 6                             | 38  |

#### Notes

1. SER FIT rate <0.1 FIT/Mb. Refer to [AN88889](#) for details.
2. This device does not support automatic write-back on error detection.
3. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at  $V_{CC} = 3$  V (for  $V_{CC}$  range of 2.2 V–3.6 V),  $T_A = 25^\circ$ C.

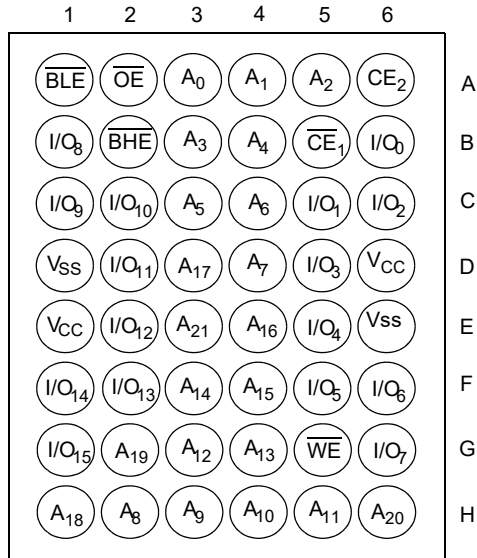


## Contents

|   |           |  |           |
|---|-----------|--|-----------|
| <b>Pin Configuration – CY62187G30</b> ..... | <b>4</b>  | <b>Ordering Information</b> .....                    | <b>14</b> |
| <b>Maximum Ratings</b> .....                | <b>5</b>  | Ordering Code Definitions .....                      | 14        |
| <b>Operating Range</b> .....                | <b>5</b>  | <b>Package Diagram</b> .....                         | <b>15</b> |
| <b>DC Electrical Characteristics</b> .....  | <b>5</b>  | <b>Acronyms</b> .....                                | <b>16</b> |
| <b>Capacitance</b> .....                    | <b>6</b>  | <b>Document Conventions</b> .....                    | <b>16</b> |
| <b>Thermal Resistance</b> .....             | <b>6</b>  | Units of Measure .....                               | 16        |
| <b>AC Test Loads and Waveforms</b> .....    | <b>6</b>  | <b>Document History Page</b> .....                   | <b>17</b> |
| <b>Data Retention Characteristics</b> ..... | <b>7</b>  | <b>Sales, Solutions, and Legal Information</b> ..... | <b>18</b> |
| <b>Data Retention Waveform</b> .....        | <b>7</b>  | Worldwide Sales and Design Support .....             | 18        |
| <b>Switching Characteristics</b> .....      | <b>8</b>  | Products .....                                       | 18        |
| <b>Switching Waveforms</b> .....            | <b>9</b>  | PSoC® Solutions .....                                | 18        |
| <b>Truth Table – CY62187G30</b> .....       | <b>13</b> | Cypress Developer Community .....                    | 18        |
|   |           | Technical Support .....                              | 18        |

**Pin Configuration – CY62187G30**

**Figure 1. 48-ball VFBGA Pinout (Dual Chip Enable) – CY62187G30 [4]**



**Notes**

4. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.
5. Tie the  $\overline{\text{BYTE}}$  pin in the 48-pin TSOP I package to V<sub>CC</sub> to use the device as a 2M × 16 SRAM. The 48-pin TSOP I package can also be used as a 4M × 8 SRAM by tying the  $\overline{\text{BYTE}}$  signal to V<sub>SS</sub>. In the 4M × 8 configuration, pin 45 is the extra address line A21, while  $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$ , and I/O<sub>8</sub> to I/O<sub>14</sub> pins are not used and can be left floating.

### Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

- Storage temperature ..... -65°C to + 150°C
- Ambient temperature with power applied ..... -55°C to + 125°C
- Supply voltage to ground potential ..... -0.5 V to V<sub>CC</sub> + 0.5 V
- DC voltage applied to outputs in High Z state<sup>[6]</sup> ..... -0.5 V to V<sub>CC</sub> + 0.5 V

- DC input voltage<sup>[6]</sup> ..... -0.5 V to V<sub>CC</sub> + 0.5 V
- Output current into outputs (LOW) ..... 20 mA
- Static discharge voltage (MIL-STD-883, Method 3015) ..... >2001 V
- Latch-up current ..... >140 mA

### Operating Range

| Grade      | Ambient Temperature | V <sub>CC</sub> <sup>[7]</sup> |
|------------|---------------------|--------------------------------|
| Industrial | -40 °C to +85 °C    | 2.2 V to 3.6 V                 |

### DC Electrical Characteristics

Over the operating range of -40°C to 85°C

| Parameter                        | Description  | Test Conditions  | 55 ns  |                    |                       | Unit |    |
|----------------------------------|--|--|--|--------------------|-----------------------|------|----|
|                                  |  |  | Min  | Typ <sup>[8]</sup> | Max                   |      |    |
| V <sub>OH</sub>                  | Output HIGH voltage  | 2.2 V to 2.7 V   | V <sub>CC</sub> = Min, I <sub>OH</sub> = -0.1 mA |                    | 2.0                   | V    |    |
|                                  |  | 2.7 V to 3.6 V   | V <sub>CC</sub> = Min, I <sub>OH</sub> = -1.0 mA |                    | 2.4                   |      |    |
| V <sub>OL</sub>                  | Output LOW voltage   | 2.2 V to 2.7 V   | V <sub>CC</sub> = Min, I <sub>OL</sub> = 0.1 mA  |                    | -                     | V    |    |
|                                  |  | 2.7 V to 3.6 V   | V <sub>CC</sub> = Min, I <sub>OL</sub> = 2.1 mA  |                    | 0.4                   |      |    |
| V <sub>IH</sub>                  | Input HIGH voltage <sup>[6]</sup>  | 2.2 V to 2.7 V   | -  | -                  | V <sub>CC</sub> + 0.3 | V    |    |
|                                  |  | 2.7 V to 3.6 V   | -  | -                  | V <sub>CC</sub> + 0.3 |      |    |
| V <sub>IL</sub>                  | Input LOW voltage <sup>[6]</sup>   | 2.2 V to 2.7 V   | -  | -                  | 0.6                   | V    |    |
|                                  |  | 2.7 V to 3.6 V   | -  | -                  | 0.8                   |      |    |
| I <sub>IX</sub>                  | Input leakage current  | GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>  | -1.0   | -                  | +1.0                  | µA   |    |
| I <sub>OZ</sub>                  | Output leakage current   | GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output disabled   | -1.0   | -                  | +1.0                  | µA   |    |
| I <sub>CC</sub>                  | V <sub>CC</sub> operating supply current                                     | V <sub>CC</sub> = Max, I <sub>OUT</sub> = 0 mA, CMOS levels  | f = 22.22 MHz (45 ns)                            | -                  | 40                    | 55.0 | mA |
|                                  |  |  | f = 1 MHz  | -                  | 15                    | 38.0 |    |
| I <sub>SB1</sub> <sup>[11]</sup> | Automatic Power-down Current – CMOS Inputs; V <sub>CC</sub> = 2.2 V to 3.6 V | $\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$<br>or $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2 \text{ V}$ ,<br>$V_{IN} \geq V_{CC} - 0.2 \text{ V}$ , $V_{IN} \leq 0.2 \text{ V}$ ,<br>$f = f_{max}$ (address and data only),<br>$f = 0$ ( $\overline{OE}$ , and $\overline{WE}$ ), $V_{CC} = V_{CC(max)}$ | -  | 12.0               | 38.0                  | µA   |    |
| I <sub>SB2</sub> <sup>[11]</sup> | Automatic Power-down Current – CMOS Inputs V <sub>CC</sub> = 2.2 V to 3.6 V  | $\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or<br>$CE_2 \leq 0.2 \text{ V}$ or<br>$(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2 \text{ V}$ ,<br>$V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or<br>$V_{IN} \leq 0.2 \text{ V}$ ,<br>$f = 0$ , $V_{CC} = V_{CC(max)}$   | -  | -                  | -                     | µA   |    |
|                                  |  |  | -  | -                  | -                     |      |    |
|                                  |  |  | -  | -                  | -                     |      |    |
|                                  |  |  | -  | -                  | 6.0                   | 38.0 |    |

**Notes**

6. V<sub>IL(min)</sub> = -2.0 V and V<sub>IH(max)</sub> = V<sub>CC</sub> + 2 V for pulse durations of less than 20 ns.
7. Full device AC operation assumes a 100-µs ramp time from 0 to V<sub>CC</sub> (min) and 400-µs wait time after V<sub>CC</sub> stabilizes to its operational value.
8. Indicates the value for the center of distribution at 3.0 V, 25°C and not 100% tested.
9. Chip enables (CE<sub>1</sub> and CE<sub>2</sub>) and BYTE must be tied to CMOS levels to meet the I<sub>SB1</sub> / I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.
10. The I<sub>SB2</sub> maximum limits at 25 °C, 40 °C, and 70 °C are guaranteed by design and not 100% tested.

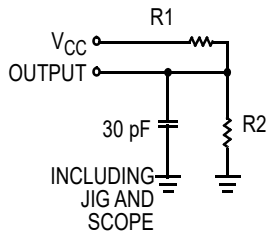
**Capacitance**

| Parameter <sup>[11]</sup> | Description        | Test Conditions   | Max  | Unit |
|---------------------------|--------------------|---|------|------|
| C <sub>IN</sub>           | Input capacitance  | T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub> | 15.0 | pF   |
| C <sub>OUT</sub>          | Output capacitance |   | 15.0 | pF   |

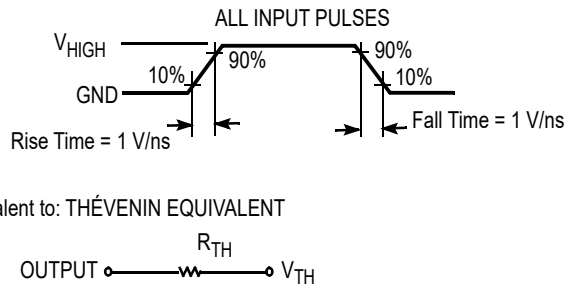
**Thermal Resistance**

| Parameter <sup>[11]</sup> | Description                              | Test Conditions   | 48-ball VFBGA | Unit |
|---------------------------|--|---|---------------|------|
| Θ <sub>JA</sub>           | Thermal resistance (junction to ambient) | Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board | 82.6          | °C/W |
| Θ <sub>JC</sub>           | Thermal resistance (junction to case)    |   | 10.8          | °C/W |

**AC Test Loads and Waveforms**



**Figure 2. AC Test Loads and Waveforms**



| Parameters        | 2.5 V | 3.0 V | Unit |
|-------------------|-------|-------|------|
| R1                | 16667 | 1103  | Ω    |
| R2                | 15385 | 1554  | Ω    |
| R <sub>TH</sub>   | 8000  | 645   | Ω    |
| V <sub>TH</sub>   | 1.20  | 1.75  | V    |
| V <sub>HIGH</sub> | 2.5   | 3.0   | V    |

**Note**

11. Tested initially and after any design or process changes that may affect these parameters.

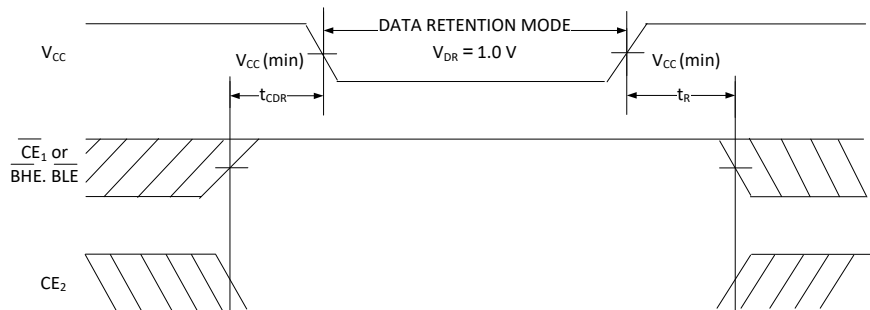
## Data Retention Characteristics

Over the Operating Range

| Parameter             | Description                          | Conditions   | Min  | Typ <sup>[12]</sup> | Max  | Unit          |
|-----------------------|--------------------------------------|--|------|---------------------|------|---------------|
| $V_{DR}$              | $V_{CC}$ for data retention          | –  | 1.5  | –                   | –    | V             |
| $I_{CCDR}^{[13, 14]}$ | Data retention current               | $2.2\text{ V} < V_{CC} \leq 3.6\text{ V}$<br>$\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$<br>or $(\overline{BHE}$ and $\overline{BLE}) \geq V_{CC} - 0.2\text{ V}$ ,<br>$V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$      | –    | 6.0                 | 38.0 | $\mu\text{A}$ |
|                       |                                      | $1.5\text{ V} \leq V_{CC} \leq 2.2\text{ V}$ ,<br>$\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$<br>or $(\overline{BHE}$ and $\overline{BLE}) \geq V_{CC} - 0.2\text{ V}$ ,<br>$V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$ | –    | –                   | 48.0 |               |
| $t_{CDR}^{[15]}$      | Chip deselect to data retention time | –  | 0.0  | –                   | –    | –             |
| $t_R^{[15, 16]}$      | Operation recovery time              | –  | 55.0 | –                   | –    | ns            |

## Data Retention Waveform

Figure 3. Data Retention Waveform<sup>[17]</sup>



### Notes

12. Indicates the value for the center of distribution at 3.0 V, 25°C and not 100% tested.
13. Chip Enables ( $\overline{CE}_1$  and  $CE_2$ ) and  $\overline{BYTE}$  must be tied to CMOS levels to meet the  $I_{SB1} / I_{SB2} / I_{CCDR}$  spec. Other inputs can be left floating.
14.  $I_{CCDR}$  is guaranteed only after the device is first powered up to  $V_{CC(min)}$  and then brought down to  $V_{DR}$ .
15. These parameters are guaranteed by design and are not tested.
16. Full-device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 400\ \mu\text{s}$  or stable at  $V_{CC(min)} \geq 400\ \mu\text{s}$ .
17.  $\overline{BHE}.\overline{BLE}$  is the AND of both  $\overline{BHE}$  and  $\overline{BLE}$ . Deselect the chip by either disabling the chip enable signals or by disabling both  $\overline{BHE}$  and  $\overline{BLE}$ .

## Switching Characteristics

| Parameter <sup>[18]</sup>              | Description   | 55 ns |      | Unit |
|--|---|-------|------|------|
|  |   | Min   | Max  |      |
| <b>Read Cycle</b>                      |   |       |      |      |
| t <sub>RC</sub>                        | Read cycle time   | 55.0  | –    | ns   |
| t <sub>AA</sub>                        | Address to data valid / Address to ERR valid  | –     | 55.0 | ns   |
| t <sub>OHA</sub>                       | Data hold from address change / ERR hold from address change                                    | 10.0  | –    | ns   |
| t <sub>ACE</sub>                       | $\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to data valid / $\overline{CE}$ LOW to ERR valid | –     | 55.0 | ns   |
| t <sub>DOE</sub>                       | $\overline{OE}$ LOW to data valid / $\overline{OE}$ LOW to ERR valid                            | –     | 25.0 | ns   |
| t <sub>LZOE</sub>                      | $\overline{OE}$ LOW to low Z <sup>[19, 20]</sup>  | 5.0   | –    | ns   |
| t <sub>HZOE</sub>                      | $\overline{OE}$ HIGH to High-Z <sup>[19, 20, 21]</sup>  | –     | 18.0 | ns   |
| t <sub>LZCE</sub>                      | $\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to low Z <sup>[19, 20]</sup>                     | 10.0  | –    | ns   |
| t <sub>HZCE</sub>                      | $\overline{CE}_1$ HIGH and CE <sub>2</sub> LOW to High-Z <sup>[19, 20, 21]</sup>                | –     | 18.0 | ns   |
| t <sub>PU</sub>                        | $\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to power-up <sup>[22]</sup>                      | 0.0   | –    | ns   |
| t <sub>PD</sub>                        | $\overline{CE}_1$ HIGH and CE <sub>2</sub> LOW to power-down <sup>[22]</sup>                    | –     | 55.0 | ns   |
| t <sub>DBE</sub>                       | BLE / BHE LOW to data valid   | –     | 55.0 | ns   |
| t <sub>LZBE</sub>                      | BLE / $\overline{BHE}$ LOW to low Z <sup>[19]</sup>   | 5.0   | –    | ns   |
| t <sub>HZBE</sub>                      | $\overline{BLE}$ / $\overline{BHE}$ HIGH to High-Z <sup>[19, 21]</sup>                          | –     | 18.0 | ns   |
| <b>Write Cycle <sup>[23, 24]</sup></b> |   |       |      |      |
| t <sub>WC</sub>                        | Write cycle time  | 55.0  | –    | ns   |
| t <sub>SCE</sub>                       | $\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to write end                                     | 40.0  | –    | ns   |
| t <sub>AW</sub>                        | Address setup to write end  | 40.0  | –    | ns   |
| t <sub>HA</sub>                        | Address hold from write end   | 0     | –    | ns   |
| t <sub>SA</sub>                        | Address setup to write start  | 0     | –    | ns   |
| t <sub>PWE</sub>                       | $\overline{WE}$ pulse width   | 40.0  | –    | ns   |
| t <sub>BW</sub>                        | $\overline{BLE}$ / $\overline{BHE}$ LOW to write end  | 40.0  | –    | ns   |
| t <sub>SD</sub>                        | Data setup to write end   | 25.0  | –    | ns   |
| t <sub>HD</sub>                        | Data hold from write end  | 0.0   | –    | ns   |
| t <sub>HZWE</sub>                      | $\overline{WE}$ LOW to High-Z <sup>[19, 20, 21]</sup>   | –     | 18.0 | ns   |
| t <sub>LZWE</sub>                      | $\overline{WE}$ HIGH to low Z <sup>[19, 20]</sup>   | 10.0  | –    | ns   |

### Notes

18. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for V<sub>CC</sub> ≥ 3 V) and V<sub>CC</sub>/2 (for V<sub>CC</sub> < 3 V), and input pulse levels of 0 to 3 V (for V<sub>CC</sub> ≥ 3 V) and 0 to V<sub>CC</sub> (for V<sub>CC</sub> < 3V). Test conditions for the read cycle use the output loading shown in Figure 2 on page 6, unless specified otherwise.
19. At any temperature and voltage condition, t<sub>HZOE</sub> is less than t<sub>LZCE</sub>, t<sub>HZBE</sub> is less than t<sub>LZBE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any device.
20. Tested initially and after any design or process changes that may affect these parameters.
21. t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZBE</sub>, and t<sub>HZWE</sub> transitions are measured when the outputs enter a high-impedance state.
22. These parameters are guaranteed by design and are not tested.
23. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  or  $\overline{BLE}$  or both = V<sub>IL</sub>, and CE<sub>2</sub> = V<sub>IH</sub>. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
24. The minimum write cycle pulse width for Write Cycle No. 1 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be equal to the sum of t<sub>HZWE</sub> and t<sub>SD</sub>.



### Switching Waveforms

Figure 4. Read Cycle No. 1 of CY62187G30 (Address Transition Controlled) [25, 26]

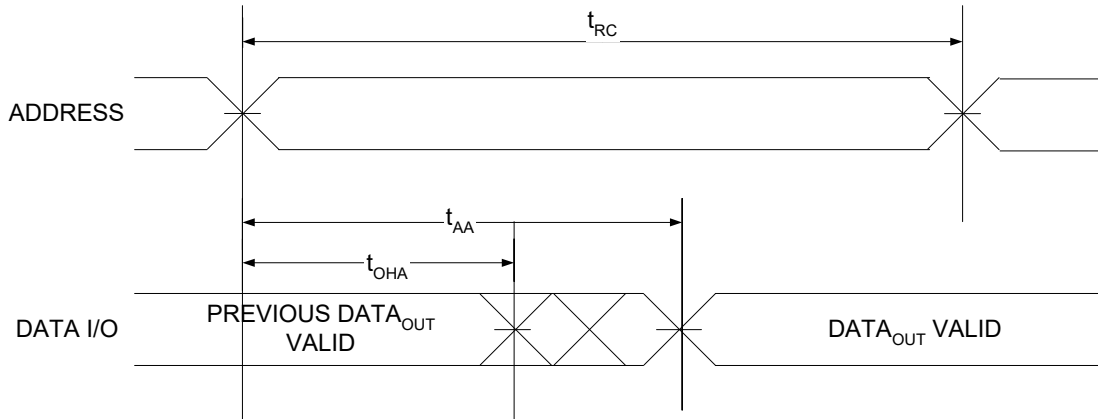
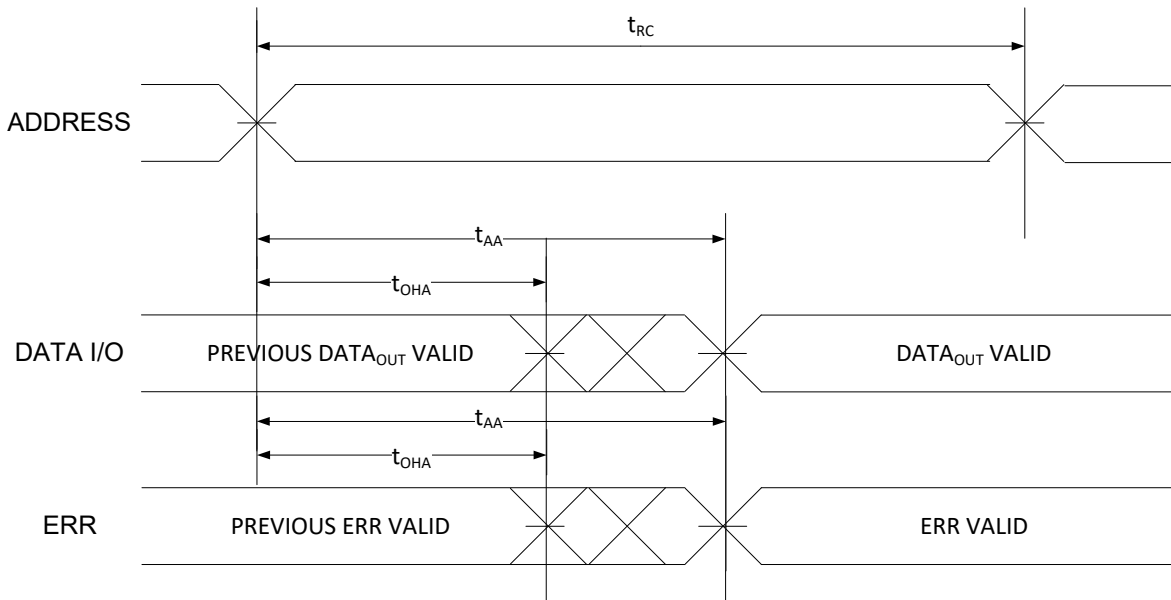


Figure 5. Read Cycle No. 1 of CY62177GE30 (Address Transition Controlled) [25, 26]



**Notes**

- 25. The device is continuously selected.  $\overline{OE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  or  $\overline{BLE}$ , or both =  $V_{IL}$ .
- 26.  $\overline{WE}$  is HIGH for read cycle.

Switching Waveforms (continued)

Figure 6. Read Cycle No. 2 ( $\overline{OE}$  Controlled) [27, 28, 29, 31]

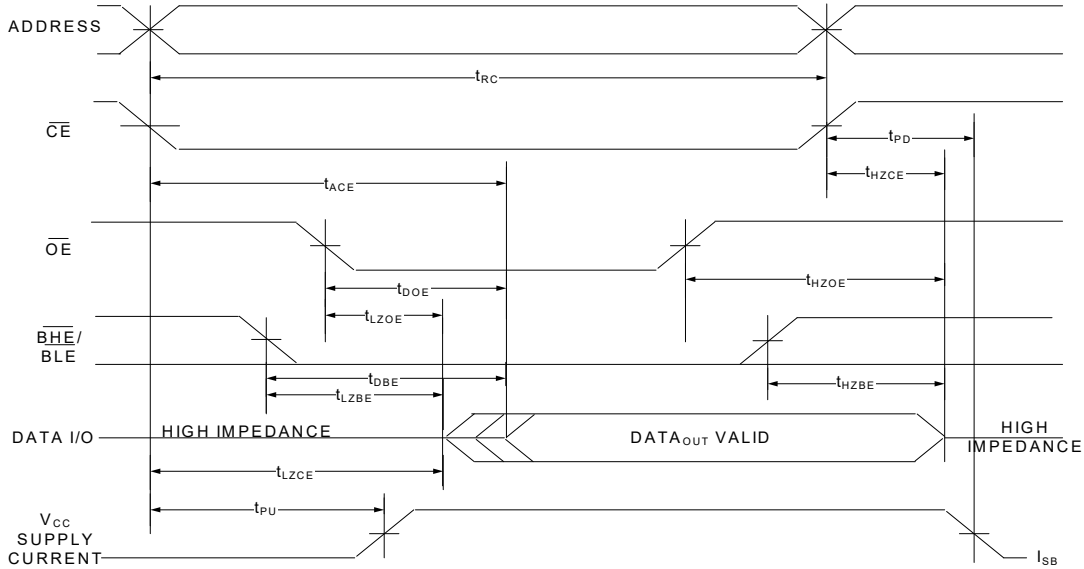
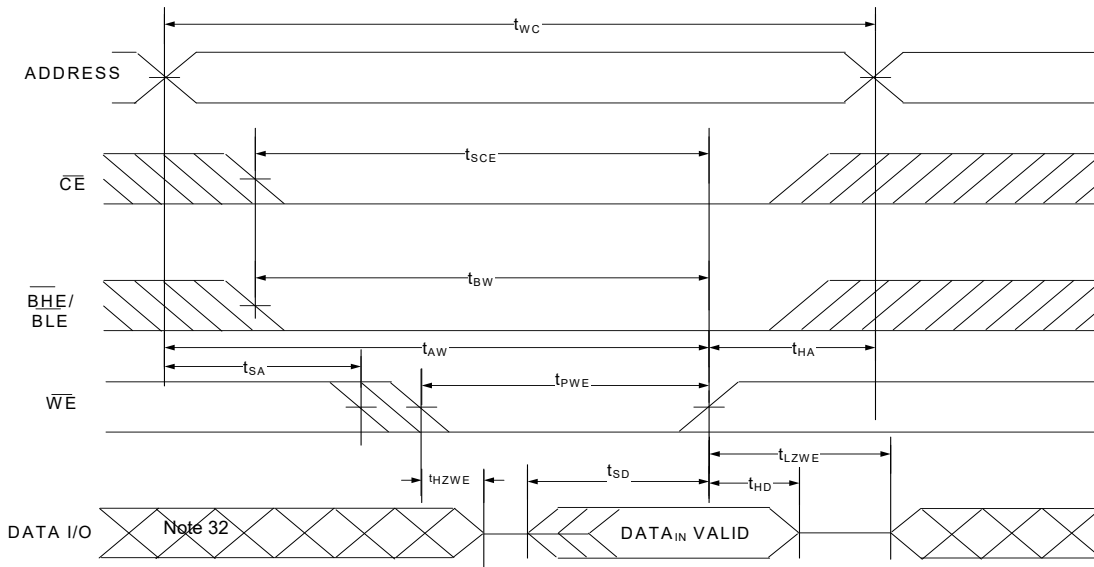


Figure 7. Write Cycle No. 1 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [28, 30, 31, 32]

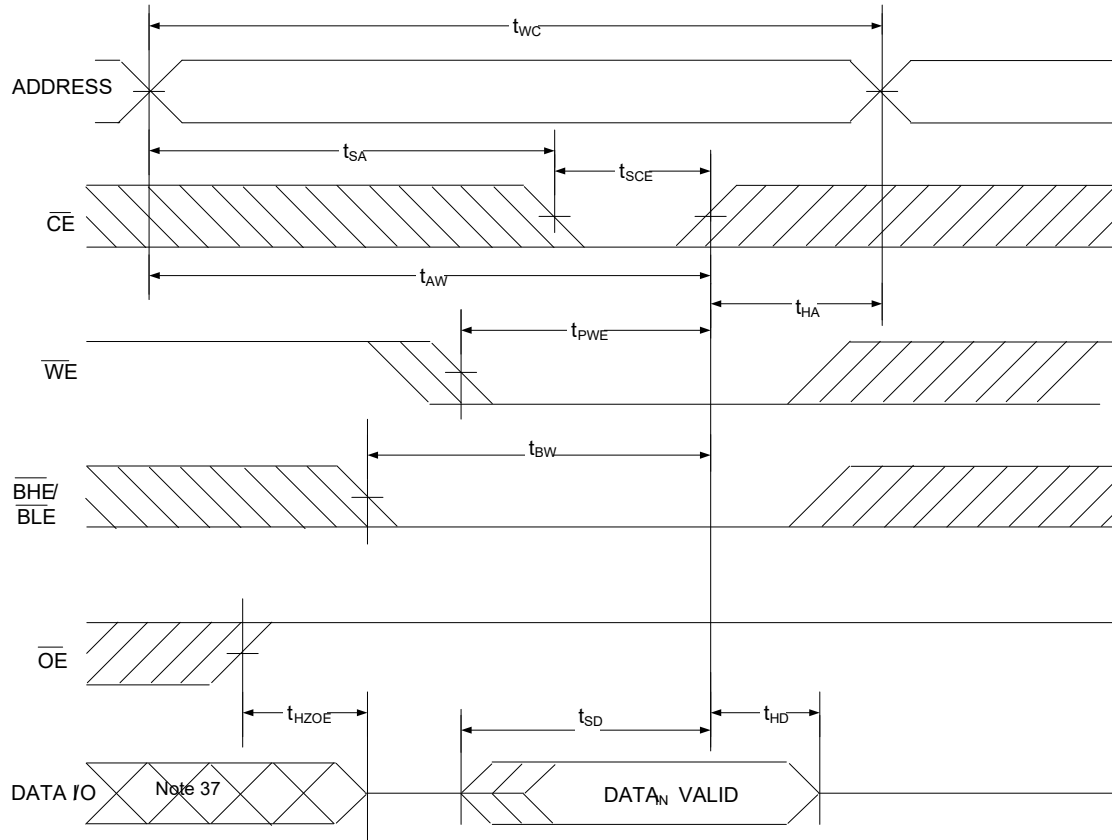


Notes

- 27.  $\overline{WE}$  is HIGH for read cycle.
- 28. For all Dual Chip Enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
- 29. Address valid prior to or coincident with  $\overline{CE}$  LOW transition.
- 30. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  or  $\overline{BLE}$ , or both =  $V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
- 31. Data I/O is in the High-Z state if  $\overline{CE} = V_{IH}$ , or  $\overline{OE} = V_{IH}$ , or  $\overline{BHE}$ , and/or  $\overline{BLE} = V_{IH}$ .
- 32. During this period, the I/Os are in the output state. Do not apply input signals.
- 33. The minimum write cycle pulse width should be equal to the sum of  $t_{HZWE}$  and  $t_{SD}$ .

Switching Waveforms (continued)

Figure 8. Write Cycle No. 2 ( $\overline{CE}$  Controlled) [34, 35, 36]



Notes

- 34. For all Dual Chip Enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
- 35. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  or  $\overline{BLE}$  or both =  $V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write. Any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
- 36. Data I/O is in the High-Z state if  $CE = V_{IH}$ , or  $OE = V_{IH}$ , or  $\overline{BHE}$ , and/or  $\overline{BLE} = V_{IH}$ .
- 37. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 4 ( $\overline{\text{BHE}}/\overline{\text{BLE}}$  Controlled,  $\overline{\text{OE}}$  LOW) [38, 39, 40]

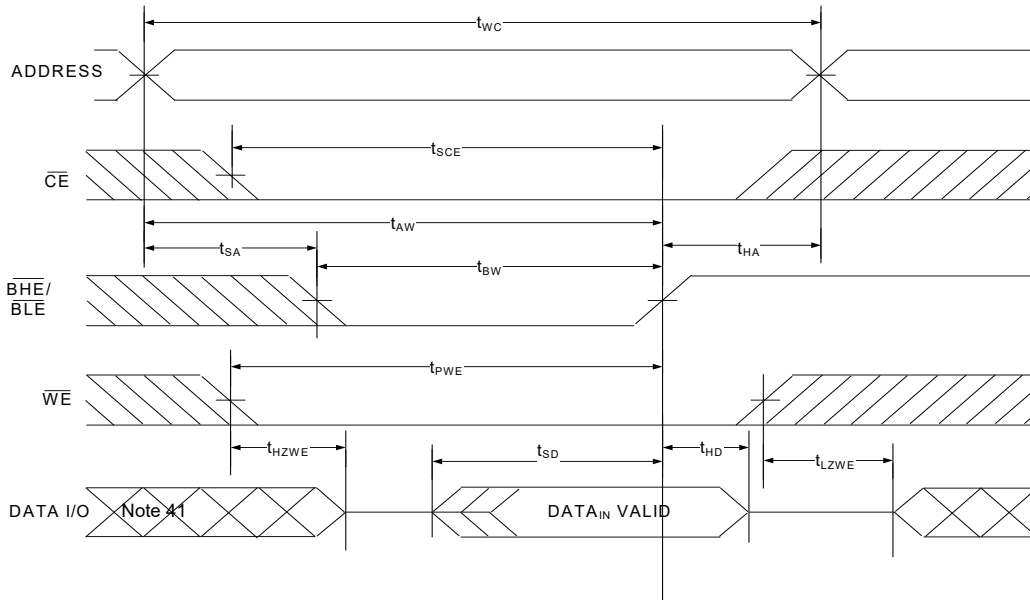
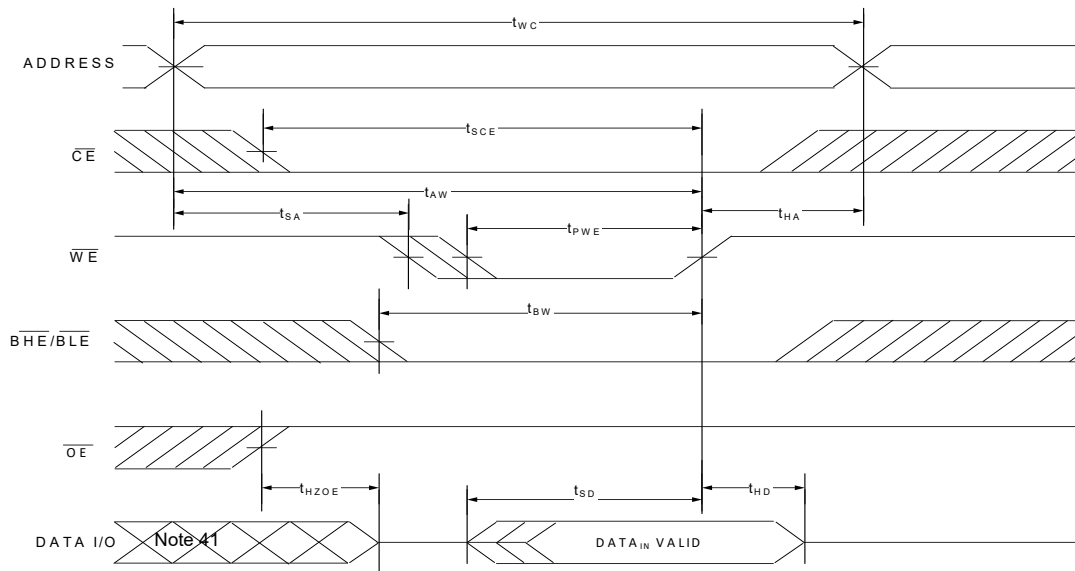


Figure 10. Write Cycle No. 5 ( $\overline{\text{WE}}$  Controlled) [38, 39, 40]



Notes

- 38. For all Dual Chip Enable devices,  $\overline{\text{CE}}$  is the logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH.
- 39. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{\text{IL}}$ ,  $\overline{\text{CE}}_1 = V_{\text{IL}}$ ,  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}}$  or both =  $V_{\text{IL}}$ , and  $\text{CE}_2 = V_{\text{IH}}$ . All signals must be ACTIVE to initiate a write. Any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
- 40. Data I/O is in the High-Z state if  $\overline{\text{CE}} = V_{\text{IH}}$ , or  $\overline{\text{OE}} = V_{\text{IH}}$ , or  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{\text{IH}}$ .
- 41. During this period, the I/Os are in output state. Do not apply input signals.

**Truth Table – CY62187G30**

| $\overline{CE}_1$ | $CE_2$            | $\overline{WE}$ | $\overline{OE}$ | $\overline{BHE}$ | $\overline{BLE}$ | Inputs/Outputs   | Mode                | Power                |
|-------------------|-------------------|-----------------|-----------------|------------------|------------------|--|---------------------|----------------------|
| H                 | X <sup>[42]</sup> | X               | X               | X                | X                | High-Z   | Deselect/Power-down | Standby ( $I_{SB}$ ) |
| X <sup>[42]</sup> | L                 | X               | X               | X                | X                | High-Z   | Deselect/Power-down | Standby ( $I_{SB}$ ) |
| X <sup>[42]</sup> | X <sup>[42]</sup> | X               | X               | H                | H                | High-Z   | Deselect/Power-down | Standby ( $I_{SB}$ ) |
| L                 | H                 | H               | L               | L                | L                | Data Out ( $I/O_0$ – $I/O_{15}$ )                                  | Read                | Active ( $I_{CC}$ )  |
| L                 | H                 | H               | L               | H                | L                | Data Out ( $I/O_0$ – $I/O_7$ );<br>High-Z ( $I/O_8$ – $I/O_{15}$ ) | Read                | Active ( $I_{CC}$ )  |
| L                 | H                 | H               | L               | L                | H                | High-Z ( $I/O_0$ – $I/O_7$ );<br>Data Out ( $I/O_8$ – $I/O_{15}$ ) | Read                | Active ( $I_{CC}$ )  |
| L                 | H                 | H               | H               | L                | H                | High-Z   | Output disabled     | Active ( $I_{CC}$ )  |
| L                 | H                 | H               | H               | H                | L                | High-Z   | Output disabled     | Active ( $I_{CC}$ )  |
| L                 | H                 | H               | H               | L                | L                | High-Z   | Output disabled     | Active ( $I_{CC}$ )  |
| L                 | H                 | L               | X               | L                | L                | Data In ( $I/O_0$ – $I/O_{15}$ )                                   | Write               | Active ( $I_{CC}$ )  |
| L                 | H                 | L               | X               | H                | L                | Data In ( $I/O_0$ – $I/O_7$ );<br>High-Z ( $I/O_8$ – $I/O_{15}$ )  | Write               | Active ( $I_{CC}$ )  |
| L                 | H                 | L               | X               | L                | H                | High-Z ( $I/O_0$ – $I/O_7$ );<br>Data In ( $I/O_8$ – $I/O_{15}$ )  | Write               | Active ( $I_{CC}$ )  |

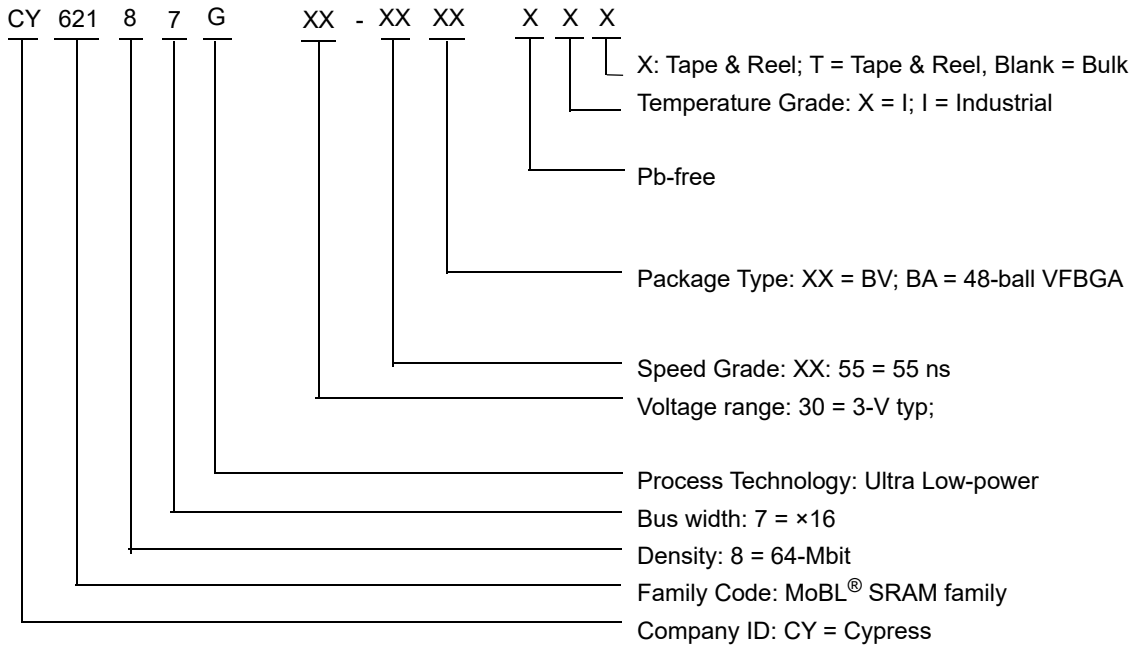
**Note**

42. The 'X' (Don't care) state for the Chip Enables refers to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins are not permitted.

**Ordering Information**

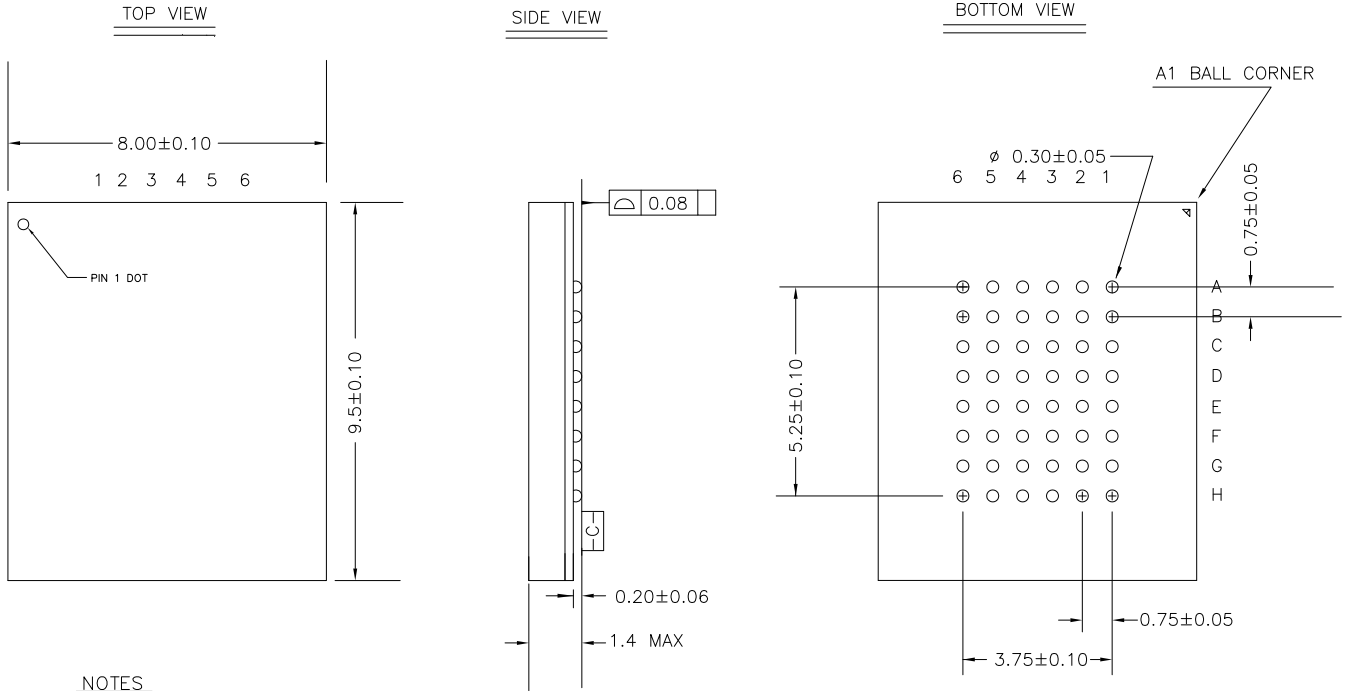
| Speed (ns) | Voltage Range | Ordering Code      | Package Diagram | Package Type (all Pb-free) | Key Features / Differentiators | Operating Range |
|------------|---------------|--------------------|-----------------|----------------------------|--------------------------------|-----------------|
| 55         | 2.2 V–3.6 V   | CY62187G30-55BAXI  | 001-50044       | 48-ball VFBGA              | Dual Chip Enable               | Industrial      |
|            |               | CY62187G30-55BAXIT |                 |                            |                                |                 |

**Ordering Code Definitions**



**Package Diagram**

**Figure 11. 48L FBGA 8 × 9.5 × 1.4 MM BK48L Package Outline, 001-50044**



NOTES

1. REFERENCE JEDEC # MO-205
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-50044 \*D

## Acronyms

**Table 1. Acronyms Used in this Document**

| Acronym                 | Description                             |
|-------------------------|---|
| $\overline{\text{BHE}}$ | Byte High Enable                        |
| $\overline{\text{BLE}}$ | Byte Low Enable                         |
| $\overline{\text{CE}}$  | Chip Enable                             |
| CMOS                    | Complementary metal oxide semiconductor |
| I/O                     | Input/output                            |
| $\overline{\text{OE}}$  | Output Enable                           |
| SRAM                    | Static random access memory             |
| TSOP                    | Thin small outline package              |
| VFBGA                   | Very fine-pitch ball grid array         |
| $\overline{\text{WE}}$  | Write Enable                            |

## Document Conventions

### Units of Measure

**Table 2. Units of Measure**

| Symbol | Unit of Measure |
|--------|-----------------|
| °C     | degree Celsius  |
| MHz    | megahertz       |
| μA     | microampere     |
| μs     | microsecond     |
| mA     | milliampere     |
| mm     | millimeter      |
| ns     | nanosecond      |
| Ω      | ohm             |
| %      | percent         |
| pF     | picofarad       |
| V      | volt            |
| W      | watt            |



**Document History Page**

| Document Title: CY62187G30 MoBL, 64-Mbit (4M words × 16-bit) Static RAM with Error-Correcting Code (ECC)<br>Document Number: 002-24731 |         |                 |   |
|--|---------|-----------------|---|
| Rev.   | ECN     | Submission Date | Description of Change   |
| **   | 6270829 | 08/16/2018      | New datasheet   |
| *A   | 6714290 | 10/30/2019      | Updated maximum standby current value in <a href="#">Features</a> , <a href="#">Product Portfolio</a> , and <a href="#">DC Electrical Characteristics</a> .<br>Updated Icc maximum value in <a href="#">Product Portfolio</a> and <a href="#">DC Electrical Characteristics</a> .<br>Updated Icc @ 1MHz maximum value in <a href="#">DC Electrical Characteristics</a> .<br>Updated <a href="#">Data Retention Characteristics</a> .<br>Added <a href="#">Thermal Resistance</a> values.<br>Added <a href="#">Package Diagram</a> spec 001-50044. |

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