L99VR02J

Datasheet

Automotive linear voltage regulator with configurable output voltage having 500 mA current capability

PowerSSO-12

Product status link
L99VR02J

Product summary	
Order code	**L99VR02JTR**
Package	PowerSSO-12
Packing	Tape and reel

Features

Max. supply voltage (load dump)	V_S	40 V
Max. output voltage tolerance	ΔV_O	+/-2%
Output current	I_O	500 mA
Quiescent current	I_{qn}	≤ 1 µA (1)

1. *Maximum value with regulator disabled*

- AEC-Q100 qualified
- Operating DC power supply voltage range from 2.15 V to 28 V
- Battery and post regulation operating modes are allowed
- Low dropout voltage
- Low quiescent current consumption
- User-selectable output voltage (0.8 V; 1.2 V; 1.5 V; 1.8 V; 2.5 V; 2.8 V; 3.3 V or 5 V)
- Output voltage precision ±2%
- Enable input for enabling/disabling the voltage regulator
- Output voltage monitoring with reset output
- Negligible ESR effect on output voltage stability for load capacitor
- Programmable autonomous watchdog through external capacitor
- Undervoltage lockout UVLO
- Fast output discharge
- Thermal shutdown and short-circuit current limitation
- Advanced thermal warning and output overvoltage diagnostic
- Programmable short-circuit output current
- Wide operating temperature range (T_J = -40 °C to 175 °C)
- Limited documentation available for customers that need support when dealing with ASIL requirements as per ISO 26262

Description

L99VR02J is a low dropout linear voltage regulator designed for automotive applications available in PowerSSO-12 packages. The LDO delivers up to 500 mA of load current. It consumes as low as 1 µA of quiescent current when the regulator is disabled. The input is 40 V tolerant to withstand load dump, while the operating input voltage range is between 2.15 V and 28 V.

The L99VR02J can be configured, through SELx pins, to generate a fixed selectable output voltage (0.8 V; 1.2 V; 1.5 V; 1.8 V; 2.5 V; 2.8 V; 3.3 V or 5 V). High output voltage accuracy (±2%) is kept over wide temperature range, line, and load variation.

The L99VR02J features enable, reset, autonomous watchdog, advanced thermal warning, fast output discharge, and I_{short} control. The regulator output current is internally limited. The device is protected against short-circuit and overload, besides it features over temperature protection. The short current value is configurable by an external resistance.

The L99VR02J can operate both in post regulation, attached to a preregulated voltage or directly connected to the battery.

1 Block diagram and pins description

Figure 1. **Functional block diagram of L99VR02J**

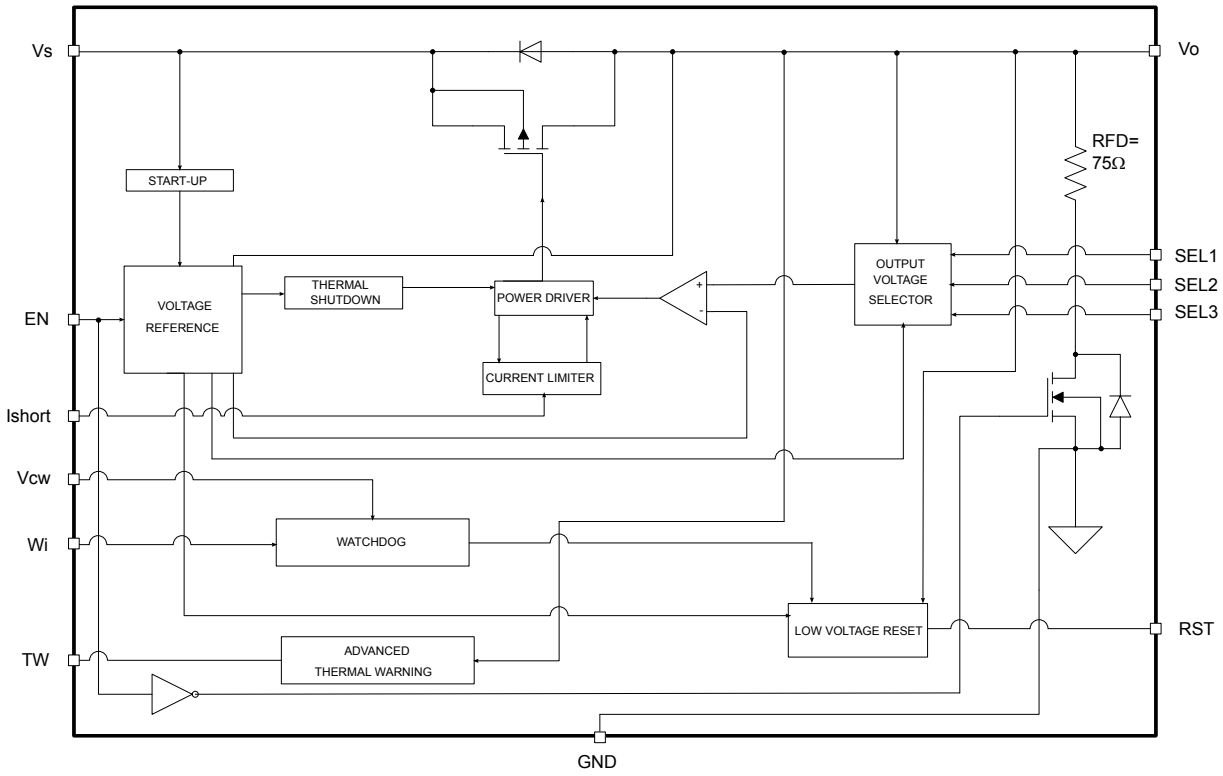
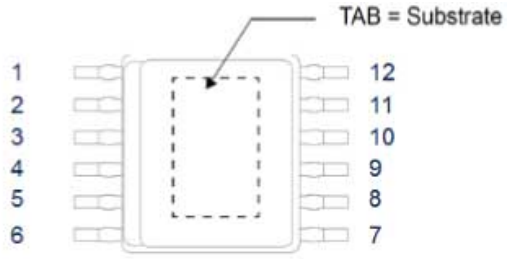


Table 1. Pins description

Pin name	PowerSSO-12 pin	Function
V_S	1	Supply voltage. Block directly to the ground with ceramic capacitor ≥ 4.7 µF and a 100 nF capacitator as close as possible to the pin
SEL1	2	Output voltage selectors.
SEL2	3	
SEL3	4	
TW	5	Advanced thermal warning output. If the device detects a junction temperature above the warning threshold, the pin is pulled low. If an overvoltage condition occurs, a square wave is provided through the TW output. Leave floating if not used.
I_{Short}	6	Programmable short circuit output current input pin. A resistor between Ishort pin and GND sets the short circuit output current value.
EN	7	Enable input: • With the enable high: Regulator, watchdog, and reset are operating • With the enable low: Regulator, watchdog, and reset are shutdown, while the fast discharge circuit is turned on Connect the enable to V_S to keep the device always enabled
GND	8	Ground reference.
V_{CW}	9	Watchdog timer adjusts. A capacitor between V_{CW} pin and GND sets the time response of the watchdog monitor.
Wi	10	Watchdog refresh input. If the square wave frequency at this input pin is too low, a low pulse at an RST pin is generated.
RST	11	Reset output. It is pulled down when the output voltage goes below Vo_th or the frequency at Wi is too low. Leave floating if not used.
V_O	12	Voltage regulator output. Block to ground with a capacitor ≥ 3.3 µF (needed for regulator stability).
TAB	TAB	Connected to ground

Figure 2. Pins configuration



PowerSSO-12

2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the Table 2. Absolute maximum ratings may damage to the device permanently. These are stress ratings only. Operations of the device under conditions above those stated in this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	DC supply voltage	-0.3 to 28	V
V_S	Single pulse / tmax < 400 ms “transient load dump”	40	V
I_S	Input current	internally limited	
V_O	DC output voltage	-0.3 to 6	V
I_O	DC output current	internally limited	
V_{WI}	Watchdog input voltage	-0.3 to V_O + 0.3	V
V_{CW}	Watchdog delay voltage	- 0.3 to V_O + 0.3	V
V_{rst}	Reset output voltage	-0.3 to V_O + 0.3	V
I_{rst}	Reset output current	Internally limited	
V_{tw}	Thermal warning output voltage	-0.3 to V_O + 0.3	V
I_{tw}	Thermal warning output current	Internally limited	
V_{sh_ctrl}	“Short current” control voltage	-0.3 to 3.6	V
V_{EN}	Enable input	-0.3 to V_S + 0.3	V
V_{SELx}	Selectors input voltage	-0.3 to V_S + 0.3	V
VESD HBM	ESD HBM voltage level (HBM-MIL STD 883C)	±2	kV
VESD CDM	ESD CDM voltage level (CDM AEC-Q100-011)	±500	V
	ESD CDM voltage level on corner pins (CDM AEC-Q100-011)	±750	V

2.2 Thermal data

2.2.1 Thermal resistance

Table 3. Operation junction temperature

Item	Symbol	Parameter	Value	Unit
A.001	$R_{thj\text{-}case}$ (1)	Junction to case thermal resistance	8	°C/W
A.002	$R_{thj\text{-}PCB}$ (2)	Junction to PCB thermal resistance	10	°C/W
A.003	$R_{thj\text{-}amb}$ (3)	Junction to ambient thermal resistance	25.5	°C/W

1. *Measured on the bottom.*
2. *Standard JEDEC 51.8.*
3. *Measured on four layers.*

Note: The values quoted are for PCB 77 mm x 86 mm x 1.6 mm, FR4, four layers; Cu thickness 0.070 mm (outer layers). Cu thickness 0.035 mm (inner layers), thermal vias separation 1.2 mm, thermal via diameter 0.3 mm +/-0.08 mm, Cu thickness on vias 0.025 mm, footprint dimension 2.2 mm x 2.9 mm.

2.2.2 Thermal protection

Table 4. Temperature threshold

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A.004	T_{prot} (1)	Thermal protection temperature		175		205	°C
A.005	T_{prot_hyst}	Thermal protection hysteresis			11		°C
A.006	T_J	Operating junction temperature	T_J	-40		175	°C
A.007	T_{stg}	Storage temperature	T_{stg}			150	°C

1. *Thermal protection is guaranteed by design and characterization.*

2.3 Electrical characteristics

Values specified in this section are for V_S = 2.15 V to 18 V, T_J = - 40 °C to +150 °C, unless otherwise stated.

Table 5. Electrical characteristics

Item	Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A.008	V_O	V_O	Output voltage	V_S = 2.15 to 18 V, I_O = 1 to 500 mA, SEL_CONF = [0;0;0]	0.784	0.8	0.816	V
				V_S = 2.15 to 18 V, I_O = 1 to 500 mA, SEL_CONF = [0;0;1]	1.176	1.2	1.224	
				V_S = 2.15 to 18 V, I_O = 1 to 500 mA, SEL_CONF = [0;1;0]	1.470	1.5	1.530	
				V_S = 2.45 to 18 V, I_O = 1 to 500 mA, SEL_CONF = [0;1;1]	1.764	1.8	1.836	
				V_S = 3.15 to 18 V, I_O = 1 to 500 mA, SEL_CONF = [1;0;0]	2.450	2.5	2.550	
				V_S = 3.45 to 18 V, I_O = 1 to 500 mA, SEL_CONF = [1;0;1]	2.744	2.8	2.856	
				V_S = 3.95 to 18 V, I_O = 1 to 500 mA, SEL_CONF = [1;1;0]	3.234	3.3	3.366	
				V_S = 5.65 to 18 V, I_O = 1 to 500 mA, SEL_CONF = [1;1;1]	4.9	5	5.1	
A.009	V_O	I_O	DC output current	V_O = 0.8 V; 1.2 V, 1.5 V; 1.8 V; 2.5 V; 2.8 V; 3.3 V; 5 V			500	mA
A.010	V_O	I_{short}	Short-circuit current lower value(1)	V_S = 4 V for V_O = 3.3 V, V_S = 5.8 V for V_O = 5 V, with I_{short} pin connected to GND	120	220	320	mA
A.011	V_O	I_{short}	Short-circuit current upper value	V_S = 4 V for V_O = 3.3 V, V_S = 5.8 V for V_O = 5 V, with I_{short} pin floating; $I_{short} > I_O$	545	815	1085	mA
A.012	V_S, V_O	$\Delta V_O / V_O$	Static line regulation	V_S is from V_{S_Low}(2) to 18 V, I_O = 1 mA; 250 mA; 500 mA, V_O = 3.3 V; 5 V			1	%

Item	Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A.012	V_S, V_O	ΔV_O / V_O	Dynamic line regulation(3)	V_S is from V_{S_Low}(2) to 18 V, T_r, f = 1 ms; I_O = 1 mA; 250 mA; 500 mA, V_O= 3.3 V; 5 V			3	%
A.013	V_O	ΔV_O / V_O	Static load regulation (4)	I_O = 1 mA to 250 mA, V_O = 3.3 V for V_S = 5 V, V_O = 5 V for V_S = 6 V			1	%
			Dynamic load regulation(3)(4)	I_O = 10 mA to 250 mA, Tr, f = 10 us, V_O = 3.3 V for V_S = 5 V, V_O = 5 V for V_S = 6 V			3	%
A.014	V_S, V_O	V_{dp}	Drop voltage(5)	I_O = 500 mA, V_O = 5 V			500	mV
				I_O = 500 mA, V_O = 3.3 V				
				I_O = 500 mA, V_O = 2.8 V				
				I_O = 500 mA, V_O = 2.5 V				
				I_O = 500 mA, V_O = 1.8 V				
A.015	V_S, V_O	PSRR	Power supply rejection ratio	V_S = 13.5 V, V_O = 5 V, I_O = 500 mA, f = 1 kHz		75(3)		dB
A.016	V_S, V_O	I_{qn}	Current consumption with regulator disabled $I_{qn} = I_{Vs} - I_O$	V_S = 3.5 V; 13.5 V, EN = low			1	µA
A.057	V_S, V_O	I_{qn_LL}	Current consumption with regulator enabled $I_{qn\_LL} = I_{Vs} - I_O$	V_S = 3.5 V; 13.5 V, I_O = 0 µA, EN = high		105	130	µA
A.017	V_S, V_O	I_{qn_0}	Current consumption with regulator enabled $I_{qn\_0} = I_{Vs} - I_O$	V_S = 3.5 V; 13.5 V, 0 < I_O ≤ 60 µA, EN = high		140	180	µA
A.018	V_S, V_O	I_{qn_50}	Current consumption with regulator enabled $I_{qn\_50} = I_{Vs} - I_O$	V_S = 3.5 V; 13.5 V, I_O = 50 mA, EN = high		0.55	0.9	mA
A.019	V_S, V_O	I_{qn_150}	Current consumption with regulator enabled $I_{qn\_150} = I_{Vs} - I_O$	V_S = 3.5 V; 13.5 V, I_O = 150 mA, EN = high		1	1.5	mA
A.020	V_S, V_O	I_{qn_250}	Current consumption with regulator enabled $I_{qn\_250} = I_{Vs} - I_O$	V_S = 3.5 V; 13.5 V, I_O = 250 mA, EN = high		1.05	2	mA
A.021	V_S, V_O	I_{qn_500}	Current consumption with regulator enabled $I_{qn\_500} = I_{Vs} - I_O$	V_S = 3.5 V; 13.5 V, I_O = 500 mA, EN = high		1.4	2.5	mA
A.022	V_S	V_{UVLO_fall}	Undervoltage lockout, falling	V_O= 0.8 V; 1.2 V; 1.5 V; 1.8 V	1.5	1.6	1.7	V
				V_O = 2.5 V; 2.8 V; 3.3 V	2.3	2.4	2.55	
				V_O = 5 V	4.6	4.8	5.0	
A.023	V_S	V_{UVLO_rise}	Undervoltage lockout, rising	V_O = 0.8 V; 1.2 V; 1.5 V; 1.8 V	1.7	1.8	2.1	V
				V_O = 2.5 V; 2.8 V; 3.3 V	2.6	2.7	2.8	
				V_O = 5 V	4.9	5.1	5.3	

1. *I_{Short} typical value of 120 mA for t = 400 µs during the power on.*
2. *V_{S_Low} = 3.5 V at V_O = 0.8 V; 1.2 V;1.5 V;1.8 V and 2.5 V, V_{S_Low} = 5 V at V_O= 2.8 V and 3.3 V, V_{S_Low}= 6 V at V_O = 5 V*

3. *Parameters are guaranteed by design.*
4. *Referred to Section 3.1 .*
5. *Considering that the minimum operating input voltage is 2.15 V, the dropout voltage (V_{dp}) is not defined for output voltages below 1.8 V.*

Table 6. Fast output discharge

Item	Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A.024	V_O	R_{FD}	Fast discharge - pull down resistor	V_S = 3.95 V; 13.5 V, V_O = 3.3 V; 5 V, EN = low	50	75	120	Ω

Table 7. Reset

Item	Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A.025	RST	V_{rst_l}	Reset output low voltage	V_S = 5 V; 13.5 V, R_{ext} ≥ 4.7 KΩ to V_O, V_O = 3.3 V; 5 V			0.2 x V_O	V
A.026	RST	I_{rst_lkg}	Reset output high leakage current	V_{rst} = 0.8 V			1	µA
A.027	RST	V_{O_th}	V_O out of regulation, low threshold	V_S = 5 V, 13.5 V, V_O decreasing, V_O = 3.3 V; 5 V	13.5%	10%	6.5%	Below V_O
A.055	RST	$V_{O\_th\_hyst}$	V_O out of regulation– low threshold hysteresis	V_S = 5 V; 13.5 V, V_O increasing, V_O = 3.3 V; 5 V		2%		V_{O_th}
A.028	RST	T_{rr}	Reset reaction time	V_S = 5 V; 13.5 V, V_O = 3.3 V; 5 V	10	16	37	µs
A.029	RST	T_{rd}	Reset delay time	V_S = 5 V; 13.5 V, V_O = 3.3 V; 5 V	160(1)	250	310	µs

1. *T_{rd} = 120 µs for V_S < 3.5 V.*

Table 8. Watchdog

Item	Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A.030	W_i	V_{ih}	Input high voltage (1)	V_S = 5 V; 13.5 V, V_O = 3.3 V; 5 V	0.7 x V_O			V
A.031	W_i	V_{il}	Input low voltage (1)	V_S = 5 V; 13.5 V, V_O = 3.3 V; 5 V			0.25 x V_O	V
A.032	W_i	I_{Wi}	Pull down current	V_{wi} = 3.3 V		6	10	µA
A.033	V_{CW}	V_{wlth}	Low threshold	V_S = 5 V; 13.5 V, V_O = 3.3 V; 5 V	10%	13%	16%	V_O
A.034	V_{CW}	V_{whth}	High threshold	V_S = 5 V; 13.5 V, V_O = 3.3 V; 5 V	44%	47%	50%	V_O
A.035	V_{CW}	I_{CWc}	Charge current	V_S = 5 V; 13.5 V, V_{CW} = 0.1 V, V_O = 3.3 V; 5 V	5	10	20	µA
A.036	V_{CW}	I_{CWd}	Discharge current	V_S = 5 V; 13.5 V, V_{CW} = 2.5 V, V_O = 3.3 V; 5 V	1.25	2.5	5	µA
A.040	V_O	I_{w_off}	Watchdog deactivation current threshold	V_S = 5 V; 13.5 V, V_O = 3.3 V; 5 V	0.4	1.05	1.5	mA
A.041	V_O	I_{w_on}	Watchdog activation current threshold	V_S = 5 V; 13.5 V, V_O = 3.3 V; 5 V	1.8	3.35	4.8	mA

1. *Watchdog input requires a square wave signal (duty cycle of 50 %).*

Table 9. Enable

Item	Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A.042	EN	V_{EN_low}	EN input low voltage				0.6	V
A.043	EN	V_{EN_high}	EN input high voltage		1.5			V
A.045	EN	I_{EN}	Pull down current	V_S = 13.5 V		4	12	µA

Table 10. Output voltages selectors

Item	Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A.046	SELx	V_{SELx_low}	SELx input low voltage				0.3	V
A.047	SELx	V_{SELx_high}	SELx input high voltage		0.7			V
A.048	SELx	I_{SELx}	Pull down current	V_S = 3.5 V; 13.5 V		0.1	0.4	µA

Table 11. Thermal warning and protection

Item	Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A.049	TW	V_{Tw_low}	Thermal warning output low voltage	$R_{ext} \geq 4.7$ kΩ to V_O, V_O = 3.3 V; 5 V			0.2 x V_O	V
A.050	TW	T_{warn}	Thermal warning temperature		140	150	165	°C
A.051	TW	T_{warn_hyst}	Thermal warning hysteresis		3	11	15	°C
A.052	V_O	OV	V_O overvoltage	V_S = 5 V; 13.5 V, V_O increasing, V_O = 3.3 V; 5 V	6.5%	10%	13.5%	Above V_O
A.056	V_O	$OV_{\_hyst}$	V_O overvoltage hysteresis	V_S = 5 V; 13.5 V, V_O decreasing, V_O = 3.3 V; 5 V		2%		Below OV
A.054	TW	T_{w_per}	Thermal warning square wave period	V_S = 5 V; 13.5 V, V_O = 3.3 V; 5 V	160(1)	250	335	µs

1. *T_{w_per} = 130 µs for V_S < 3.5 V.*

Note: All parameters are guaranteed in the junction temperature range -40°C to 150 °C (unless otherwise specified). L99VR02J device is still operative and functional at higher temperatures (up to 175 °C). Parameters limit at junction temperature above 150 °C may change respect to what is specified as per the standard temperature range. Device functionality at high junction temperature is guaranteed by characterization. All parameters are guaranteed by design for V_O not reported in test condition.

Note: Minimum input voltage values are achievable adopting an input ceramic capacitator: C5750X7R2A475M230KA– ceramic capacitor multistrate SMD, 4.7 µF, 100 V, ±20%, X7R, C series TDK.

2.4 Electrical characteristics curves

Figure 3. Output voltage vs T_j

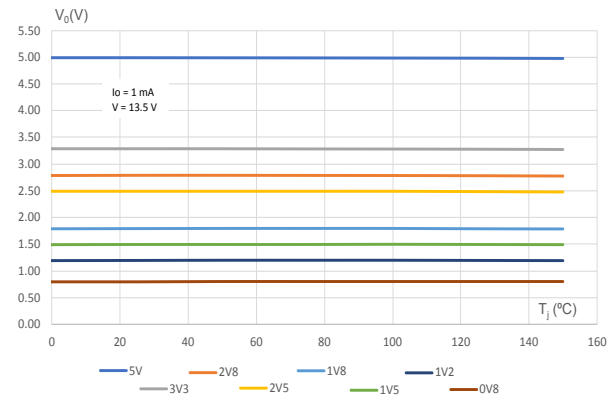


Figure 4. Output voltage vs V_S

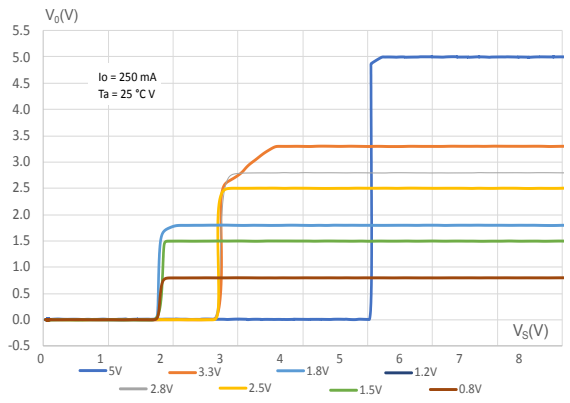


Figure 5. Drop voltage vs output current

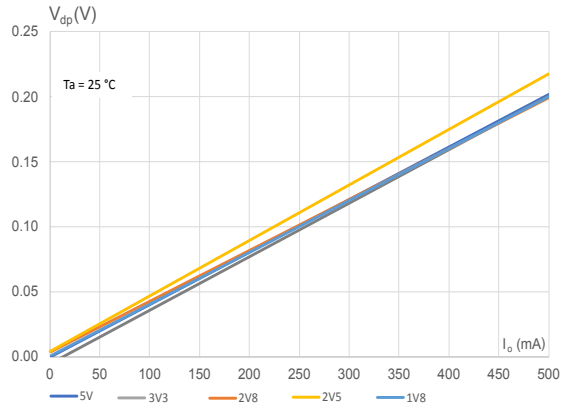


Figure 6. Current consumption vs output current

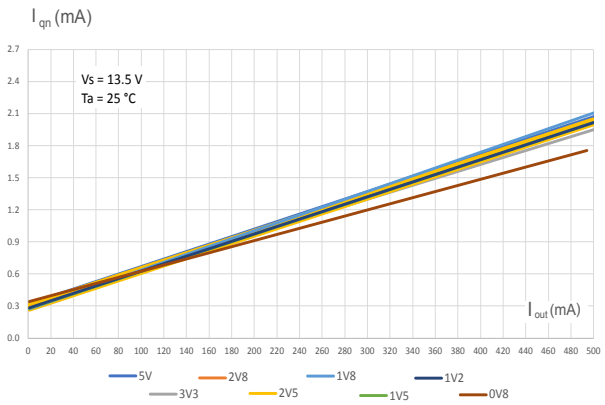


Figure 7. Current consumption vs input voltage (I_o < 1 mA)

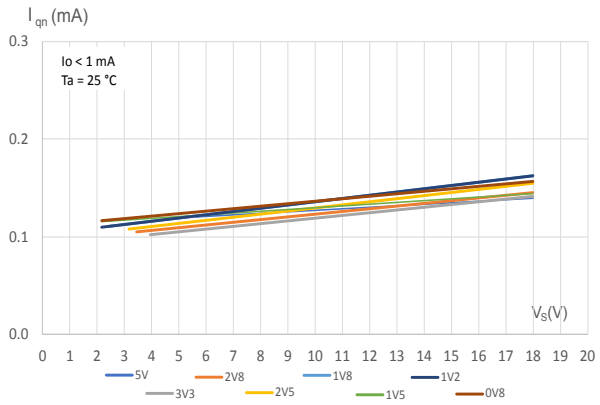


Figure 8. Current consumption vs input voltage (I_o = 50 mA)

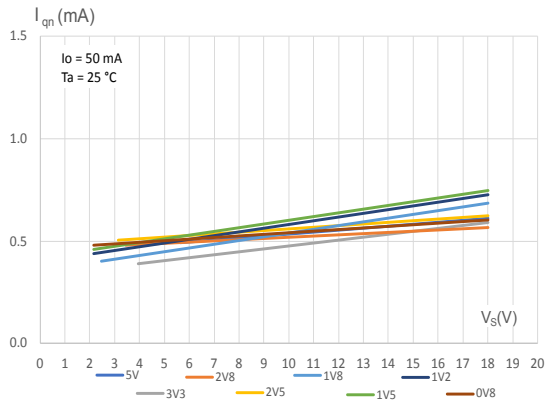


Figure 9. Current consumption vs input voltage (I_o = 250 mA)

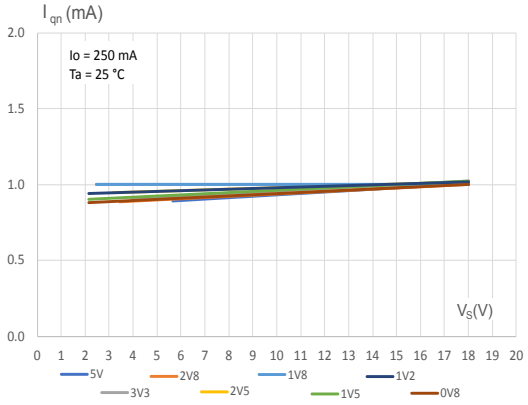


Figure 10. Short-circuit current vs T_j (I_{short} pin tied to GND)

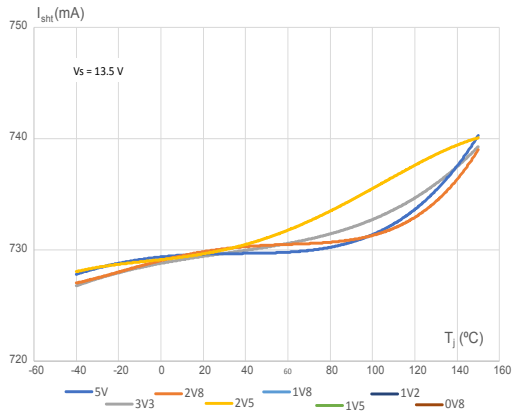


Figure 11. Short-circuit current vs T_j (I_{short} pin floating)

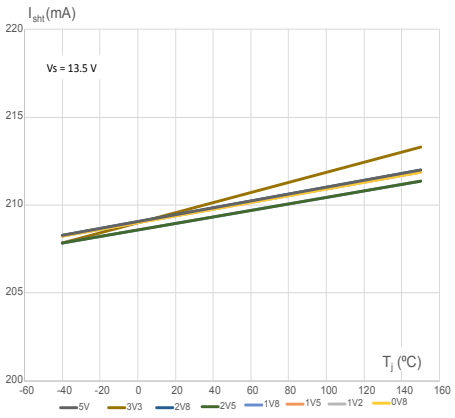


Figure 12. Short-circuit current vs input voltage

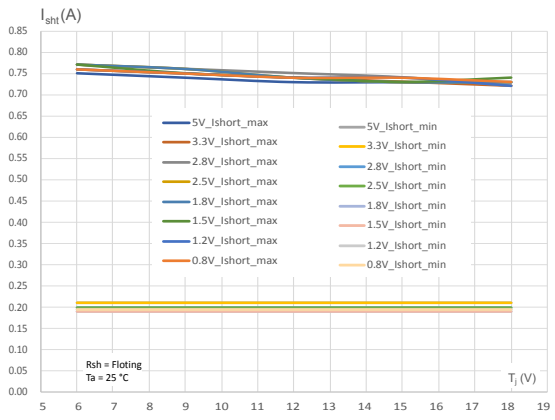


Figure 13. Output voltage vs enable voltage (V_O = 0.8 V)

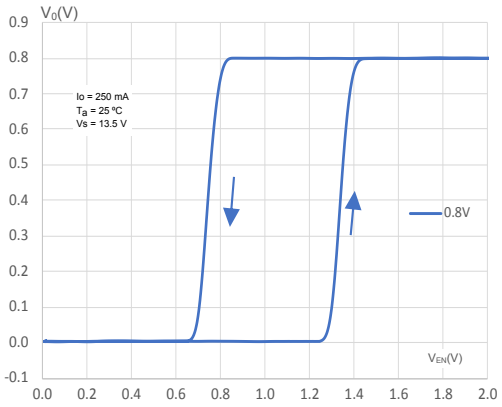


Figure 14. Output voltage vs enable voltage (V_O = 1.2 V)

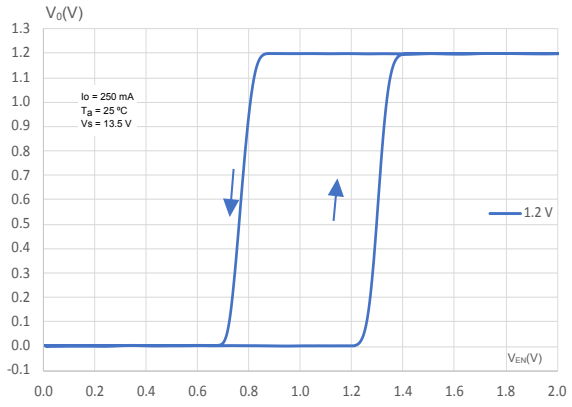


Figure 15. Output voltage vs enable voltage (V_O = 1.5 V)

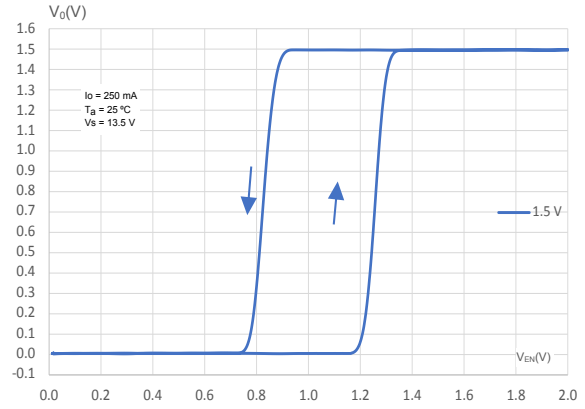


Figure 16. Output voltage vs enable voltage (V_O = 1.8 V)

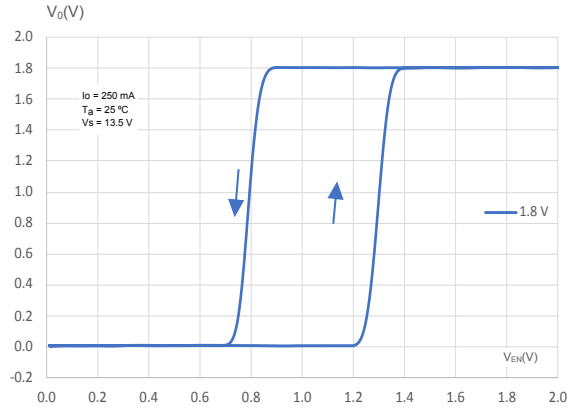


Figure 17. Output voltage vs enable voltage (V_O = 2.5 V)

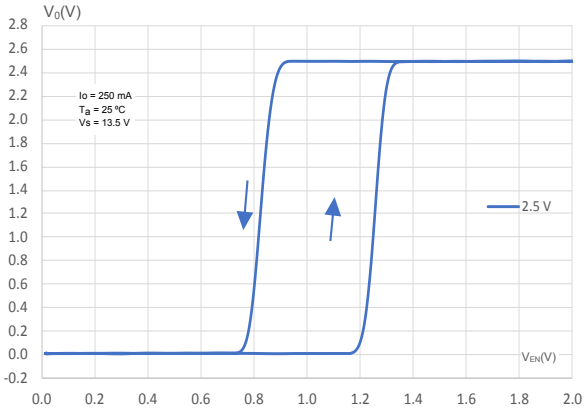


Figure 18. Output voltage vs enable voltage (V_O = 2.8 V)

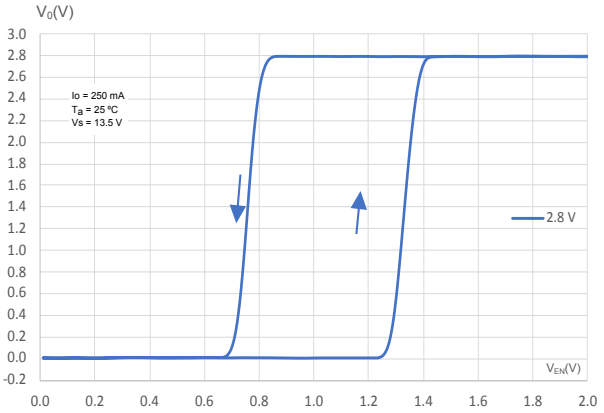


Figure 19. Output voltage vs enable voltage (V_O = 3.3 V)

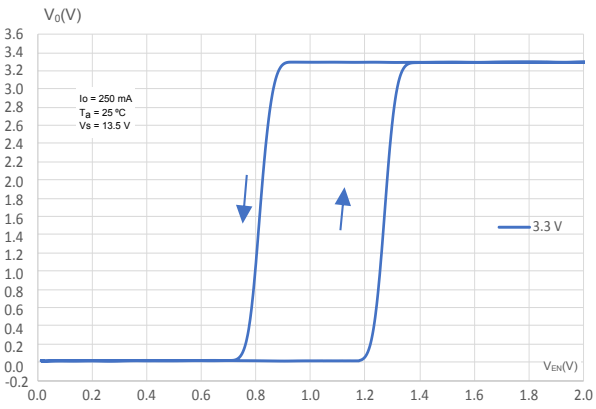


Figure 20. Output voltage vs enable voltage (V_O = 5 V)

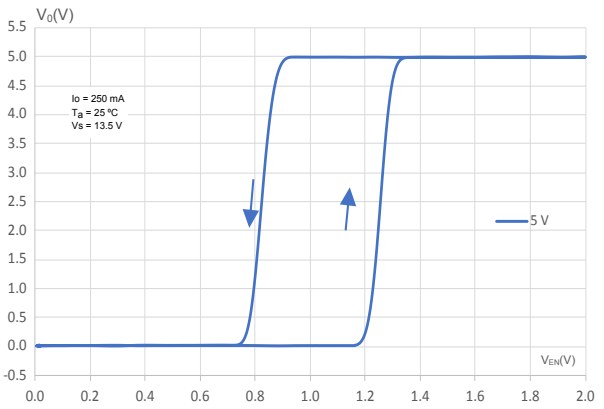


Figure 21. V_{EN_high} vs T_j

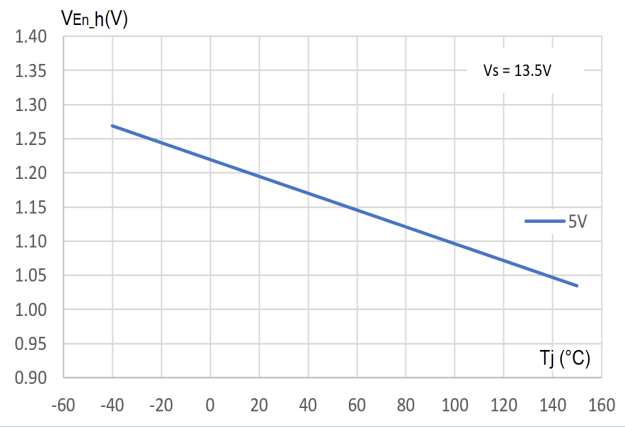


Figure 22. V_{EN_low} vs T_j

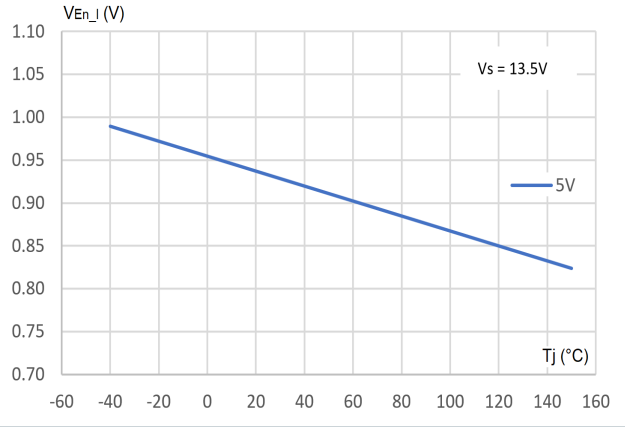


Figure 23. V_{whth} vs T_j

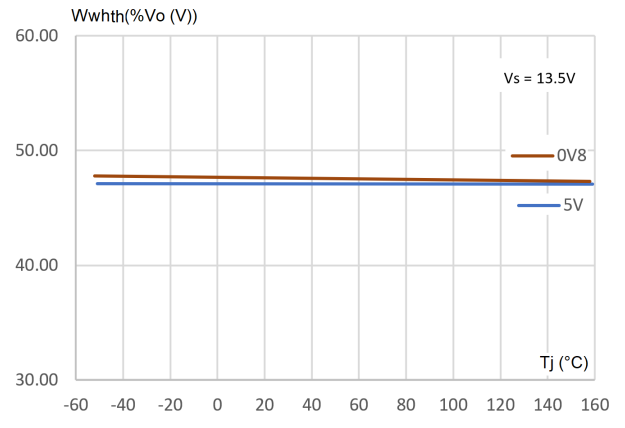


Figure 24. V_{wlth} vs T_j

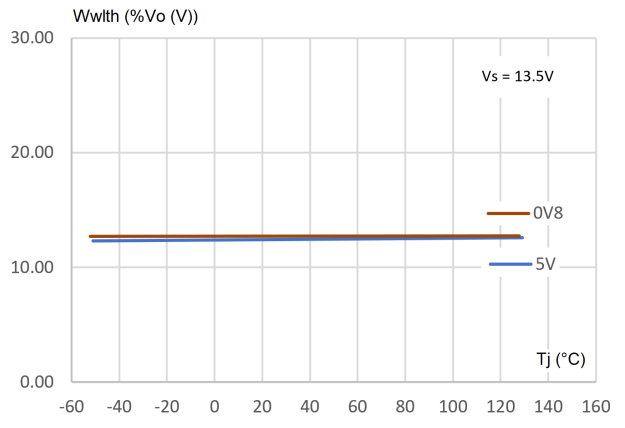


Figure 25. I_{CWc} vs T_j

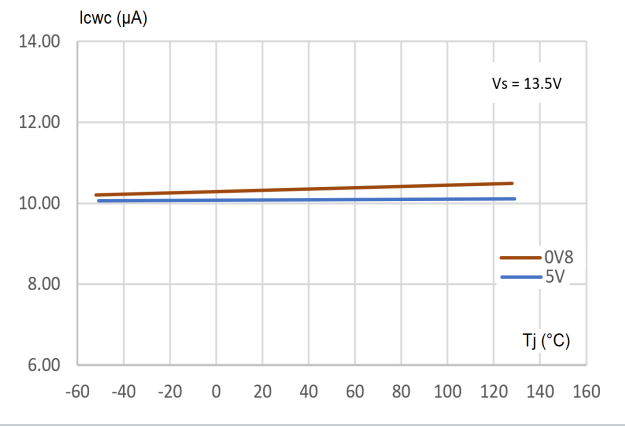


Figure 26. I_{CWd} vs T_j

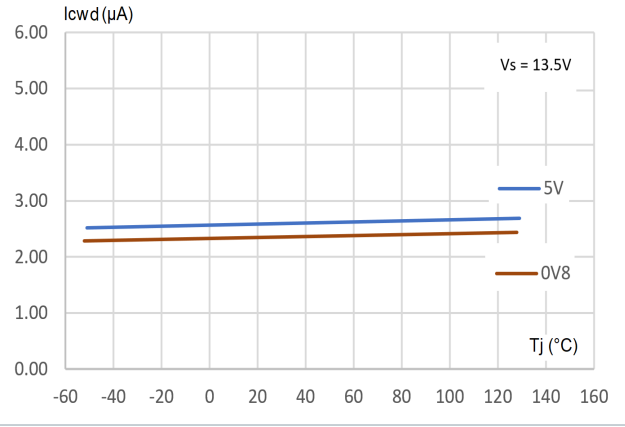
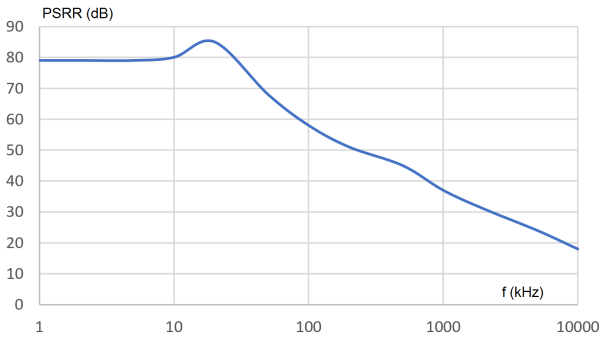


Figure 27. **PSRR**



3 Test circuit and waveforms plot

3.1 Load regulation

Figure 28. **Load regulation test circuit**

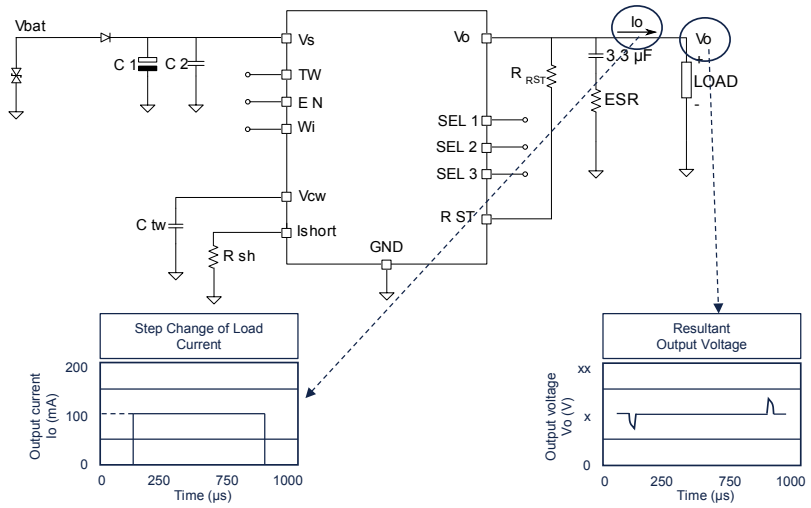


Figure 29. **Maximum load variation response (V_o = 5 V)**

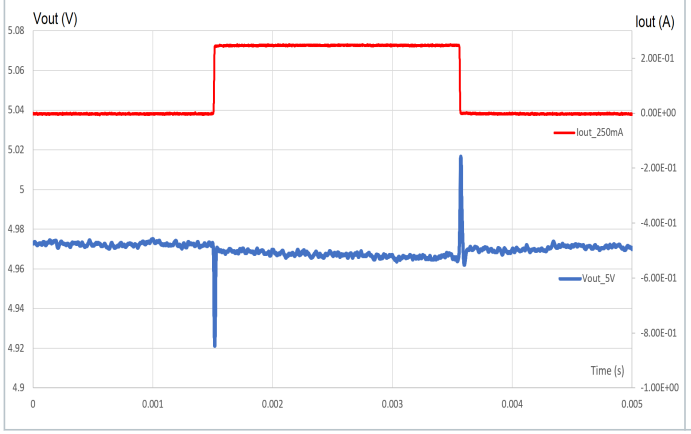
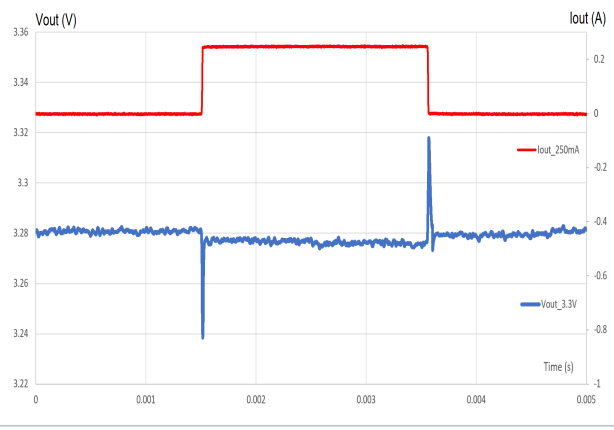


Figure 30. **Maximum load variation response (V_o = 3.3 V)**



4 Application information

Figure 31. **Application schematic**

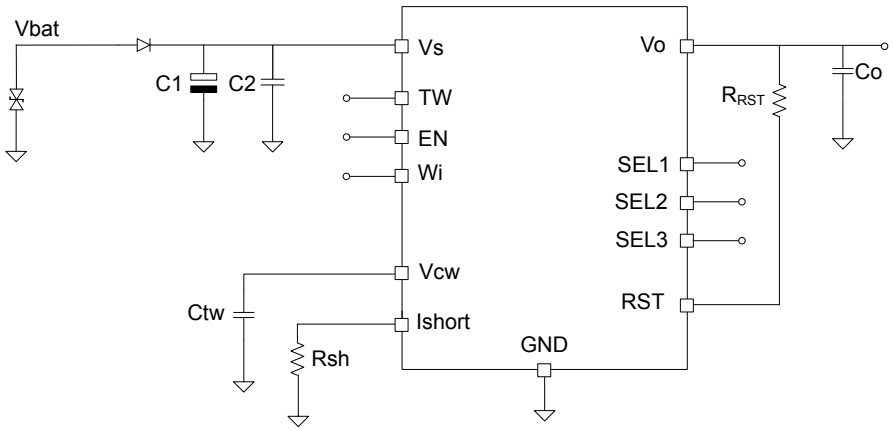
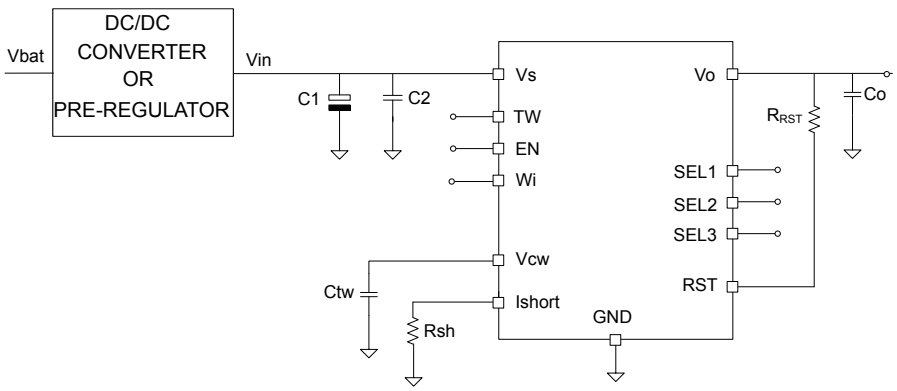


Figure 32. **Application schematic – Post regulation**



Input ceramic capacitor $C_2 \geq 4.7$ µF is necessary for the regulator to operate properly. The other input capacitor C1 can be used as backup supply for the application. The C_O capacitor, connected to the output pin, is for bypassing to GND the high-frequency noise and it guarantees stability even during sudden line and load variations.

Suggested value is $C_O = 3.3$ µF.

The ESR of the SMD output ceramic capacitor has a negligible effect on the stability of the L99VR02J for capacitors with low ESR. A ceramic SMD capacitor is recommended on the V_O pin.

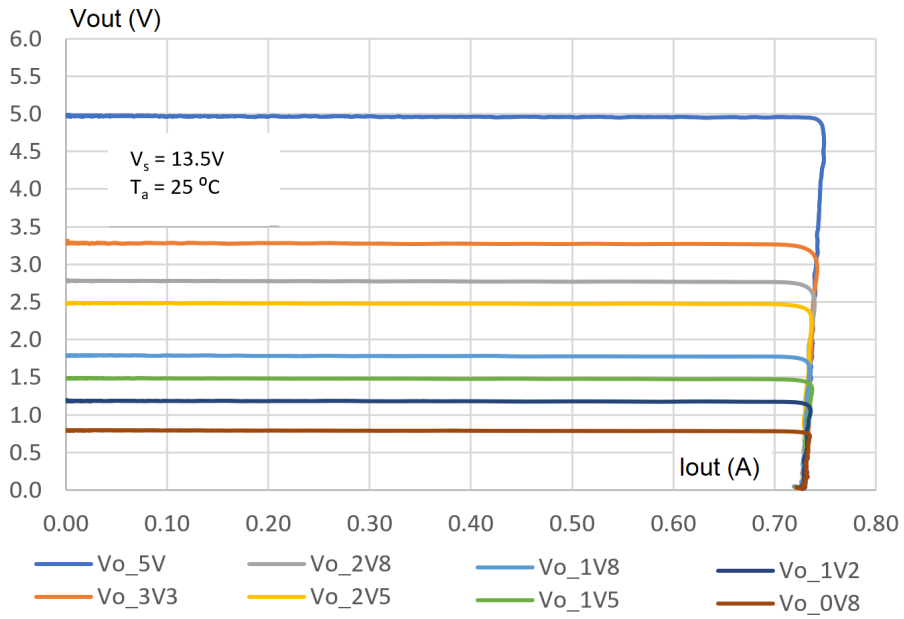
4.1 Voltage regulator

The voltage regulator uses a p-channel MOS transistor as a regulating element. With this structure, a very low dropout voltage at current up to I_O = 500 mA is obtained. The high-precision of the output voltage (±2%) is obtained with a pretrimmed reference voltage. The voltage regulator automatically adapts its own quiescent current to the output current level. In light load conditions, the quiescent current goes down to I_{qn_LL} = 105 µA (low consumption mode). L99VR02J operates with reduced input voltage (post regulation) minimizing the internal power dissipation and maximizing the output current.

4.2 Output current limitation

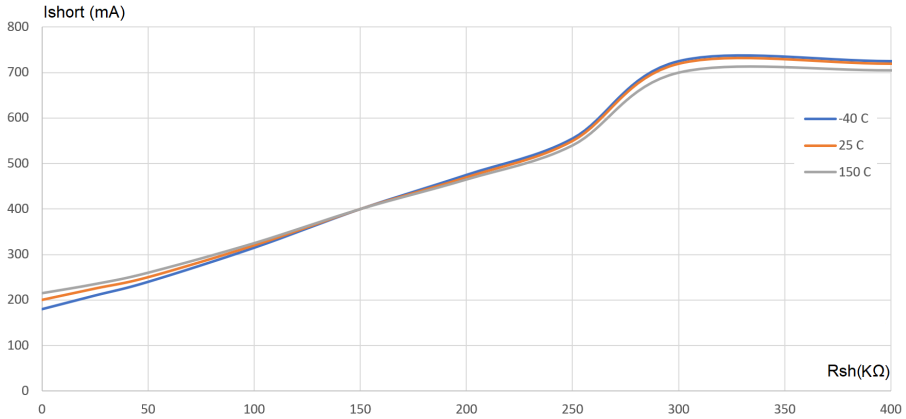
Output current limitation is present to protect the regulator and the application from the overload condition, such as short to ground.

Figure 33. Behavior of output current versus regulated voltage V_O



The I_{short} current can be set in the range from 220mA (typ) to 815mA (typ). This through an external resistor R_{sh} connected between the I_{short} pin and the ground.

Figure 34. I_{short} versus R_{sh}



Open pin (no resistance on the I_{short} pin), is seen as a max resistance corresponding to the maximum I_{short} current.

4.3 Output voltage selection

The L99VR02J can provide one out of eight different output voltages. The combination of three digital input selectors (SELx) determines the output voltage according to the following Table 12.

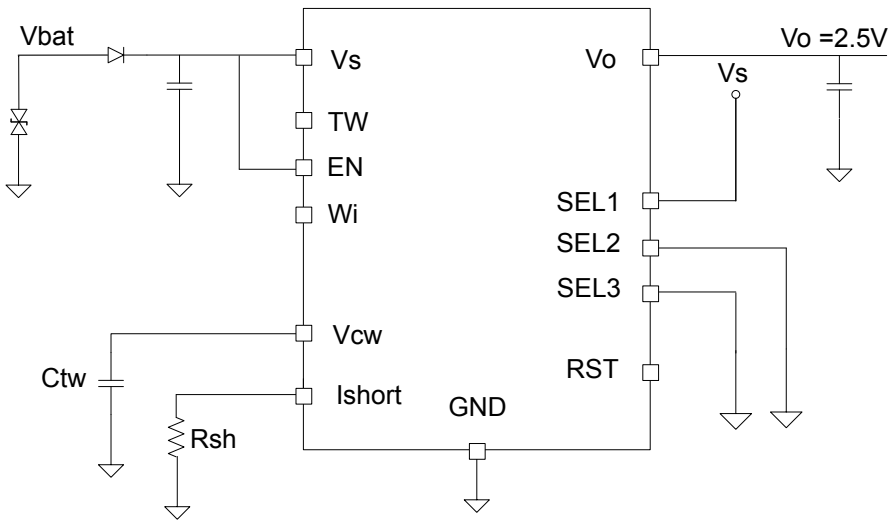
Table 12. Truth table

V_O	SEL1	SEL2	SEL3
5	1	1	1
3.3	1	1	0
2.8	1	0	1
2.5	1	0	0
1.8	0	1	1
1.5	0	1	0
1.2	0	0	1
0.8 (default)	0	0	0

The SELx pins configuration is acquired at the device startup (EN transition from low to high) and once configuration is acknowledged. It cannot be changed until the next EN transition.

When all the pins are left not connected, the default configuration is selected.

Figure 35. Example of output voltage selection



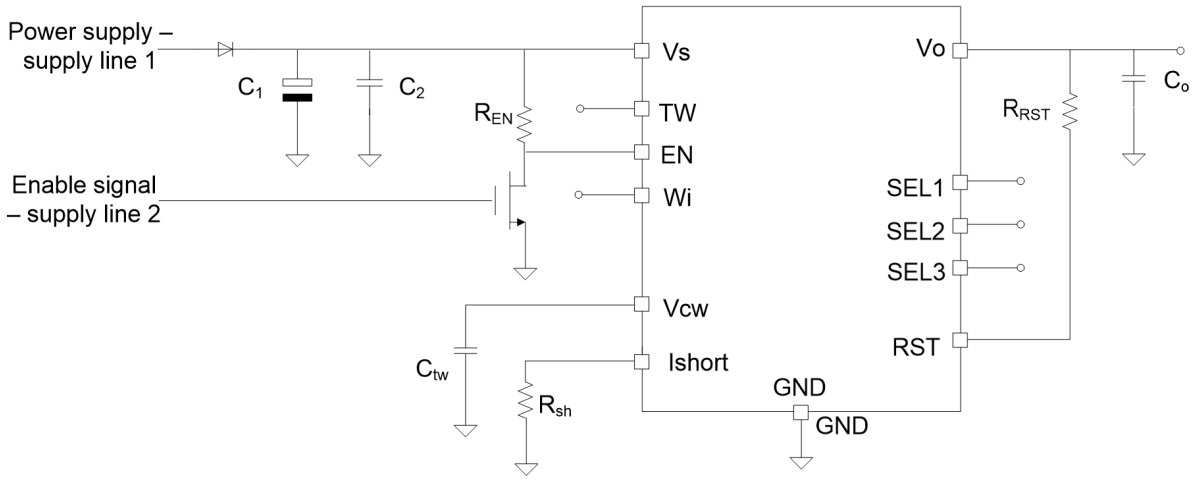
SELx pins are internally connected to GND via the pull-down current source.

4.4 Enable

The L99VR02J is enabled/disabled by the enable input; a high voltage signal switches the regulator ON. When the enable pin is set low, the output is switched-off. The current consumption of the device becomes as low as 1 µA and the fast output discharge circuit is activated.

It may happen that the components drive the enable pin supplied at a voltage different from the regulator supply voltage. In this case, the EN input pin must be set high only once V_S > 1.5 V. A solution to drive the enable pin is depicted in the Figure 36.

Figure 36. Typical example of enable control

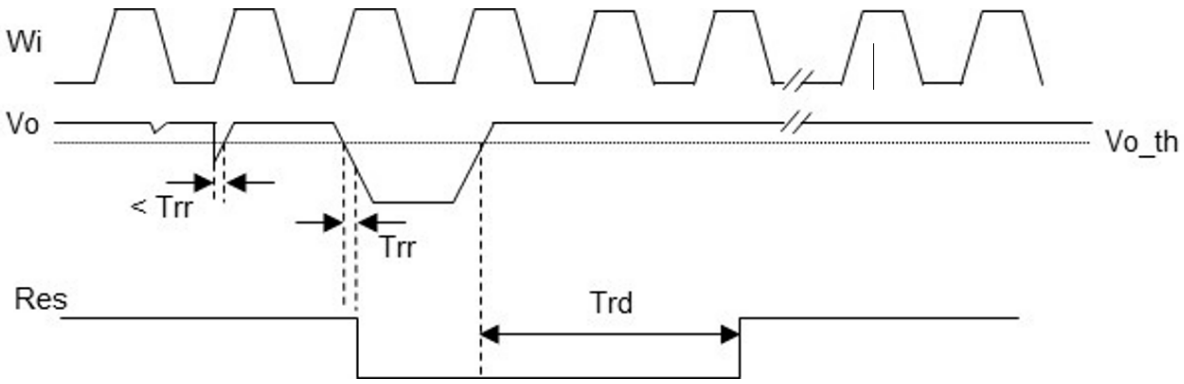


In any case, to avoid exceeding the absolute maximum rating, a special care must be adopted in driving the EN pin since the enable input voltage is linked to the maximum DC supply voltage (V_S) applied to the L99VR02J (-0.3 V to V_S + 0.3 V).

4.5 Reset

The reset circuit supervises the output voltage V_O. If the output voltage falls below V_{O_th}, then RST is pulled low with a reaction time T_{rr}. When the output voltage rises above, V_{O_th}+ $V_{O\_th\_hyst}$ then RST is pulled high with a delay time T_{rd}. An internal circuit generates the delay. The reset circuit is active when EN is high. Being RST an open-drain output an external resistance (R_{rst}) is needed between the RST pin and the V_O pin. The external resistance value can be in a range between 4.7 KΩ and 20 KΩ. Leave the RST pin floating if not used. Be aware that the current flowing through the RST pin drawn from V_O when the RST pin is pulled low. It may affect the watchdog activation/deactivation based on the regulator output current consumption monitoring.

Figure 37. Reset timing diagram



4.6 Autonomous watchdog

The watchdog input W_i monitor a supplied microcontroller. If pulses are missing, the RST output pin is set low. The watchdog timeout can be set within a wide range with the external capacitor, C_{tw}. The watchdog circuit discharges the capacitor C_{tw}, with the constant current I_{CWd}. If the lower threshold V_{wlth} is reached, a watchdog reset is generated. To avoid it, the microcontroller must generate a positive edge during the discharge of the capacitor before the voltage reaches the threshold V_{wlth}. To calculate the sawtooth period "T_{wop}", taking care that the microcontroller triggers the positive edge during the discharge phase of C_{tw} (T_d). The following equations can be used:

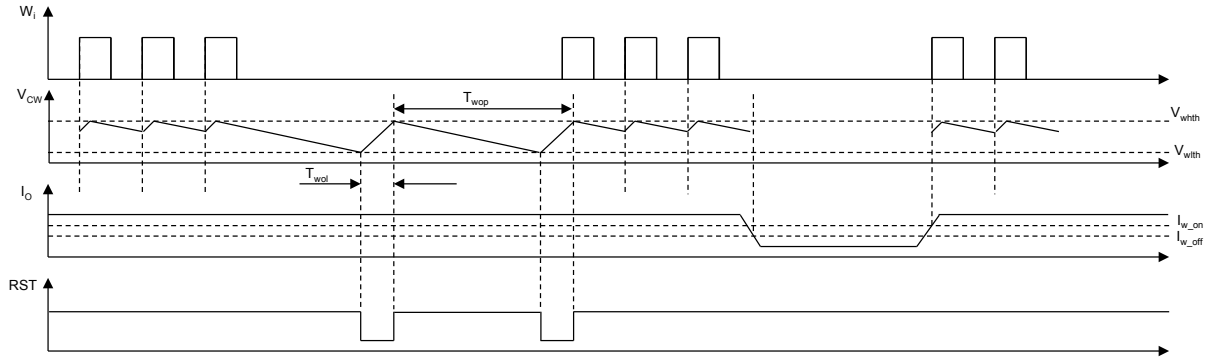
$$(V_{whth} - V_{wlth}) \times C_{tw} = I_{CWd} \times T_d$$

$$(V_{whth} - V_{wlth}) \times C_{tw} = I_{CWc} \times T_{wol}$$

$$T_{wop} = T_d + T_{wol}$$

Every W_i positive edge switches the current source from discharging to charging. The same happens when the lower threshold is reached. When the voltage reaches the upper threshold, V_{whth}, the current switches from charging to discharging. The result is a saw-tooth voltage at the watchdog timer capacitor C_{tw}. If a microcontroller operates in low power mode, it is not able to generate any pulse to refresh the voltage regulator watchdog, triggering so the microcontroller reset. In such a case, the watchdog functionality is automatically deactivated anytime the microcontroller current consumption falls under the I_{w_off} threshold. This to avoid generating the microcontroller reset. On the other hand, when the current consumption rises above the I_{w_on} threshold the watchdog functionality is once again activated. Once the regulator is enabled for the first time, if $I_O < I_{w\_off}$, the watchdog is not activated. While if $I_O > I_{w\_off}$, the watchdog is activated.

Figure 38. Watchdog timing diagram



Since the RST output pin is shared by the watchdog circuit and the output voltage monitoring circuit, for applications where the watchdog is not needed, to prevent the watchdog from generating RST pulses without anyhow losing the reset functionality of the V_O monitoring, the V_{cw} pin has to be connected to V_O. V_{cw} pin must be always tied to ground by an external capacitor (C_{tw}) when watchdog function is used.

Note: when the watchdog timer is used and the regulator recovers from a thermal shut-down event or recovers from an output under-voltage event (including the recovery from output under-voltage event at the regulator output turning on), the reset pin might be pulled back high with a delay longer than T_{rd}, in the range between T_{rd} and T_{rd} +T_{wol} due to the watchdog that might affect the RST pin release. The watchdog will not affect the RST pin release in the case where recovering from a thermal shut-down event or recovering from an output under-voltage event (including the recovery from output under-voltage event at the regulator output turning on) the I_O drops below I_{w_off} before T_{rd}. The output current I_O consists in the load current, the current drawn from the RST pin and the TW pin through the pull-down resistors connected to V_O when the RST and the TW pins are asserted low and the current needed to charge/discharge the output capacitor C_O.

Note: When the watchdog timer is used, in the case of an output under-voltage event not making the V_O drop to zero volt, since the watchdog will still be running during the output under-voltage condition, the first watchdog timeout after the reset pin is released coming out of the output under-voltage event might occur before expected ($0 \le$ timeout $\le T_{wop} - T_{wol}$).

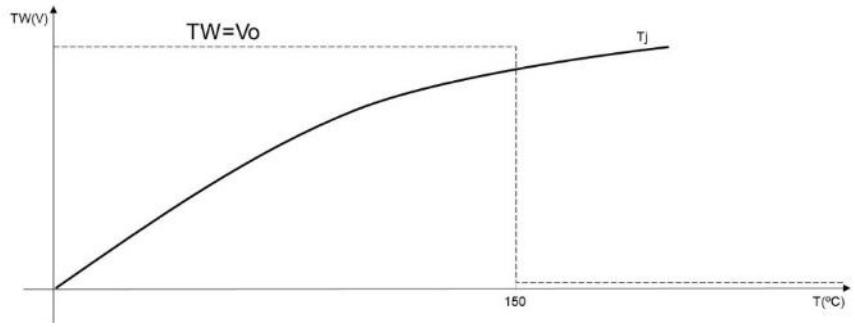
Table 13. **Watchdog timer**

Usage of watchdog timer	Connection of V_{CW} pin
Watchdog timer is not used	Connect to the V_O pin
Watchdog timer is used	Connect to an external capacitor C_{tw}

4.7 Thermal warning and thermal shutdown

To warn the microcontroller about a severe temperature increase, a thermal warning output has been implemented. If the device detects a junction temperature above T_{warn}, the advanced thermal warning (TW) output pin is pulled low while the voltage regulator, and its features remain all active. The TW pin returns to its high logic level (equal to the V_O output value) once the temperature falls below the threshold T_{wam} - T_{wam_hyst}.

Figure 39. **Thermal warning diagram**

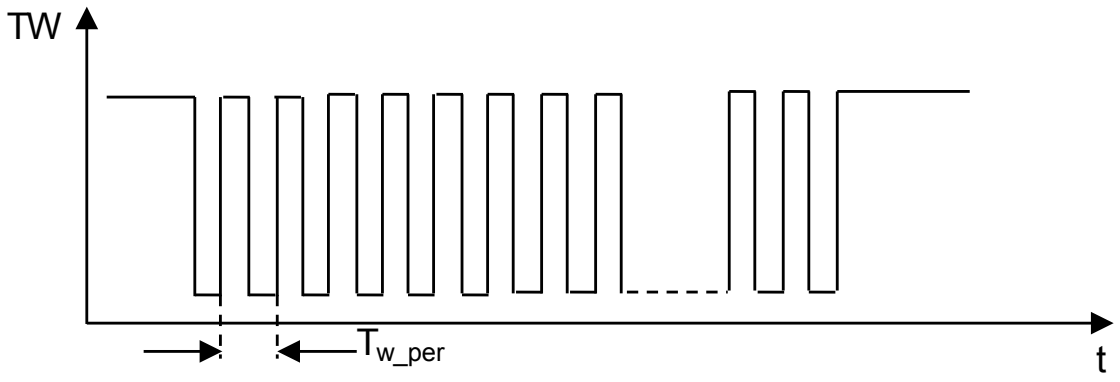


When junction temperature reaches the T_{prot} thermal shutdown threshold the regulator output is quickly shut-off through the internal fast output discharge circuit; to be reactivated, junction temperature has to decrease below T_{prot}- T_{prot_hyst}. Being TW an open-drain output an external resistance (R_{TW}) is needed between the TW pin and the V_O pin. The external resistance value can be in a range between 4.7 KΩ and 20 KΩ. Be aware that the current flowing through the TW pin drawn from V_O when the TW pin is pulled low may affect the watchdog activation/deactivation based on the regulator output current consumption monitoring. Leave floating if not used.

4.8 Overvoltage detection by advanced thermal warning read-out

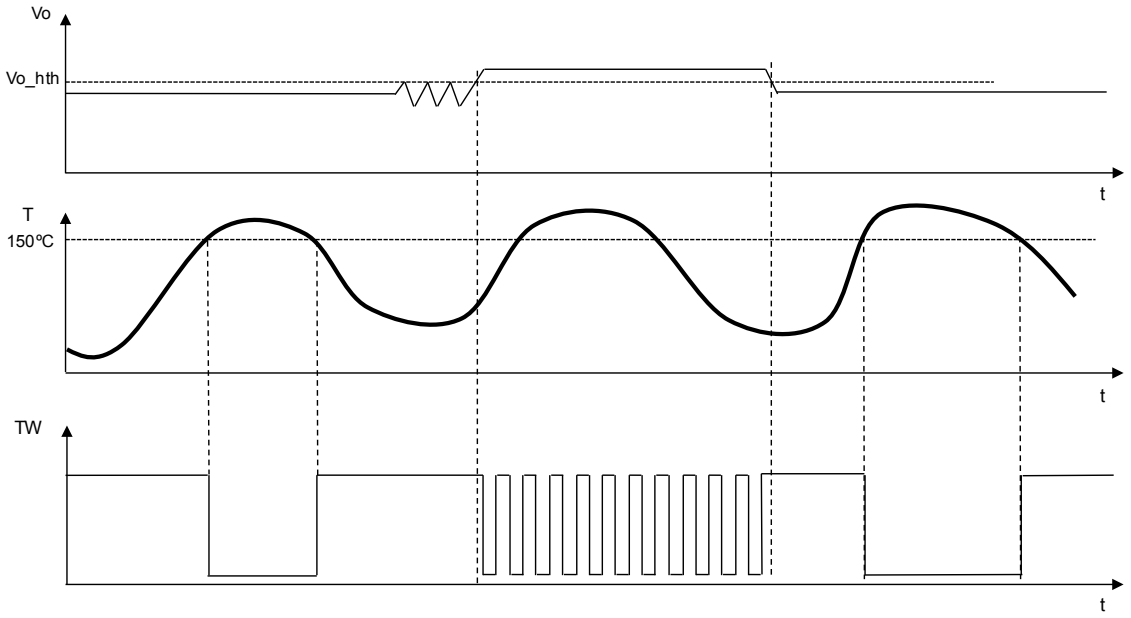
The TW pin also provides diagnostics about output overvoltage (OV); to distinguish between a thermal warning event and an output overvoltage event, two different signals are generated at the same TW output pin. How reported in the previous paragraph a thermal warning event detection sets the TW pin LOW, instead an output overvoltage event generates a square wave at the TW pin (Figure 40. Square wave on TW pin generated during an overvoltage). Overvoltage detection has higher priority than thermal warning detection so that concurrence of thermal warning and over voltage events lead to a square wave like in the case of overvoltage detection (as shown in Figure 41. Warning signal caused by overvoltage and thermal warning on TW pin).

Figure 40. Square wave on TW pin generated during an overvoltage



A typical example of thermal warning and overvoltage failures management is depicted in Figure 41. Warning signal caused by overvoltage and thermal warning on TW pin.

Figure 41. Warning signal caused by overvoltage and thermal warning on TW pin



4.9 Fast output discharge

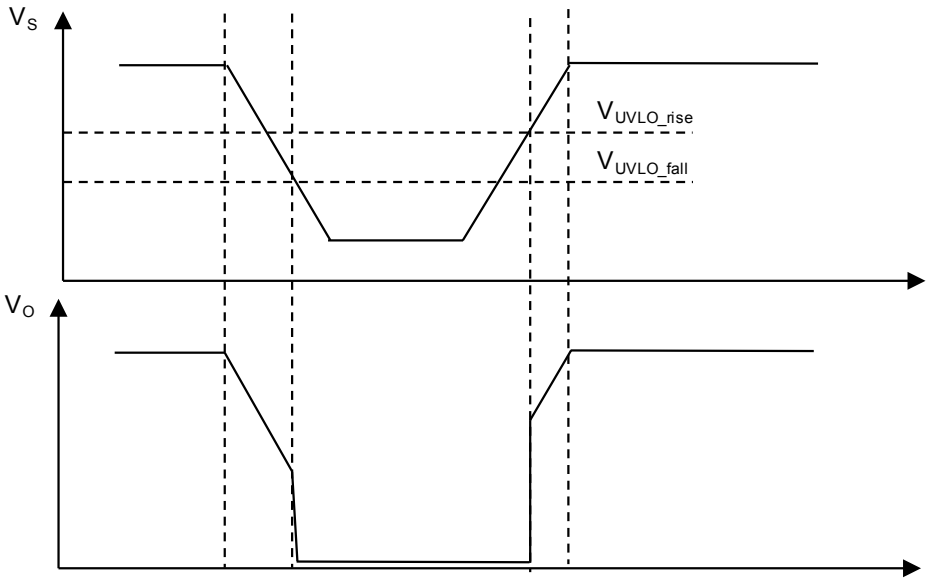
To assure a quick discharge of the external capacitor tied to the output pin down to around 1.3 V the L99VR02J uses an internal pulldown circuit. Activated each time the EN pin goes low, during thermal shutdown and during undervoltage lockout, the output current flows through the pulldown resistor of the fast output discharge circuit to the ground. The fast output discharge feature is available for the output voltages,

V_O = 2.5 V (SELx = [1;0;0]); V_O = 2.8 V (SELx = [1;0;1]); V_O = 3.3 V (SELx = [1;1;0]) and V_O = 5 V (SELx = [1;1;1]).

4.10 Undervoltage lockout UVLO

The undervoltage lockout (UVLO) circuit allows a fast regulating element to turn off (activating the internal fast output discharge circuit). This if the input voltage drops below the threshold, V_{UVLO_fall}, avoiding an undesired unknown output state during low input voltage. When the input voltage is above the V_{UVLO_rise} threshold, the regulating element is again turned on.

Figure 42. Undervoltage lock out on output voltage



4.11 Support to ISO26262

Even if not designed as the safety HW element, the device contains some features that can be used to support the application that needs to fulfill functional safety requirements. Analysis of the IC's capability to reach the required safety level, should be made at system level under user responsibility.

The following device safety requirements have been considered for a typical application:

Table 14. Safety requirement

ID	Description
SR-001	Operation of voltage regulator is allowed until over the temperature limit.
SR-002	Operation of voltage regulator is enabled until the programmed current limit is reached.
SR-003	Output voltage of regulator shall remain within programmed range when the RST pin is not asserted.
SR-004	Output voltage of the regulator shall remain within programmed range when the square wave at the TW pin is not generated.

Based on the above requirements list the following safety mechanism has been implemented:

Table 15. Implemented safety mechanism

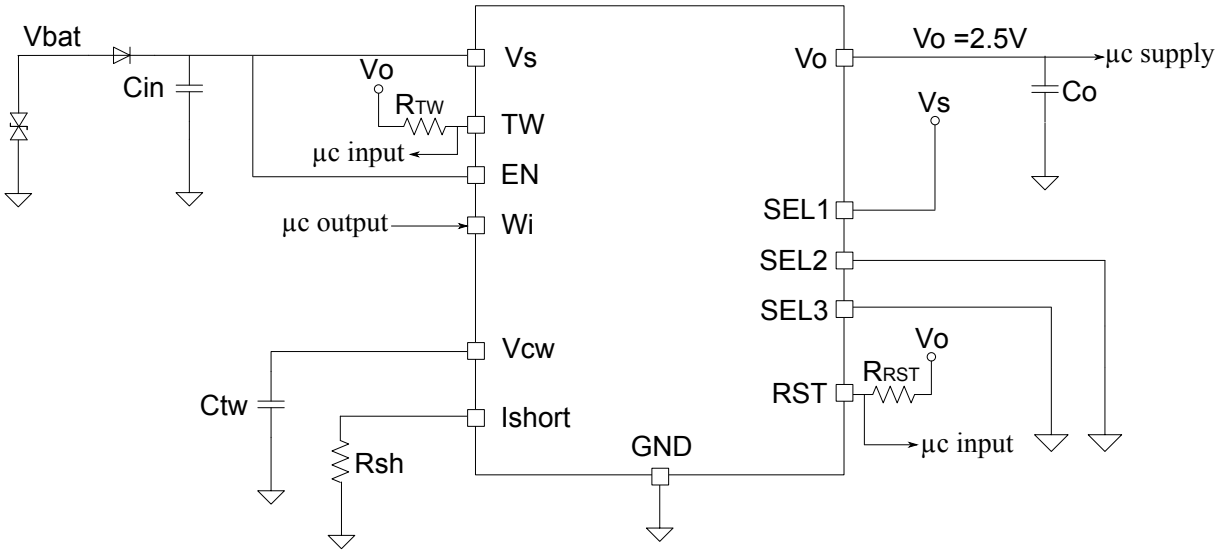
ID	Description	SR covered
SM1	Thermal sensor acting by the TW pin	SR-004
SM2	Overtemperature protection	SR-001
SM3	Limitation on maximum output current	SR-002
SM4	Output voltage V_O monitoring for undervoltage detection	SR-002
SM5	Output voltage V_O monitoring for overvoltage detection	SR-002
SM6	RST reset assertion in case of V_O undervoltage detection	SR-003

In addition to the internal watchdog for checking the correct operation of the microcontroller, it can be considered a system-level safety mechanism.

More details about functional safety can be found in the device safety manual, provided on customer request.

5 Application

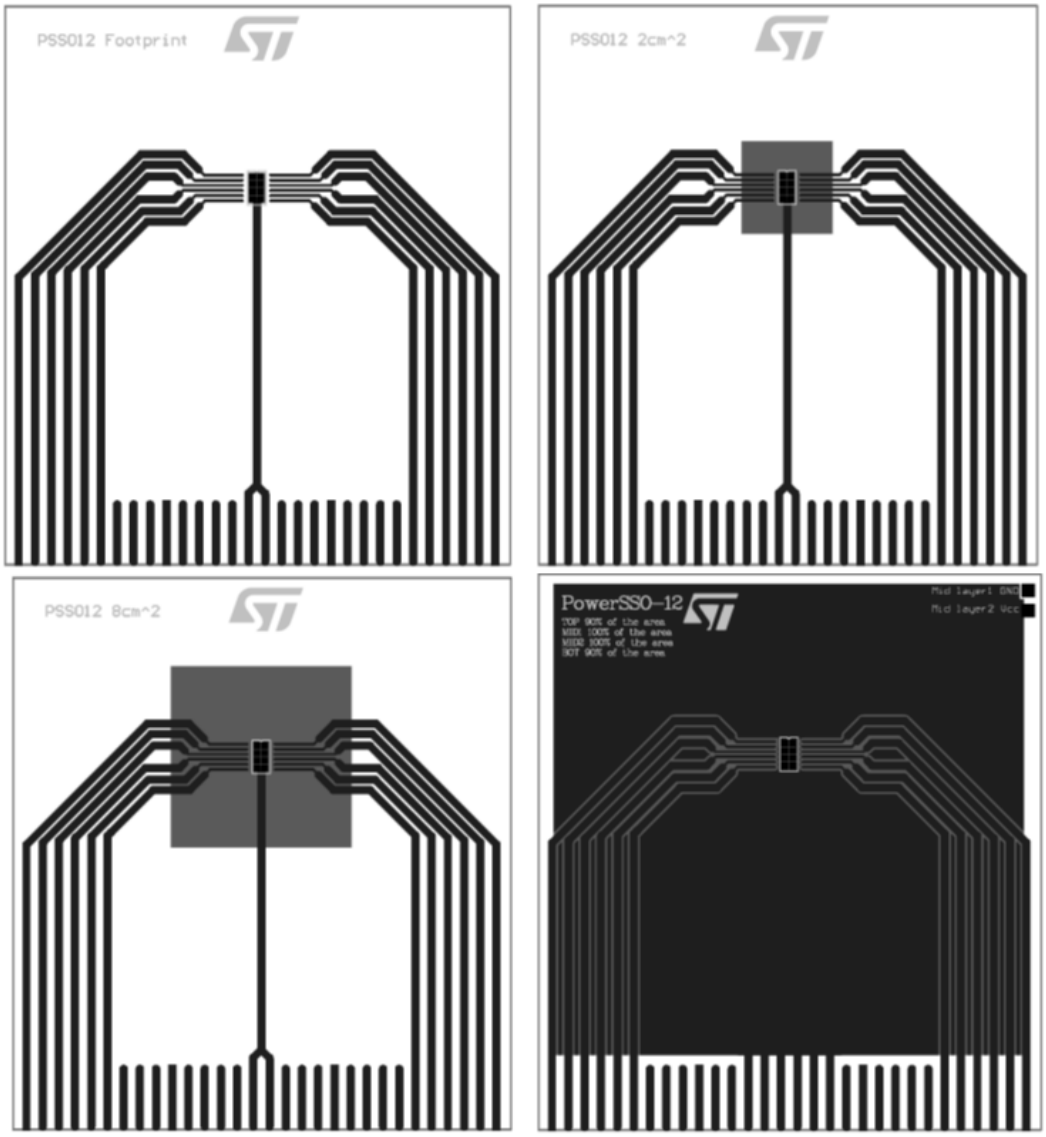
Figure 43. **Typical application**



6 Package and PCB thermal data

6.1 PowerSSO-12 thermal data

Figure 44. **PowerSSO-12 PC board**



Note: The values quoted are for PCB 77 mm x 86 mm x 1.6 mm, FR4, two and four layers; Cu thickness 0.070 mm (outer layers). Cu thickness 0.035 mm (inner layers), thermal vias separation 1.2 mm, thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 0.025 mm, footprint dimension 2.2 mm x 2.9 mm.

Figure 45. $R_{thj-amb}$ versus PCB copper area in open box free air condition

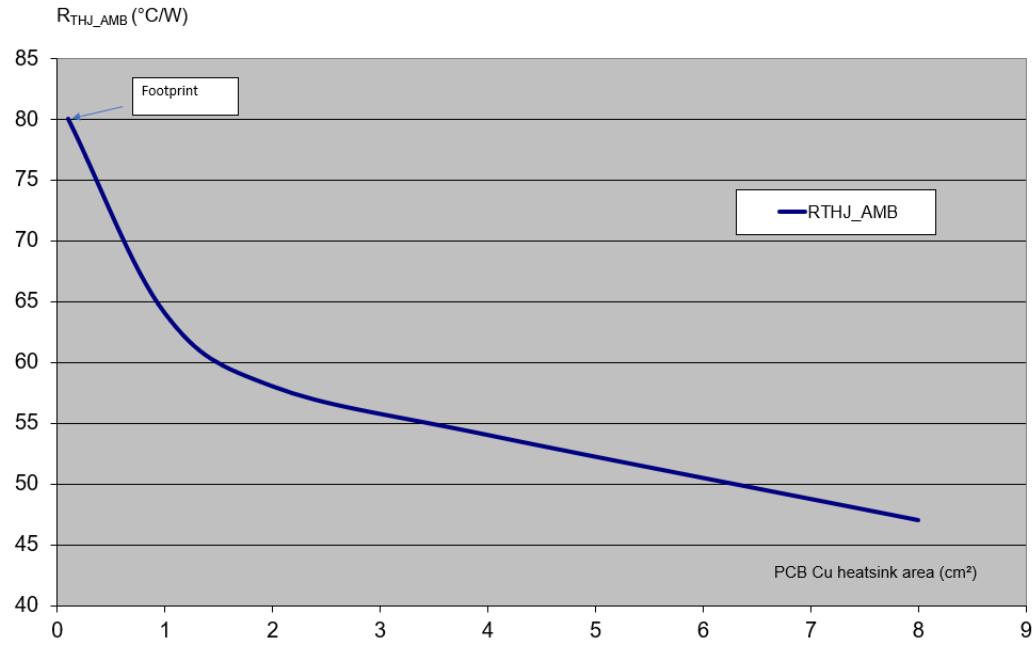
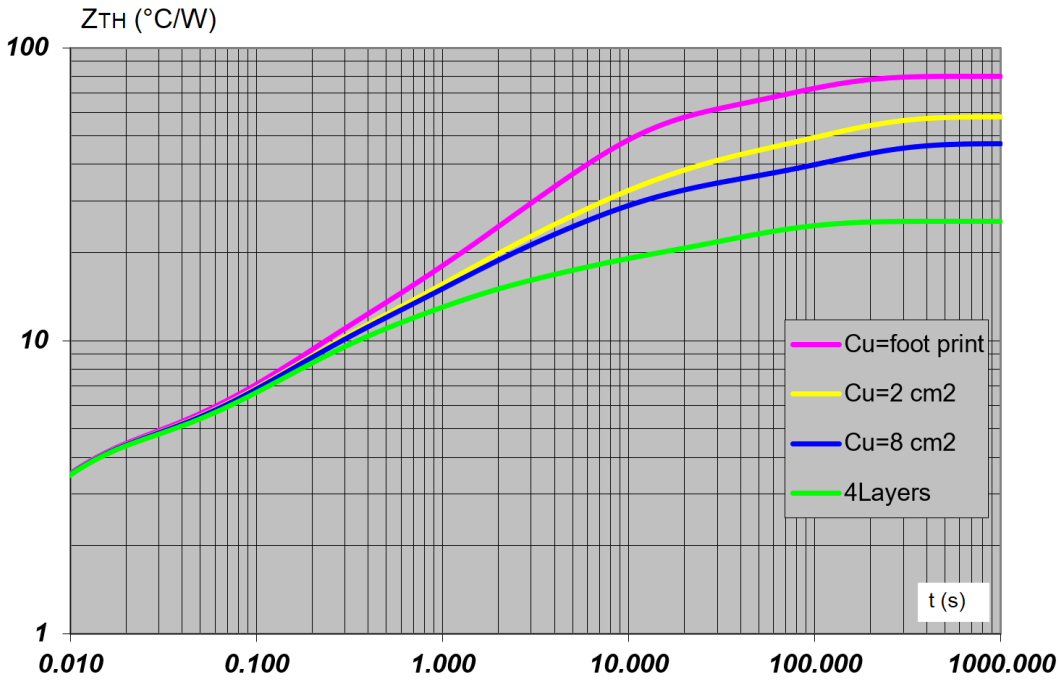


Figure 46. PowerSSO-12 thermal impedance junction ambient single pulse



Pulse calculation:

$Z_{TH\delta} = R_{TH}.\delta + Z_{THtp}(1-\delta)$

Where $\delta = tp/T$

Figure 47. **Thermal fitting model of a V_{reg} in PowerSSO-12**

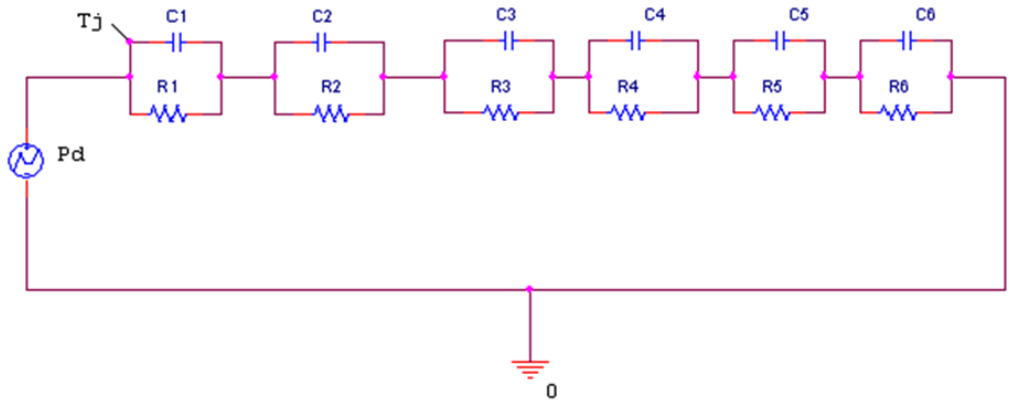


Table 16. **PowerSSO-12 thermal parameter**

Area/island (cm^2)	Footprint	2	8	4L
R1 (°C/W)	3.8			
R2 (°C/W)	4.2			
R3 (°C/W)	6	6	6	5
R4 (°C/W)	18	9	8	4.5
R5 (°C/W)	22	15	10	4
R6 (°C/W)	26	20	15	4
C1 (W.s/°C)	0.0015			
C2 (W.s/°C)	0.035			
C3 (W.s/°C)	0.15			
C4 (W.s/°C)	0.4	0.4	0.4	0.8
C5 (W.s/°C)	0.27	0.8	1	7
C6 (W.s/°C)	3	6	8	15

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 PowerSSO-12 package information

Figure 48. PowerSSO-12 package dimensions

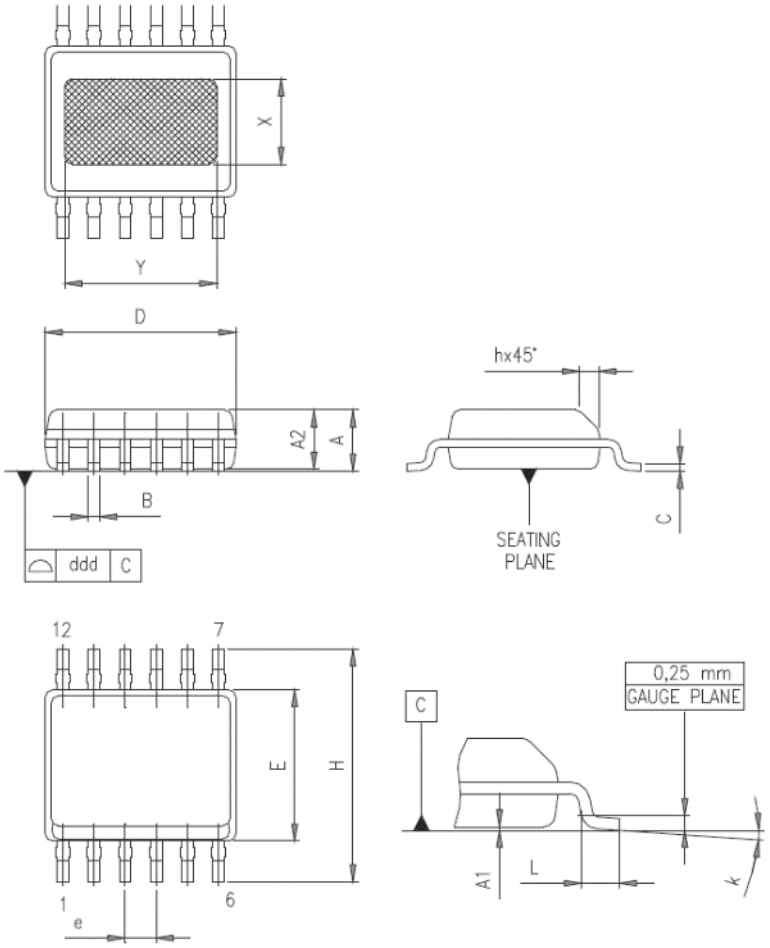
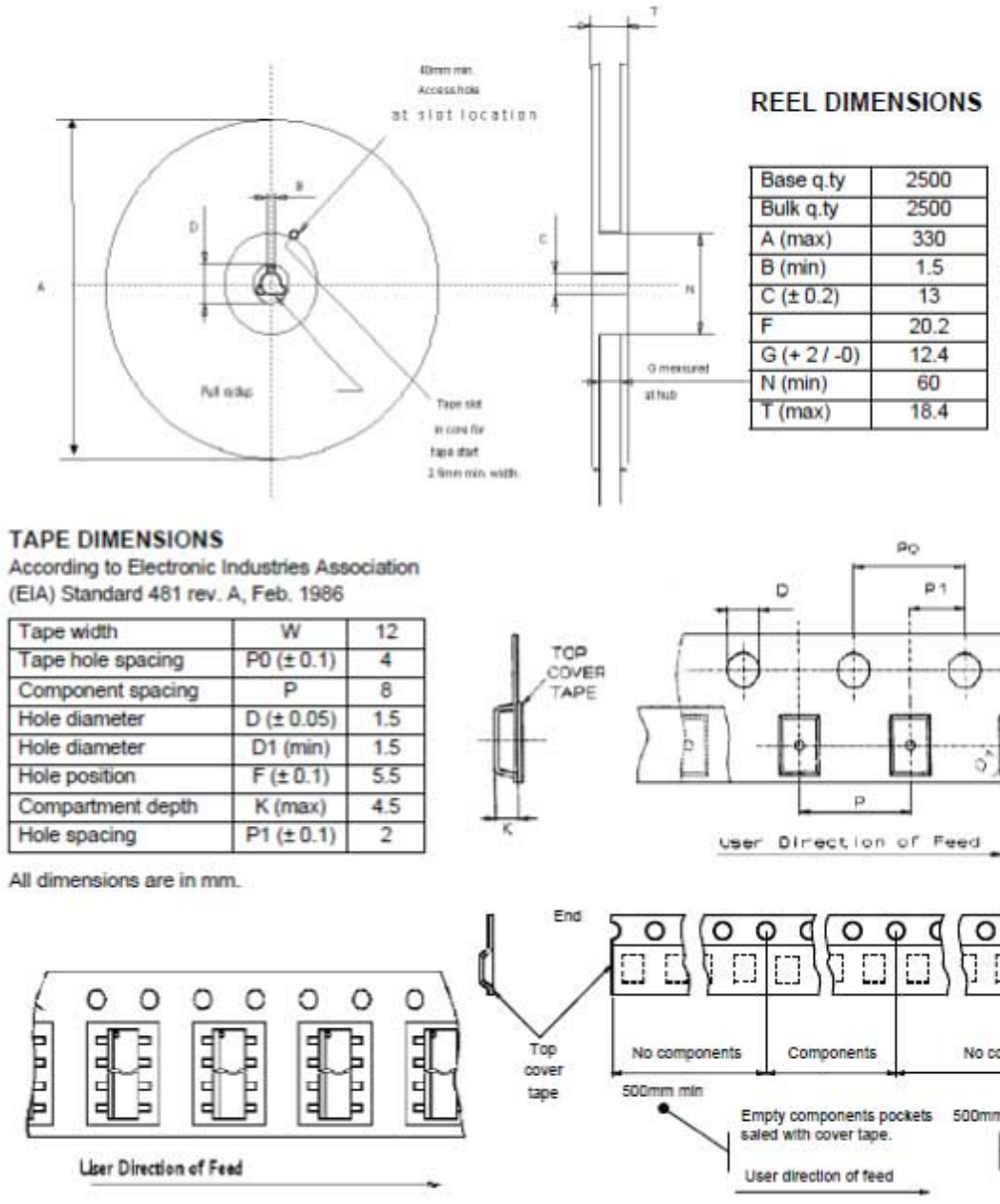


Table 17. **PowerSSO-12 package mechanical data**

Symbol	Millimeters		
	Min	Typ.	Max
A	1.250		1.700
A1	0.000		0.100
A2	1.100		1.600
b	0.230		0.410
c	0.190		0.250
D	4.800		5.000
E	3.800		4.000
e		0.800	
H	5.800		6.200
h	0.250		0.500
L	0.400		1.270
k	0°		8°
X	2.200		2.800
Y	2.900		3.500
ddd			0.100

7.2 PowerSSO-12 packaging information

Figure 49. **PowerSSO-12 tape and reel shipment (suffix "TR")**



Revision history

Table 18. **Document revision history**

Date	Version	Changes
22-Dec-2022	1	Initial release

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