Product Change Notification - SYST-12COGF694

Date:
13 Feb 2019
Product Category:
8-bit Microcontrollers
Affected CPNs:

Notification subject:
ERRATA - PIC16(L)F18313/18323 Family Silicon Errata and Data Sheet Clarification
Notification text:
SYST-12COGF694
Microchip has released a new DeviceDoc for the PIC16(L)F18313/18323 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at PIC16(L)F18313/18323 Family Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change: 1) Added two lines to Table 2. Added sections 4.2 and 5.3. Other minor corrections. 2) Data Sheet Clarifications: Added Table 35-6. Other minor corrections

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 13 Feb 2019

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A
Attachment(s):
PIC16(L)F18313/18323 Family Silicon Errata and Data Sheet Clarification

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Affected Catalog Part Numbers (CPN)

PIC16F18313-E/P
PIC16F18313-E/RF
PIC16F18313-E/RFV01
PIC16F18313-E/RFVAO
PIC16F18313-E/SN
PIC16F18313-E/SNVAO
PIC16F18313-I/P
PIC16F18313-I/PJIN
PIC16F18313-I/RF
PIC16F18313-I/SN
PIC16F18313-I/SNJIN
PIC16F18313-I/SNVAO
PIC16F18313T-E/RF021
PIC16F18313T-E/RFVAO
PIC16F18313T-E/SN
PIC16F18313T-E/SNVAO
PIC16F18313T-I/RF
PIC16F18313T-I/SN
PIC16F18313T-I/SNVAO
PIC16F18323-E/JQ
PIC16F18323-E/P
PIC16F18323-E/SL
PIC16F18323-E/SLVAO
PIC16F18323-E/ST
PIC16F18323-E/STVAO
PIC16F18323-I/JQ
PIC16F18323-I/P
PIC16F18323-I/PJIN
PIC16F18323-I/PREL
PIC16F18323-I/SL
PIC16F18323-I/SLJIN
PIC16F18323-I/SLVAO
PIC16F18323-I/ST
PIC16F18323T-E/JQ
PIC16F18323T-E/SL
PIC16F18323T-E/SLVAO
PIC16F18323T-E/ST
PIC16F18323T-E/STVAO
PIC16F18323T-I/JQ
PIC16F18323T-I/SL
PIC16F18323T-I/SLVAO
PIC16F18323T-I/ST
PIC16LF18313-E/P
PIC16LF18313-E/RF
PIC16LF18313-E/SN
PIC16LF18313-I/P

PIC16LF18313-I/RF
PIC16LF18313-I/SN
PIC16LF18313T-E/RF
PIC16LF18313T-I/RF
PIC16LF18313T-I/SN
PIC16LF18323-E/JQ
PIC16LF18323-E/P
PIC16LF18323-E/SL
PIC16LF18323-E/SLVAO
PIC16LF18323-E/ST
PIC16LF18323-I/JQ
PIC16LF18323-I/P
PIC16LF18323-I/SL
PIC16LF18323-I/ST
PIC16LF18323-I/ST024
PIC16LF18323-I/ST025
PIC16LF18323-I/STC02
PIC16LF18323T-E/SL
PIC16LF18323T-E/SLVAO
PIC16LF18323T-I/JQ
PIC16LF18323T-I/SL
PIC16LF18323T-I/SLC01
PIC16LF18323T-I/ST
PIC16LF18323T-I/ST024
PIC16LF18323T-I/ST025
PIC16LF18323T-I/ST026
PIC16LF18323T-I/STC02

PIC16(L)F18313/18323

PIC16(L)F18313/18323 Family Silicon Errata and Data Sheet Clarification

The PIC16(L)F18313/18323 family devices that you have received conform functionally to the current Device Data Sheet (DS40001799**E**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F18313/18323 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A6**).

Data Sheet clarifications and corrections start on page 7, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F18313/18323 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)		
		A3	A4	A6
PIC16F18313	3034h	2003h	2004h	2006h
PIC16LF18313	3036h	2003h	2004h	2006h
PIC16F18323	3035h	2003h	2004h	2006h
PIC16LF18323	3037h	2003h	2004h	2006h

Note 1: The Device IDs (DEVID and DEVREV) are located at addresses 8006h and 8005h, respectively. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC16(L)F183XX Memory Programming Specification"* (DS40001738) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)		
				A3	A4	A6
Oscillators	Register Reset Values	1.1	Reset value of OSCTUNE register is 0x20.	X		
Oscillators	32 MHz Clock	1.2	32 MHz Internal Clock Signal is not stable.	X		
Oscillators	Fail-Safe Clock Monitor (FSCM)	1.3	The FSCM may fail to trigger.	X		
Oscillators	Status Flag	1.4	PLLR bit of OSCSTAT1 register is incorrectly cleared.	X		
EUSART	Transmit	2.1	TX pin driven low.	X		
Master Synchronous Serial Port (MSSP)	SPI Slave Mode	3.1	Slave Select release during Sleep corrupts data.	X		
Master Synchronous Serial Port (MSSP)	SPI Slave Mode	3.2	Receive data lost when Slave Select enable occurs just before Sleep execution.	X		
Master Synchronous Serial Port (MSSP)	SPI Slave Mode	3.3	WCOL improperly set in Sleep.	X		
Master Synchronous Serial Port (MSSP)	SPI Slave Mode	3.4	SSPBUF transmit shift register may be corrupted under certain conditions.	X	X	X
Nonvolatile Memory (NVM) Control	NVMREG Access	4.1	Self-writes on LF devices below 2.2V at -40°C may not work.	X	X	
Nonvolatile Memory (NVM) Control	WRERR Bit	4.2	Write Error (WRERR) bit is incorrectly set.	X	X	X
Electrical Specifications	Fixed Voltage Reference (FVR) Accuracy	5.1	Fixed Voltage Reference (FVR) output tolerance may be higher than specified at temperatures below -20°C.	X	X	X
Electrical Specifications	SMBus 2.0	5.2	The maximum V_{IL} level changes when V_{DD} is below 4.0V at 125°C.	X	X	
Electrical Specifications	NVM Access	5.3	NVM access on LF devices may not work at all specified voltage and temperature ranges.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A6**).

1. Module: Oscillators

1.1 Register Reset Values

Upon any Power-on Reset (POR), the value in the OSCTUNE register will be 0x20, which is the lowest frequency adjustment allowed.

Work around

On initial start-up or after any Power-on Reset, write a 0x00 value into the OSCTUNE register, restoring the frequency adjustment back to the factory calibrated setting.

Affected Silicon Revisions

A3	A4	A6					
X							

1.2 32 MHz Clock

When the 32 MHz internal oscillator frequency is selected by writing '110' to either the RSTOSC [2:0] bits of Configuration Word 1 or the NOSC[2:0] bits of OSCCON1 and writing '0111' or '1xxx' to the HFFRQ[3:0] bits of OSCFRQ, the oscillator will fail to lock at 32 MHz and may become unstable.

Work around

1. To achieve a 32 MHz internal oscillator upon power-up or Reset, write '000' to the RSTOSC[2:0] bits of Configuration Word 1, which automatically selects the 32 MHz INTOSC with an internal 2xPLL, sets the HFFRQ[3:0] bits to '0110', and sets the NDIV[3:0] bits of OSCCON1 to '0000' (1:1 divider ratio).

2. To achieve a 32 MHz internal oscillator from an established clock source, write '000' to the NOSC[2:0] bits and '0000' to the NDIV[3:0] bits of OSCCON1, and write '0110' to the HFFRQ[3:0] bits of OSCFRQ.

HFFRQ[3:0]	Nominal Freq. (MHz) (NOSC = 110)	2xPLL Freq. (MHz) (NOSC = 000)
0000	1	Reserved
0001	2	
0010	Reserved	
0011	4	
0100	8	16
0101	12	24
0110	16	32
0111	Reserved	Reserved
1xxx	Reserved	Reserved

Affected Silicon Revisions

A3	A4	A6					
X							

1.3 Fail-Safe Clock Monitor (FSCM)

The Fail-Safe Clock Monitor may fail to trigger with the loss of the external clock signal when the 4x PLL is enabled. This includes all external clock modes, LP, XT, HS, ECL, ECM, and ECH.

Work around

None.

Affected Silicon Revisions

A3	A4	A6					
X							

1.4 Status Flag

When switching from the Internal Oscillator with PLL enabled to an external oscillator with PLL enabled and the clock switch fails, the PLL ready (PLLR) bit of the OSCSTAT1 register is incorrectly cleared.

Work around

None.

Affected Silicon Revisions

A3	A4	A6					
X							

2. Module: EUSART

2.1 Transmit

When the EUSART module is enabled (SPEN = `1`) with the transmit function disabled (TXEN = `0`), the TX assigned pin is driven low.

Work around

Load the desired logic level into the corresponding LATx register and assign the I/O function via the PPS output register.

Affected Silicon Revisions

A3	A4	A6					
X							

3. Module: Master Synchronous Serial Port (MSSP)

3.1 SPI Slave Data Corruption During Sleep

When the MSSP module is configured in SPI Slave mode with $\overline{SS}$ pin control enabled (SSPM = `0100`) and the device is in Sleep mode during SPI activity, if the SPI master releases the $\overline{SS}$ line ($\overline{SS}$ goes high) before the device wakes from Sleep and updates SSPBUF, the received data will be lost.

Work around

Method 1: The SPI master must wait a minimum of parameter SP83 (1.5 TCY + 40 nS) after the last SCK edge AND the additional wake-up time from Sleep (device dependent) before releasing the $\overline{SS}$ line.

Method 2: If both the master and slave devices have an available pin, once the slave has completed the transaction and BF or SSPIF is set, the slave could toggle an output to inform the master that the transaction is complete and that it is safe to release the $\overline{SS}$ line.

Affected Silicon Revisions

A3	A4	A6					
X							

3.2 SPI Slave Data Corruption During Sleep

When the MSSP module is configured in SPI Slave mode with $\overline{SS}$ pin control enabled (SSPM = `0100`) and the device is in Sleep mode during SPI activity, if the SPI master enables $\overline{SS}$ ($\overline{SS}$ goes low) within 1 TCY before Sleep is executed, the data written into the SSPBUF by the slave for transmission will remain in the SSPBUF, and the byte received by the slave will be completely discarded. The MSb of the data byte that is currently loaded into SSPBUF will be transmitted on each of the eight SCK clocks, resulting in either a 0x00 or 0xFF to be incorrectly transmitted. This issue typically occurs when the device wakes up from Sleep to process data and immediately goes back to Sleep during the next transmission.

Work around

The SPI Slave must wait a minimum of 2.25*TCY from the time the $\overline{SS}$ line becomes active ($\overline{SS}$ goes low) before executing the Sleep command.

Affected Silicon Revisions

A3	A4	A6					
X							

3.3 WCOL Bit Improperly Set During Sleep

When the MSSP module is configured with either of the Slave modes listed below and Sleep is executed during transmission, the WCOL bit is erroneously set. Although the WCOL bit is set, it does not cause a break in transmission or reception.

Mode 1: SPI Slave mode with $\overline{SS}$ disabled (SSPM = `0101`) and CKE = `0`.

Mode 2: SPI Slave mode with $\overline{SS}$ enabled (SSPM = `0100`) and $\overline{SS}$ is not set and then cleared before each consecutive transmission. This typically occurs during multiple byte transmissions in which the master does not release the $\overline{SS}$ line until all transmission has completed.

Work around

Method 1: The WCOL bit can be ignored since the issue does not interfere with MSSP hardware.

Method 2: Clear the SSPEN after each transaction, then set SSPEN before the next transaction.

Affected Silicon Revisions

A3	A4	A6					
X							

3.4 MSSP SPI Slave Mode

When operating in SPI Slave mode, if the incoming SCK clock signal arrives during any of the conditions below, the SSPBUF transmit shift register may become corrupted. The transmitted slave byte cannot be guaranteed to be correct, and the state of the WCOL bit may or may not indicate a write collision.

These conditions include:

- A write to an SFR
- A write to RAM following an SFR read
- A write to RAM prior to an SFR read

<u>Work around</u>

Method 1 (Interrupt-based using $\overline{SS}$): Connect the $\overline{SS}$ line to both the $\overline{SS}$ input and either an INT or IOC input pin.

1. Enable INT or IOC interrupts (interrupt on falling edge if available, otherwise check that $\overline{SS}$==0 when the interrupt occurs).
2. Load SSPBUF with the data to be transmitted.
3. Continue program execution.
4. When the Interrupt Service Routine (ISR) is invoked, do either of the following:
   a) Add a delay that ensures the first SCK clock will be complete, or
   b) Poll SSPSTAT.BF (while(BF==0)) and wait for the transmission/reception to complete.

Once either of these are complete, it is safe to return to program execution.

Method 2 (Bit polling-based using $\overline{SS}$):

1. Load SSPBUF with the data to be transmitted.
2. Poll the $\overline{SS}$ line and wait for the SS to go active (while(!PORTx.$\overline{SS}$==0)).
3. When $\overline{SS}$ is active ($\overline{SS}$==0), do either of the following:
   a) Add a delay that ensures the first SCK clock will be complete, or
   b) Poll SSPSTAT.BF (while(BF==0)), and wait for the transmission/reception to complete.

Once one of these two methods are complete, it is safe to return to program execution.

Method 3 ($\overline{SS}$ not available):

1. Load SSPBUF with the data to be transmitted.
2. Poll SSPSTAT.BF (while(BF==0)), and wait for the transmission/reception to complete.

<u>Affected Silicon Revisions</u>

A3	A4	A6					
X	X	X					

4. Module: Nonvolatile Memory (NVM) Control

4.1 NVMREG Access

When performing self-writes through NVMREG access on PIC16LF18313/18323 devices with VDD below 2.2V and at temperature of -40°C, the write operation may not work. This applies to both Program Flash Memory and EEPROM writes.

<u>Work around</u>

None.

<u>Affected Silicon Revisions</u>

A3	A4	A6					
X	X						

4.2 NVM WRERR

If a Reset occurs while a self-write operation is in progress, the Write Error (WRERR) bit is set. If the user clears the WRERR bit and another Reset occurs even though no self-write is in progress, the WRERR bit will be incorrectly set again since the internal write latch has not been cleared.

<u>Work around</u>

A successful write operation will clear the WRERR condition.

<u>Affected Silicon Revisions</u>

A3	A4	A6					
X	X	X					

5. Module: Electrical Specifications

5.1. Fixed Voltage Reference (FVR) Accuracy

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings, (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

<u>Work around</u>

At temperatures above -20°C, the stated tolerances in the data sheet remain in effect. Operate the FVR only at temperatures above -20°C.

<u>Affected Silicon Revisions</u>

A3	A4	A6					
X	X	X					

5.2. SMBus 2.0 V_{IL} Level

At 125°C when the V_{DD} voltage level supplied to the device is 4.0V and above, the maximum SMBus 2.0 voltage level for the V_{IL} parameter is 0.8V. When V_{DD} drops below 4.0V, the maximum SMBus voltage level for V_{IL} drops to 0.7V. This issue applies to extended temperature devices only.

Work around

None.

Affected Silicon Revisions

A3	A4	A6					
X	X						

5.3. Nonvolatile Memory

Nonvolatile memory (NVM) access on LF devices may not work when operating at temperatures between -40°C and +25°C and V_{DD} levels below 2.0V.

Work around

None.

Affected Silicon Revisions

A3	A4	A6					
X	X	X					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001799**E**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

TABLE 35-6: THERMAL CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)					
Param No.	**Sym.**		**Typ.**	**Units**	**Conditions**
TH01	θ_{JA}	Thermal Resistance Junction to Ambient	**46.2**	**°C/W**	**8-pin PDIP package**
			112.4	**°C/W**	**8-pin SOIC package**
			52.2	**°C/W**	**8-pin UDFN package**
			70.0	°C/W	14-pin PDIP package
			95.3	°C/W	14-pin SOIC package
			100.0	°C/W	14-pin TSSOP package
			51.5	°C/W	16-pin UQFN 4x4 mm package
			62.2	°C/W	20-pin PDIP package
			87.3	°C/W	20-pin SSOP package
			77.7	°C/W	20-pin SOIC package
			43.0	°C/W	20-pin UQFN 4x4 mm package
TH02	θ_{JC}	Thermal Resistance Junction to Case	**33.3**	**°C/W**	**8-pin PDIP package**
			50.0	**°C/W**	**8-pin SOIC package**
			4.0	**°C/W**	**8-pin UDFN package**
			32.75	°C/W	14-pin PDIP package
			31.0	°C/W	14-pin SOIC package
			24.4	°C/W	14-pin TSSOP package
			5.4	°C/W	16-pin UQFN 4x4 mm package
			27.5	°C/W	20-pin PDIP package
			31.1	°C/W	20-pin SSOP package
			23.1	°C/W	20-pin SOIC package
			5.3	°C/W	20-pin UQFN 4x4 mm package
TH03	T_{JMAX}	Maximum Junction Temperature	150	°C	
TH04	PD	Power Dissipation	0.8	W	$PD = P_{INTERNAL} + P_{I/O}$
TH05	$P_{INTERNAL}$	Internal Power Dissipation	—	W	$P_{INTERNAL} = I_{DD} \times V_{DD}$(1)
TH06	$P_{I/O}$	I/O Power Dissipation	—	W	$P_{I/O} = \Sigma(I_{OL} * V_{OL}) + \Sigma(I_{OH} * (V_{DD} - V_{OH}))$
TH07	P_{DER}	Derated Power	—	W	$P_{DER} = PD_{MAX}(T_J - T_A)/\theta_{JA}$(2)

Note 1: I_{DD} is the current to run the chip alone without driving any load on the output pins.

2: T_A = Ambient Temperature, T_J = Junction Temperature.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev G Document (01/2019)

Added two lines to Table 2. Added sections 4.2 and 5.3. Other minor corrections.

Data Sheet Clarifications: Added Table 35-6. Other minor corrections.

Rev F Document (01/2018)

Added Module 5.2: SMBus 2.0 V_{IL} Level.
Other minor corrections.

Rev E Document (07/2017)

Added Module 5: Electrical Specifications.

Data Sheet Clarifications: Removed Module 1: Comparator. Other minor corrections.

Rev D Document (01/2017)

Added Module 4: Nonvolatile Memory Control.

Data Sheet Clarifications:

Removed Module 1 through Module 7; Added new Module 1: Comparator.

Rev C Document (09/2016)

Data Sheet Clarifications:

Added new Module 6: Packaging Information.

Rev B Document (01/2016)

Added silicon revision A4 to Tables 1 and 2.

Rev A Document (10/2015)

Initial release of this document.

Note the following details of the code protection feature on Microchip devices:

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