Specification

BT45232

BTHQ128064AVD1-FSTF-12-LEDMULTI-COG

Doc. No.: COG-BTD12864-49

Version December 2010

DOCUMENT REVISION HISTORY

DOCUMENT REVISION FROM TO	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
A	2010.09.28	First Release. Based on: a.) VL-QUA-012B REV.Y 2010.12.10 According to VL-QUA-012B, LCD size is small because Unit Per Laminate=24 which is more than 6pcs/Laminate.	CHEN YUE	CHI SHAO BO
A B	2010.10.07	Items 1 to 4 were updated: 1.) (Page 6, Figure 2) Block Diagram was updated. 2.) (Page 7,Table 2(a)) Interface signals description was updated. 3.) (Page 11,Table 5) VLCD update define. 4.) (Page 16, Figure 7) Reference circuit was added.	LI WEI	CHI SHAO BO
B C	2010.12.23	Item 1 was updated: 1.) (Page 11,Table 5) None 4 was added.	LI WEI	CHI SHAO BO

CONTENTS

**Specification
of
LCD Module Type
Model No.: COG-BTD12864-49**

1.   General Description

- 128 x 64 Dots FSTN B & W Positive Transflective Dot Matrix LCD Module.
- Viewing Angle: 12 o'clock.
- Driving scheme: 1/65 duty, 1/7 bias.
- 'SITRONIX'ST7565P (COG) LCD controller/ driver or equivalent.
- FPC connection.
- RGB TRI color backlight.
- "RoHS " compliance.

2.   Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

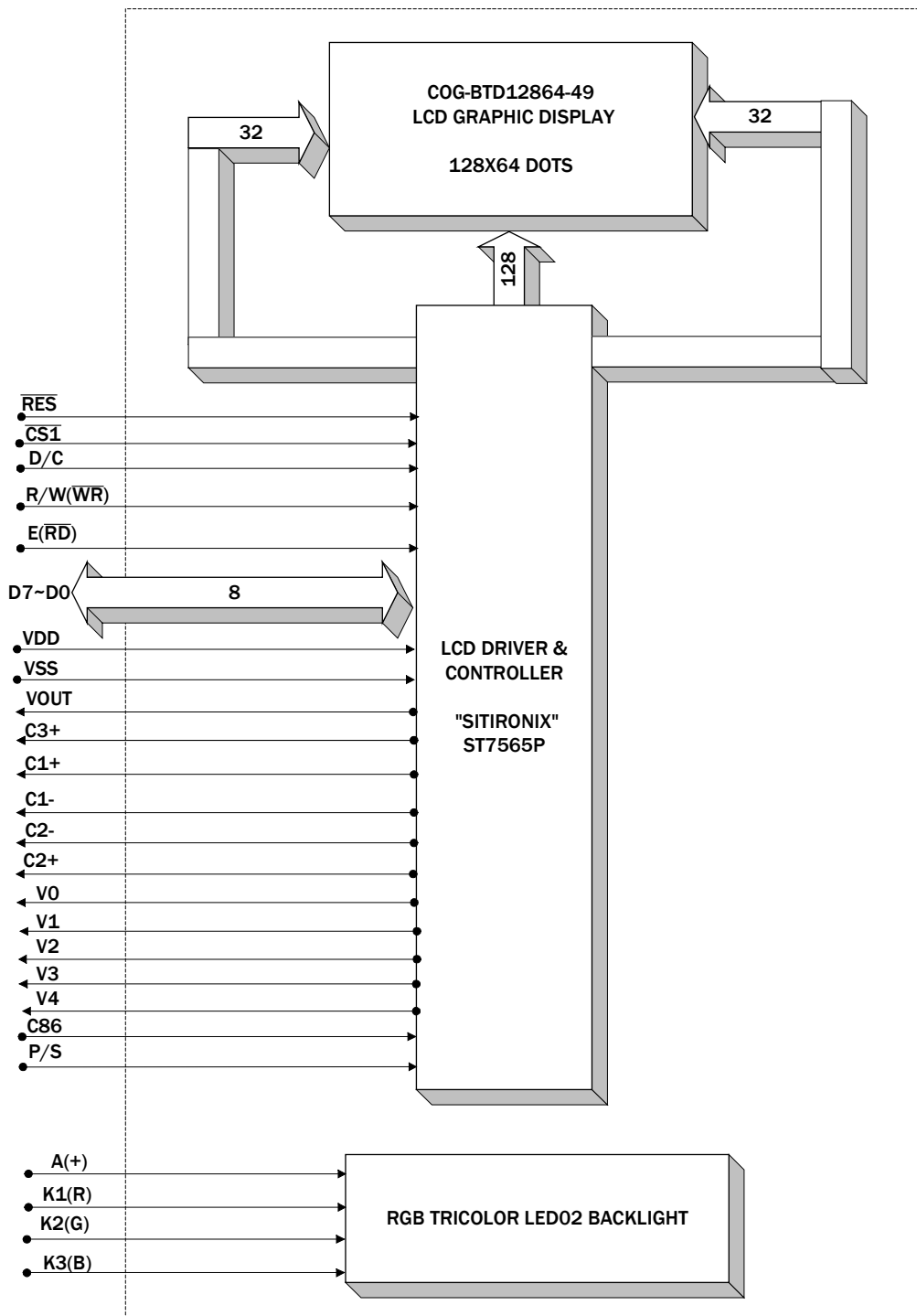| Parameter	Specifications	Unit
Outline dimensions	55.6(W) x 70.2(H) x 4.48(D) (Included FPC. Exclude terminals of backlight)	mm
Viewing area	50.60(W) x 31.0(H)	mm
Active area	46.577(W) x 27.697(H)	mm
Display format	128(W) x 64(H)	dots
Dot size	0.349(W) x 0.418(H)	mm
Dot spacing	0.015(W) x 0.015(H)	mm
Dot pitch	0.364(W) x 0.433(H)	mm
Weight	Approx: 15	grams

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ISSUE	AMENDMENT	DATE
△²	UPDATE THE IC AND PIN	10.04.26

TITLE: MODULE SPECIFICATION
PROJECT NO.: BTD12864
CUSTOMER REF.:

TOLERANCE UNLESS OTHERWISE SPECIFIED:
X.X ±0.3
X.XX ±0.1
ANGULAR ±1°
DIMENSIONS IN MM
MATERIAL: N/A FINISH: N/A
SCALE: DO NOT DN SCALE OVERALL THK: N/A
THIRD ANGLE PROJECTION

	NAME	SIGN	DATE
DRAWN:	QIU QINGRING		10.04.26
CHECKED:	CHI SHAO BO		
APPROVED:	PRITT LEE		

ITEM NO.: BT45232
BTHQ128064AVD1-FSTF-12-LEDMULTI-COG
FILE NO.: COG-BTD12864-49 R1 REV: 1
SHEET 1 OF 1

Display Type: FSTN, B&W, +VE, TRANSFLECTIVE
Display Resolution: 128 X 64 DOTS
Viewing Angle: 12 OCLOCK
Mux ratio and bias level: 1/65 DUTY, 1/7 BIAS
LCD Controller/Driver: ST7565P
Logic Voltage: 3.3V
LCD Driving Voltage: 8.65±0.2V
Operation Temperature: 0°C to 50°C
Storage Temperature: -20°C to 65°C

BACKLIGHT
TYPE: LED02 (2 PCS LEDS)
COLOR: RED &GREEN &BLUE
VOLTAGE: 4.2V (TYP)

LUMINANCE(cd/m2) (ON THE BACKLIGHT SURFACE)	RED 620~635nm	GREEN 510~540nm	BLUE 465~480nm
MIN.	–	–	–
TYP.	70	150	30
MAX.	–	–	–

REMARKS:

28 PIN CONNECTION	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	P/S	C86	V0	V1	V2	V3	V4	C2-	C2+	C1+	C1-	C3+	VOUT	VSS	VDD	D7	D6	D5	D4	D3	D2	D1	D0	E(RD)	R/W(WR)	D/C	CS1	RES

K1 (RED)
K2 (GREEN)
K3 (BLUE)

CIRCUIT FOR RGB TRICOLOR BACKLIGHT

128 X 64 DOTS

A(+) K1(R)
K2(G) K3(B)

DOTS SIZE FOR CUSTOMER REFERENCE ONLY

NOTES:
1. ◇ : SPECIAL CHARACTERISTIC
2. + : SAFETY CHARACTERISTIC
3. ▽ : CRITICAL DIMENSION
4. ( ) : REFERENCE DIMENSION

Figure 2: Block Diagram.

3.   Interface signals

Table 2(a): Pin Assignment

Pin No.	Symbol	Description
1	P/S	This pin configures the interface to be parallel mode or serial mode. P/S = "H": Parallel data input/output. P/S = "L": Serial data input. The following applies depending on the P/S status: | P/S	Data/Command	Data	Read/Write	Serial Clock
"H"	D/C	D0 to D7	$\overline{RD}$, $\overline{WR}$	X
"L"	D/C	D7	Write only	D6	 When P/S = "L", D0 to D5 must be fixed to "H". $\overline{RD}$ (E) and $\overline{WR}$ (R/W) are fixed to either "H" or "L". The serial access mode does NOT support read operation.
2	C86	This is the MPU interface selection pin. C86 = "H": 6800 Series MPU interface. C86 = "L": 8080 Series MPU interface.
3	V0	This is a multi-level power supply for the liquid crystal drive. The voltage supply applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on VSS, and must maintain the relative magnitudes shown below. $V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq VSS$ When the power supply turns ON, the internal power supply circuits produce the V1 to V4 voltages shown below. The voltage settings are selected using the LCD bias set command. For 1/7 bias: V1= 6/7 * V0, V2=5/7 * V0, V3=2/7 *V0, V4=1/7 * V0.
4	V1	
5	V2	
6	V3	
7	V4	
8	C2-	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2P terminal.
9	C2+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.
10	C1+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.
11	C1-	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1P terminal.
12	C3+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.
13	VOUT	DC/DC voltage converter. Connect a capacitor between this terminal and VSS or VDD.
14	VSS	Ground.
15	VDD	Power supply pins for logic.

Table 2(b): Pin Assignment

Pin No.	Symbol	Description
16	D7	This is an 8-bit bi-directional data bus that connects to an 8-bit standard MPU data bus. When the serial interface is selected (P/S = LOW), then D7 serves as the serial data input terminal (SI) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to high impedance. When the chip select is inactive, D0 to D7 are set to high impedance.
17	D6	
18	D5	
19	D4	
20	D3	
21	D2	
22	D1	
23	D0	
24	E($\overline{RD}$)	When connected to 8080 series MPU, this pin is treated as the "$\overline{RD}$" signal of the 8080 MPU and is LOW-active. The data bus is in an output status when this signal is "L". When connected to 6800 series MPU, this pin is treated as the "E" signal of the 6800 MPU and is HIGH-active. This is the enable clock input terminal of the 6800 Series MPU.
25	R/W($\overline{WR}$)	When connected to 8080 series MPU, this pin is treated as the "$\overline{WR}$" signal of the 8080 MPU and is LOW-active. The signals on the data bus are latched at the rising edge of the $\overline{WR}$ signal. When connected to 6800 series MPU, this pin is treated as the "R/W" signal of the 6800 MPU and decides the access type : When R/W = "H": Read. When R/W = "L": Write.
26	D/C	This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or command. D/C = "H": Indicates that D0 to D7 are display data. D/C= "L": Indicates that D0 to D7 are control data.
27	$\overline{CS1}$	This is the chip select signal. When /CS1 = "L", then the chip select becomes active, and data/command I/O is enabled.
28	$\overline{RES}$	When $\overline{RES}$ is set to "L", the register settings are initialized (cleared). The reset operation is performed by the /RES signal level.

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4.   Absolute Maximum Ratings

4.1   Electrical Maximum Ratings – for IC Only

Table 3

Parameter	Symbol	Min.	Max.	Unit
Power Supply voltage (Logic)	VDD	+0.3	+3.6	V
Power Supply voltage (VDD2)	VDD2	+0.3	+3.6	V
Power Supply voltage (V0, VOUT)	V0, VOUT	+0.3	+14.5	V
Power Supply voltage (V1, V2, V3, V4)	V1, V2, V3, V4	V0	+0.3	V

Note:

1. The VDD2, V0 to V4 and VOUT are relative to the VSS = 0V reference.
2. Insure that the voltage levels of V1, V2, V3, and V4 are always such that
   $VOUT \geq V0 \geq V1 \geq V2 \geq V3 \geq V4$.
3. Permanent damage to the LSI may result if the LSI is used outside of the absolute maximum ratings. Moreover, it is recommended that in normal operation the chip be used at the electrical characteristic conditions, and use of the LSI outside of these conditions may not only result in malfunctions of the LSI, but may have a negative impact on the LSI reliability as well.
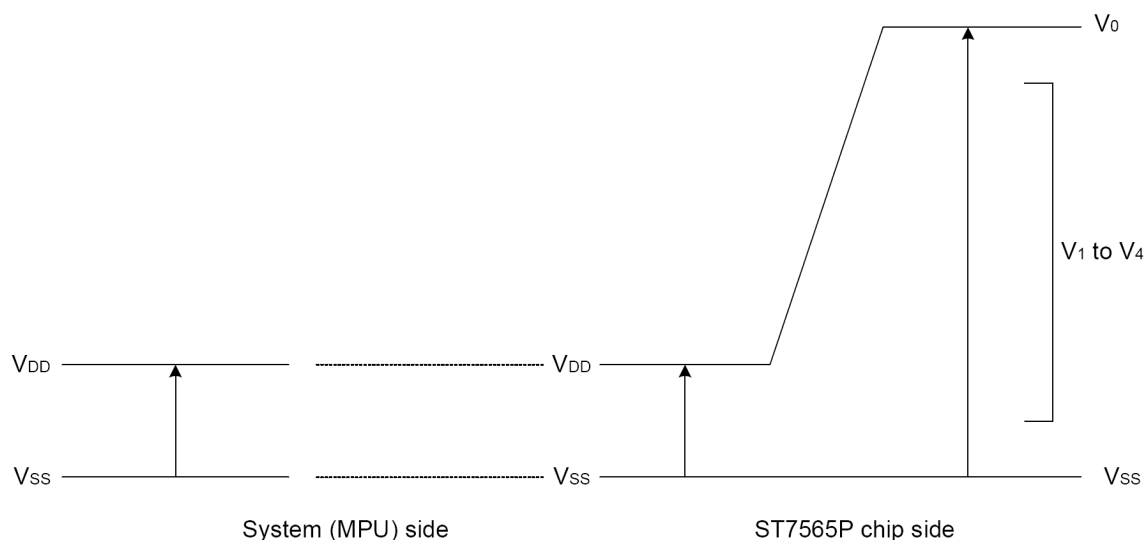

Figure 3

4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg) (Note 1)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	0°C	+50°C	-20°C	+65°C	Dry
Humidity (Note 1)	90% max. RH for Ta ≤ 40°C < 50% RH for 40°C < Ta ≤ Maximum operating temperature				No condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration: 11 ms Peak acceleration: 981 m/s^2 = 100g Number of shocks: 3 shocks in 3 mutually perpendicular axes.				3 directions

Note 1: Product cannot sustain at extreme storage conditions for long time.

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5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = +25 °C, VDD = +3.3±5%, VSS = 0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VDD-VSS		3.14	3.3	3.47	V
Supply voltage (LCD) (built-in)	VLCD =V0-VSS	Ta = 0 °C, Character mode VDD = +3.3V, Note 1	-	8.9	-	V
		Ta = 25 °C, Character mode VDD = +3.3V, Note 1	8.45	8.65	8.85	V
		Ta = +50 °C, Character mode VDD = +3.3V, Note 1	-	8.1	-	V
Low-level input signal voltage	V_{ILC}	Note 2	VSS	-	0.2xVDD	V
High-level input signal voltage	V_{IHC}	Note 2	0.8xVDD	-	VDD	V
Supply Current (Logic & LCD)	IDD	VDD = +3.3V,Note 1, Character mode	-	0.46	0.69	mA
		VDD = +3.3V,Note 1, Checker board mode	-	0.78	1.2	mA
Supply current of LED02 backlight	VLED (RED)	Forward voltage = 4.2V Number of LED die =2dies.	-	30	40	mA
	(GREEN) VLED		-	30	40	
	(BLUE) VLED		-	30	40	
Wavelength of LED02 backlight	λ (RED)		620	628	635	nm
	λ (GREEN)		510	525	540	
	λ (BLUE)		465	472	480	
Luminance (on the backlight surface) of backlight	(RED)	Note 4	38	70	140	cd/m^2
	(GREEN)		80	150	280	
	(BLUE)		15	30	80	

Note 1: There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

Note 2: D/C, D0 to D5, D6, D7, E($\overline{RD}$),R/W($\overline{WR}$),$\overline{CS1}$,C86,P/S,$\overline{RES}$ terminals.

Note 3: Do not display a fixed pattern for more than 30 min. because it may cause image sticking due to LCD characteristics. It is recommended to change display pattern frequently. If customer must fix display pattern on the screen, please consider to activate screen saver.

Note 4: The expected lifetime of backlight is 15K hours at 25°C,RH45%, If =15mA/die. This is a presumption target, no experimental data support.

5.2 Timing Specifications

System Bus read/Write Characteristics 1 (For the 8080 Series MPU)
At Ta = 0 °C to +50 °C, VDD = +3.3V±5%, VSS = 0V.

Table 6

Item	Signal	Symbol	Condition	Rating Min.	Rating Max.	Units
Address hold time	A0	t_{AH8}		0	—	
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		240	—	
Enable L pulse width (WRITE)	WR	t_{CCLW}		80	—	
Enable H pulse width (WRITE)		t_{CCHW}		80	—	
Enable L pulse width (READ)	RD	t_{CCLR}		140	—	Ns
Enable H pulse width (READ)		t_{CCHR}		80		
WRITE Data setup time	D0 to D7	t_{DS8}		40	—	
WRITE Address hold time		t_{DH8}		0	—	
READ access time		t_{ACC8}	C_L = 100 pF	—	70	
READ Output disable time		t_{OH8}	C_L = 100 pF	5	50	

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, (t_r +t_f) $\leq$ (t_{CYC8} – t_{CCLW} – t_{CCHW}) for (t_r + t_f) $\leq$ (t_{CYC8} – t_{CCLR} – t_{CCHR}) are specified.

*2 All timing is specified using 20% and 80% of V_{DD} as the reference.

*3 t_{CCLW} and t_{CCLR} are specified as the overlap between /CS1 being "L" (CS2 = "H") and /WR and /RD being at the "L" level.
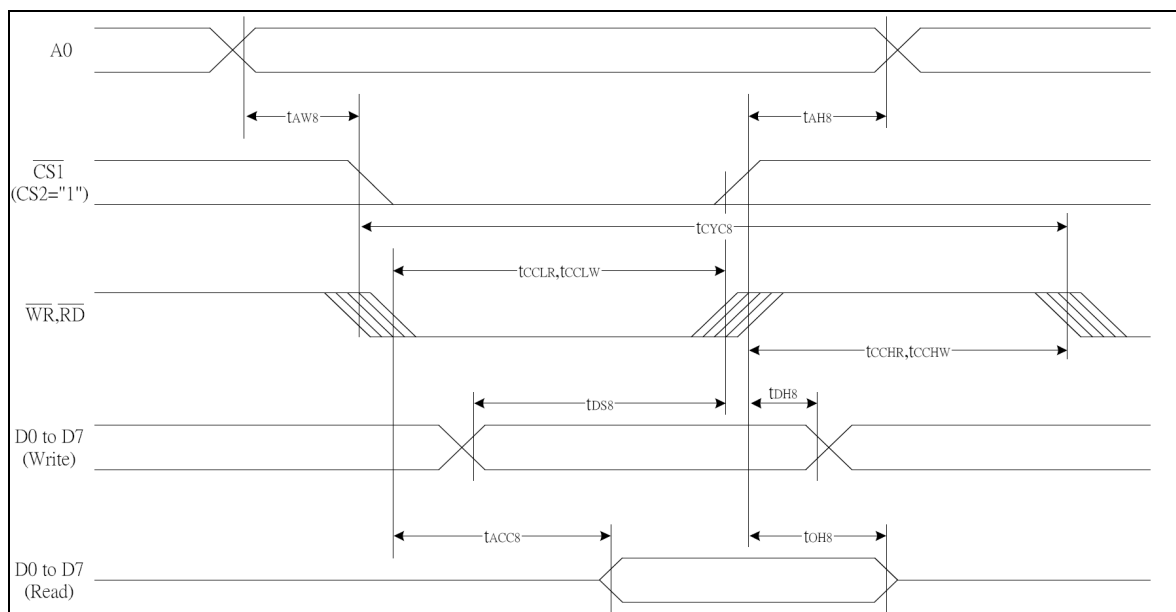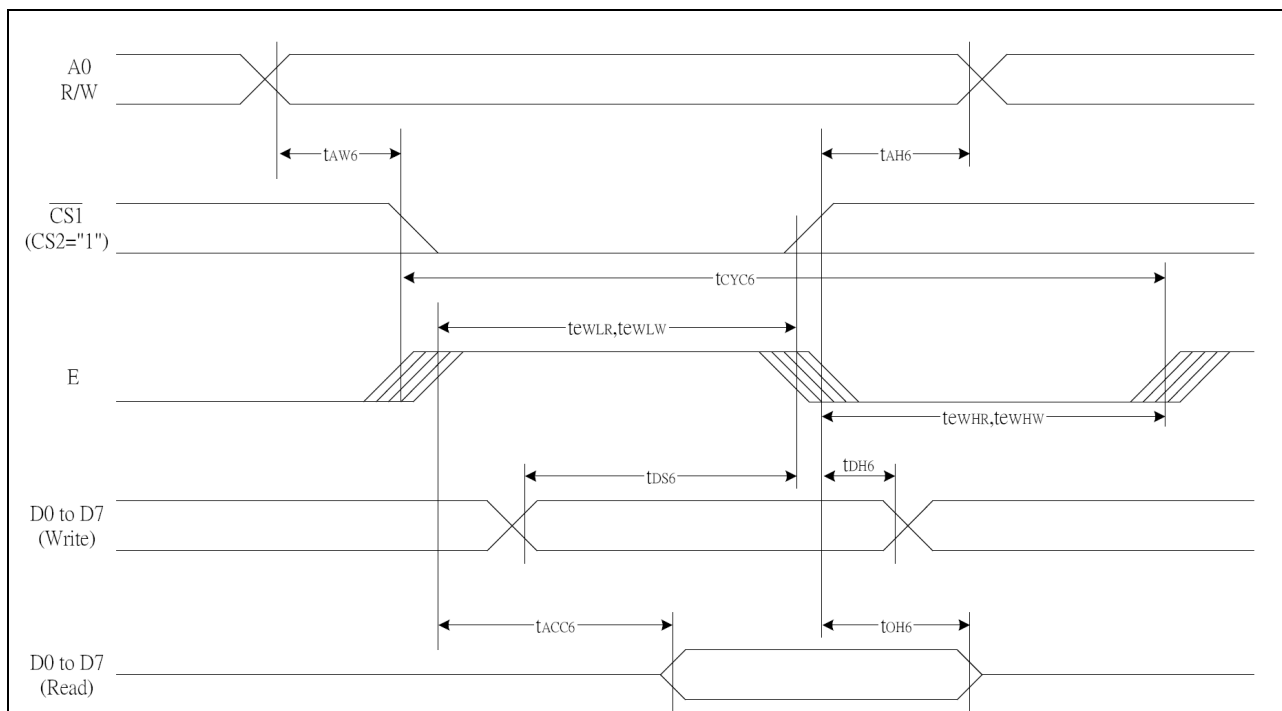

Figure 4: The timing diagram of system bus read/write (For the 8080 Series MPU)

System Bus read/Write Characteristics 2 (For the 6800 Series MPU)

At Ta =0 °C to +50 °C, VDD = +3.3V±5%, VSS = 0V.

Table 7

Item	Signal	Symbol	Condition	Rating Min.	Rating Max.	Units
Address hold time	A0	t_{AH6}		0	—	
Address setup time	A0	t_{AW6}		0	—	
System cycle time		t_{CYC6}		240	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		80	—	
Enable H pulse width (WRITE)	WR	t_{EWHW}		80	—	
Enable L pulse width (READ)	RD	t_{EWLR}		80	—	ns
Enable H pulse width (READ)	RD	t_{EWHR}		140		
WRITE Data setup time	D0 to D7	t_{DS6}		40	—	
WRITE Address hold time	D0 to D7	t_{DH6}		0	—	
READ access time	D0 to D7	t_{ACC6}	C_L = 100 pF	—	70	
READ Output disable time	D0 to D7	t_{OH6}	C_L = 100 pF	5	50	

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, (t_r +t_f) $\leq$ (t_{CYC6} – t_{EWLW} – t_{EWHW}) for (t_r + t_f) $\leq$ (t_{CYC6} – t_{EWLR} – t_{EWHR}) are specified.
*2 All timing is specified using 20% and 80% of V_{DD} as the reference.
*3 t_{EWLW} and t_{EWLR} are specified as the overlap between $\overline{CS1}$ being "L" (CS2 = "H") and E.

Figure 5: The timing diagram of system bus read/write (For the 6800 Series MPU)

Reset Timing

At Ta =0 °C to +50 °C, VDD = +3.3V±5%, VSS = 0V.

Table 8

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R		—	—	1.0	us
Reset "L" pulse width	/RES	t_{RW}		1.0	—	—	us

*1 All timing is specified with 20% and 80% of V$_{DD}$ as the standard.

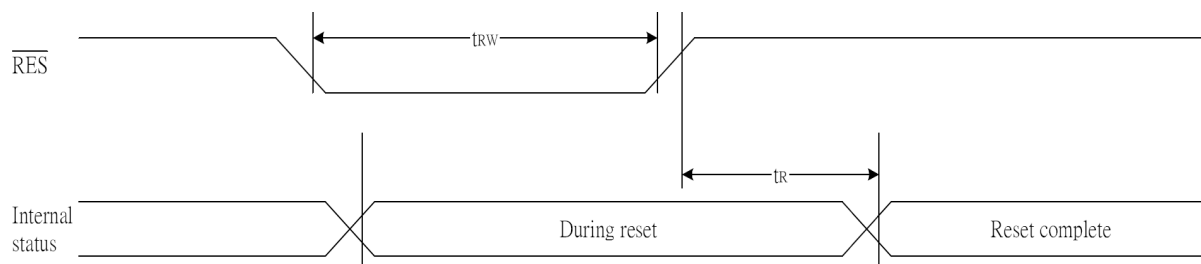Figure 6: Reset Timing

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5.3. Command Table

<u>Table 9</u>

Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
				Command Code								
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 / 1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(3) Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4) Column address set upper bit	0	1	0	0	0	0	1	Most significant column address				Sets the most significant 4 bits of the display RAM column address.
Column address set lower bit	0	1	0	0	0	0	0	Least significant column address				Sets the least significant 4 bits of the display RAM column address.
(5) Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6) Display data write	1	1	0	Write data								Writes to the display RAM
(7) Display data read	1	0	1	Read data								Reads from the display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0 / 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 / 1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 / 1	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0 / 1	Sets the LCD drive voltage bias ratio 0: 1/9 bias, 1: 1/7 bias (ST7565P)
(12) Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0 / 1	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17) V0 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio(Rb/Ra) mode
(18) Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	1	Set the V0 output voltage electronic volume register
Electronic volume register set				0	0	Electronic volume value						
(19) Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0 / 1	0: OFF, 1: ON
Static indicator register set				0	0	0	0	0	0	0	Mode	Set the flashing mode
(20) Booster ratio set	0	1	0	1	1	1	1	1	0	0	0	select booster ratio 00: 2x,3x,4x 01: 5x 11: 6x
				0	0	0	0	0	0	step-up value		
(21) Power saver												Display OFF and display all points ON compound command
(22) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(23) Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

5.4 Initial code setting (for reference only)

Table 10

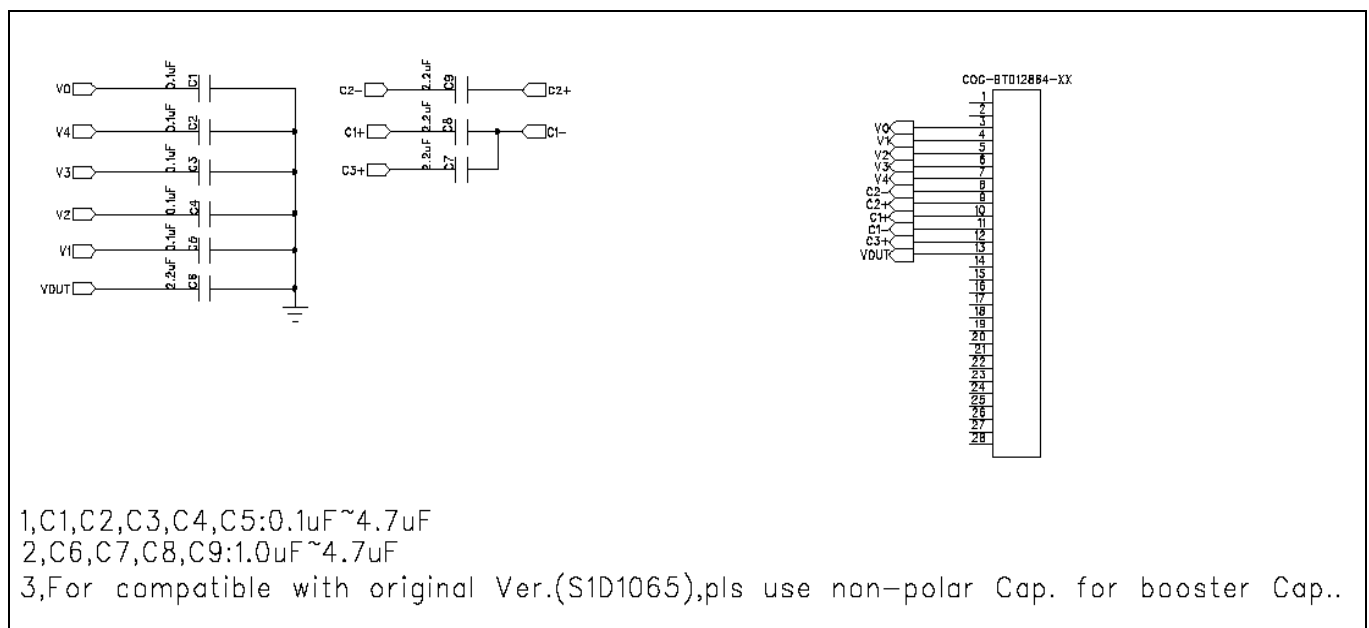| Description	Setting data
Reset	0xe2
LCD bias set	0xa3
ADC select	0xa0
Common output mode select	0xc8
V5 voltage regulator internal resistor ratio set	0x25
Electronic volume mode set	0x81
Electronic volume	0x13
Power control set	0x25
Display start line set	0x40
Page address set	0xb0
Column address upper bit set	0x10
Column address lower bit set	0x04
Display all point ON/OFF	0xa4
Display normal or reverse	0xa6

5.5 Reference circuit

1,C1,C2,C3,C4,C5:0.1uF~4.7uF
2,C6,C7,C8,C9:1.0uF~4.7uF
3,For compatible with original Ver.(S1D1065),pls use non-polar Cap. for booster Cap..

Figure 7: Reference Circuit Diagram

6.   Electro-Optical Characteristics

Table 11(B/L: Red)

Item	Symbol	Temp. °C	Value Min.	Value Typ.	Value Max.	Unit	Condition	
Driving voltage	Vop	+25	-	8.75	-	V	Vop= optimum voltage	
Response time	Ton	+25	-	4119	4942	msec	Vop= Optimum voltage θ = 0°, ϕ = 0°	
	Toff		-	7087	9213			
Optimum viewing area Cr ≥ 2	θ1(6 o'clock)	+25	22	32	-	DEG	ϕ = 0°	Vop= Optimum voltage (Remark 1)
	θ2(12 o'clock)		15	22	-			
	ϕ1(3 o'clock)		14	20	-		θ = 0°	
	ϕ2(9 o'clock)		17	25	-			
Contrast ratio	Cr	+25	2.8	4	-	-	Vop = Optimum voltage θ = 0°, ϕ = 0°	
Transmittance		+25	14%	20%	-	-	Vop = Optimum voltage	

Remark 1: Due to hardware limitation, the maximum measurable angle is 50 ^{O}

Table 12(B/L: Green)

Item	Symbol	Temp. °C	Value Min.	Value Typ.	Value Max.	Unit	Condition	
Driving voltage	Vop	+25	-	8.76	-	V	Vop= optimum voltage	
Response time	Ton	+25	-	5136	6677	msec	Vop= Optimum voltage θ = 0°, ϕ = 0°	
	Toff		-	4231	5500			
Optimum viewing area Cr ≥ 2	θ1(6 o'clock)	+25	21	30	-	DEG	ϕ = 0°	Vop= Optimum voltage (Remark 1)
	θ2(12 o'clock)		22	35	-			
	ϕ1(3 o'clock)		30	43	-		θ = 0°	
	ϕ2(9 o'clock)		20	28	-			
Contrast ratio	Cr	+25	2.8	4	-	-	Vop = Optimum voltage θ = 0°, ϕ = 0°	
Transmittance		+25	13%	19%	-	-	Vop = Optimum voltage	

Remark 1: Due to hardware limitation, the maximum measurable angle is 50 ^{O}

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Table 13(B/L: Blue)

Item	Symbol	Temp. °C	Min.	Typ.	Max.	Unit	Condition	
Driving voltage	Vop	+25	-	8.75	-	V	Vop= optimum voltage	
Response time	Ton	+25	-	8487	11033	msec	Vop= Optimum voltage $\theta = 0°$, $\phi = 0°$	
	Toff		-	7314	9508			
Optimum viewing area Cr ≥ 2	θ1(6 o'clock)	+25	21	30	-	DEG	$\phi = 0°$	Vop= Optimum voltage (Remark 1)
	θ2(12 o'clock)		28	40	-			
	φ1(3 o'clock)		28	40	-		$\theta = 0°$	
	φ2(9 o'clock)		20	28	-			
Contrast ratio	Cr	+25	2.8	4	-	-	Vop = Optimum voltage $\theta = 0°$, $\phi = 0°$	
Transmittance		+25	12%	17%	-	-	Vop = Optimum voltage	

Remark 1: Due to hardware limitation, the maximum measurable angle is 50 ^{O}

6.1 ISO plot

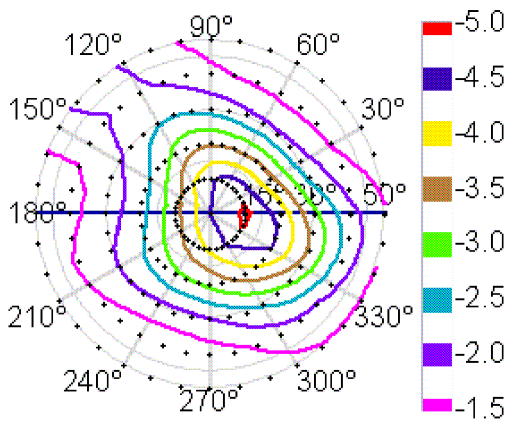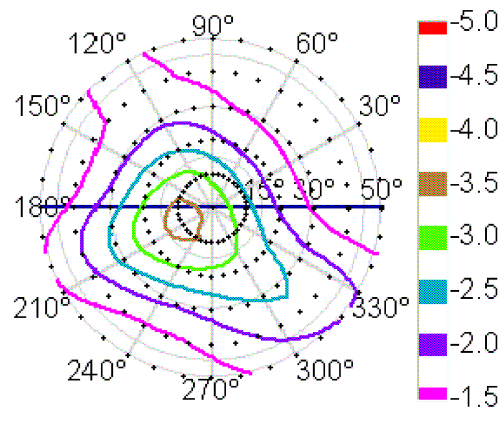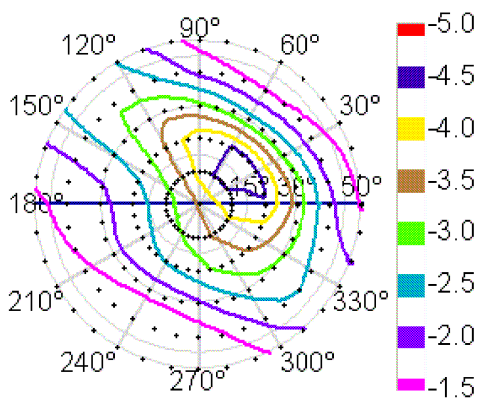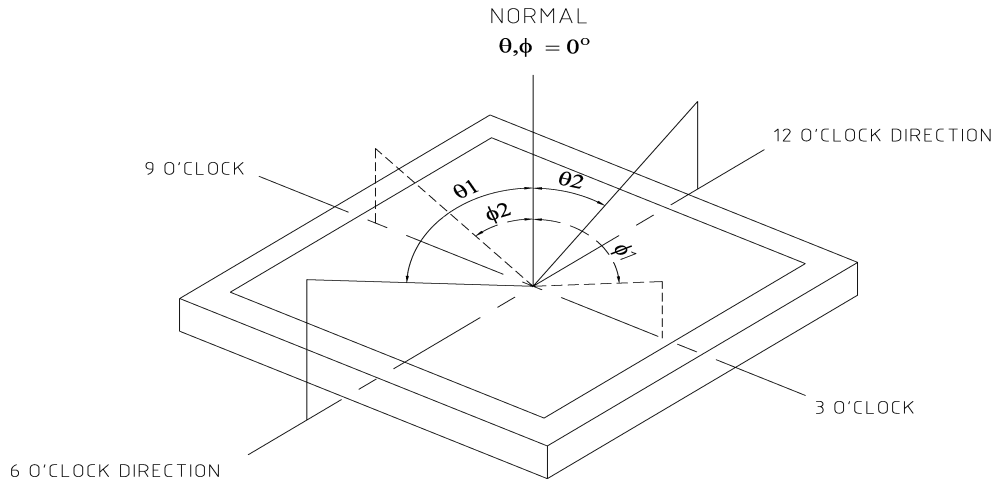Figure 7: B/L: Red

Figure 8: B/L: Green

Figure 9: B/L: Blue

6. 2   Optical Characteristics Definition

a.) Viewing Angle

NORMAL
$\theta, \phi = 0°$

12 O'CLOCK DIRECTION

9 O'CLOCK

$\theta1$ $\theta2$

$\phi2$

ϕ_1

3 O'CLOCK

6 O'CLOCK DIRECTION
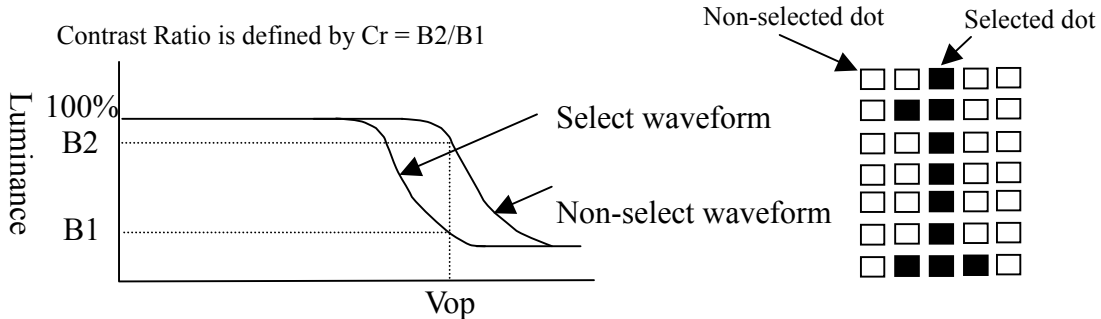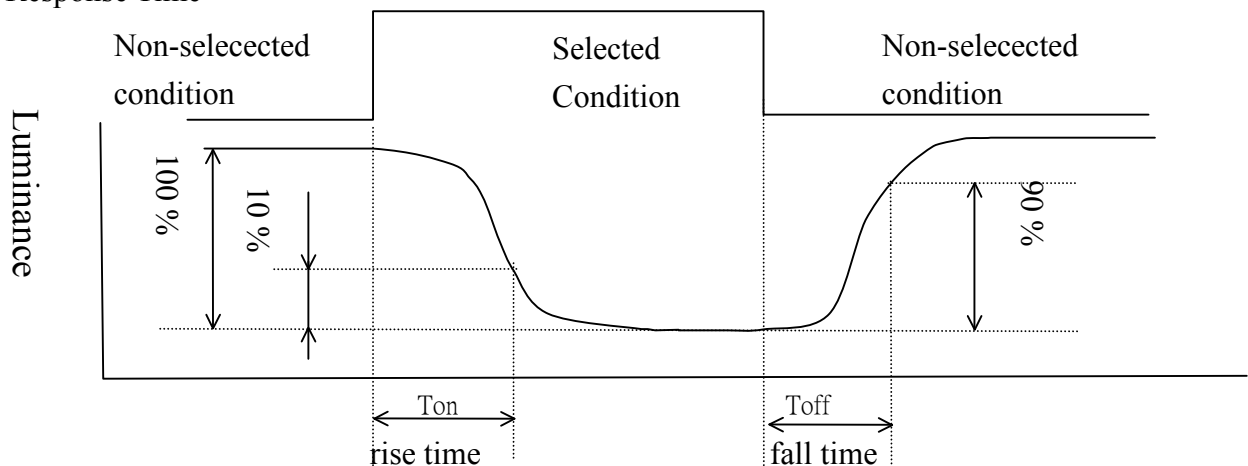
b.) Contrast Ratio

B1 = segments luminance in case of non-selected waveform

B2 = segments luminance in case of selected waveform

Contrast Ratio is defined by Cr = B2/B1

Non-selected dot   Selected dot

Luminance

100%
B2

Select waveform

B1

Non-select waveform

Vop

c.) Response Time

Non-selecected condition

Selected Condition

Non-selecected condition

Luminance

100 %

10 %

90 %

Ton

rise time

Toff

fall time