MAX16137

1% Accuracy Single-Window Voltage Monitor with BIST

General Description

The MAX16137 is a low-voltage, ±1% accurate supervisory circuit that monitors a single system supply voltage for undervoltage and overvoltage faults within a factory-set threshold window. When the monitored supply voltage drops below the undervoltage threshold or goes above the overvoltage threshold, the reset output asserts low. The reset output deasserts after the reset timeout period when the supply voltage returns to within the undervoltage and overvoltage threshold window. The reset output is active-low available in either the push-pull or open-drain options.

The MAX16137 offers factory-trimmed nominal input voltage options from 0.5V to 5V in approximately 20mV increment. A variety of factory-trimmed undervoltage/overvoltage thresholds from ±4% to ±11% are available to accommodate different supply voltages and tolerances.

The MAX16137 features a unique Built-In-Self-Test (BIST) diagnostic capability that monitors the health of the internal reset circuit during power-up. If the built-in-self-test fails, the MAX16137 asserts $\overline{BIST}$ low. During normal operation, the MAX16137 performs an on-demand BIST when the $\overline{CLR/BIST}$ is pulled low for more than 150µs. See the Built-In-Self-Test section for more details.

The MAX16137 is available in a small, 2mm x 2mm, 8-pin TDFN side-wettable package with exposed pad and operates over the automotive temperature range of -40°C to +125°C.

Applications

- Advanced Driver-Assistance Systems (ADAS)
- Multivoltage ASICs
- Servers
- Storage Equipment

Benefits and Features

- ±1% Allow Precision Supply Monitoring
- BIST Enhances System Safety
- Enables ASIL Compliance at System Level
- Factory-Set Threshold 0.5V to 5V with 20mV Increment
- Factory-Set Input Tolerance ±4% to ±11% UV/OV Threshold Window
- Factory-Set Reset Timeout
- Latched Overvoltage Fault Output
- 5µs Overvoltage Fault Response
- Open-Drain/Push-Pull Reset Output
- 2mm x 2mm TDFN-8 Side-Wettable Package
- -40°C to +125°C Temperature Range
- AEC-Q100 Qualified

***Ordering Information* appears at end of data sheet.**

Typical Application Circuit

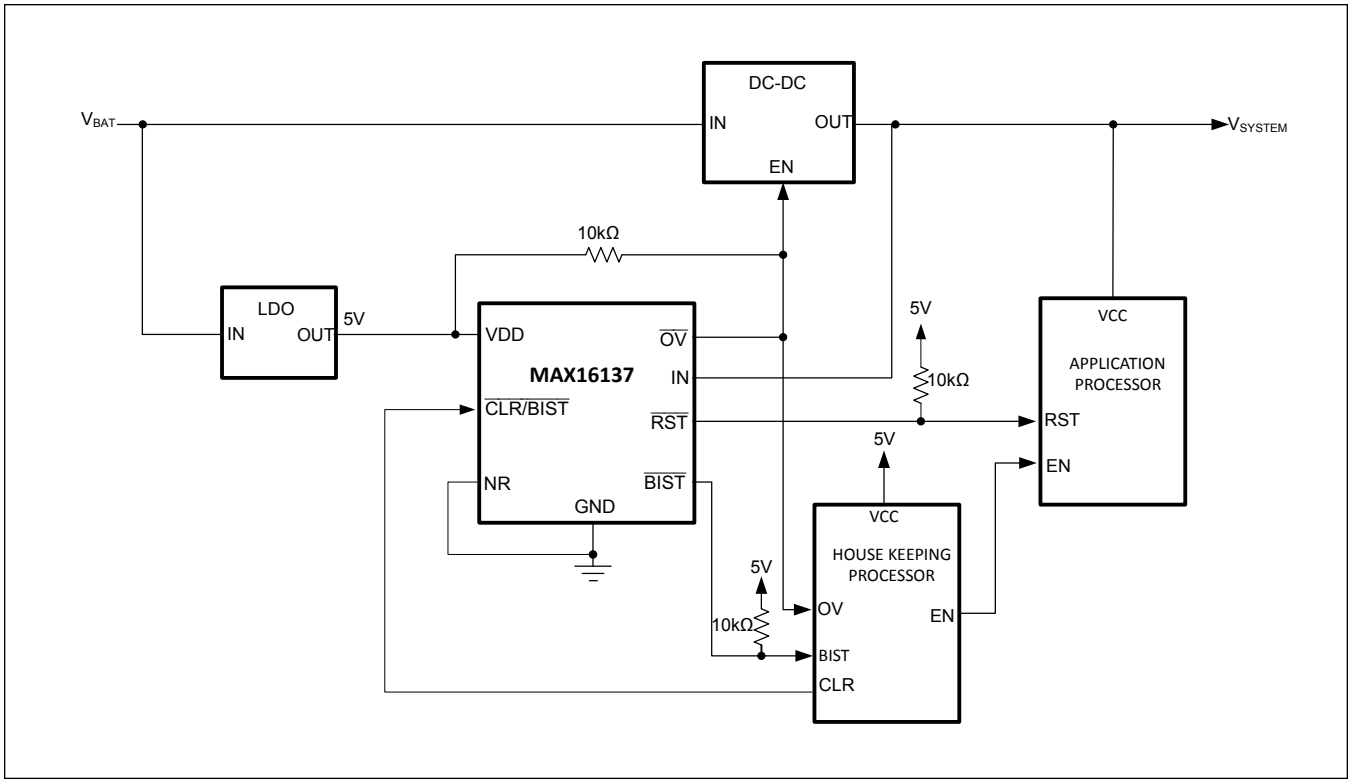


TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Absolute Maximum Ratings

VDD to GND ..... -0.3V to +6V
IN, $\overline{RST}$(Open-Drain Output), $\overline{CLR/BIST}$, $\overline{OV}$, $\overline{BIST}$, NR to GND ..... -0.3V to +6V
$\overline{RST}$(Push-Pull Output) to GND .....-0.3V to (V_{DD}+0.3V)V
Input/Output Continuous Current, $\overline{RST}$, $\overline{CLR/BIST}$, $\overline{OV}$, $\overline{BIST}$, NR ..... ±20mA
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Soldering Temperature (Reflow) ..... +260°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature ((Soldering, 10s)) ..... +300°C
Continuous Power Dissipation (T_A = +70°C, TDFN-8, derate 6.2mW/°C above +70°C) 496mW

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TDFN-8

Package Code	T822CY+2C
Outline Number	21-100341
Land Pattern Number	90-100117
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	162
Junction to Case (θ_{JC})	20

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{DD} = 1.71V to 5.5V. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Operating Voltage Range	V_{DD}	Comparators functional	1.71		5.5	V
Minimum Supply Voltage		$\overline{RST}$ is guaranteed to be at a known logic	1.1			V
Supply Current	I_{DD}	$\overline{RST}$, $\overline{OV}$, $\overline{BIST}$ not asserted		12	23	µA
Undervoltage Lockout Threshold	V_{UVLO}	V_{DD} rising	1.30	1.50	1.68	V
UVLO Hysteresis	V_{UVLO_HYS}	V_{DD} falling		47		mV
INPUT VOLTAGE(IN)						
Nominal Input Voltage Programming Range	V_{IN_NOM}		0.5		5	V
Nominal Input Voltage Programming Step				20		mV

Electrical Characteristics (continued)

(V_{DD} = 1.71V to 5.5V. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage/ Overvoltage Window Threshold Programming Range	TOL	Reset occurs when V_{IN_NOM} falls outside of V_{IN_NOM} x (1 ± TOL)	±4		±11	%
Window Threshold Programming Resolution	TOL_{RES}			1		%
INPUT THRESHOLD ACCURACY						
Undervoltage Threshold Accuracy	V_{UVTH_A}	All V_{IN_TH} setting, V_{IN_NOM} falling, V_{UVTH} = V_{IN_NOM} x (1 - TOL%)	-1		1	%
Overvoltage Threshold Accuracy	V_{OVTH_A}	All V_{IN_TH} setting, V_{IN_NOM} rising, V_{OVTH} = V_{IN_NOM} x (1 + TOL%)	-1		1	%
Undervoltage/ Overvoltage Threshold Hysteresis	V_{HYS}			0.5		%VTH
Input Current	I_{IN}			1.3	5	µA
Overvoltage Fault-to-$\overline{OV}$ Assert Delay	$t_{OV\ DLY}$	(V_{OVTH} - 1%) to (V_{OVTH} + 1%)		5		µs
CLEAR/BUILT-IN-SELF-TEST INPUT($\overline{CLR/BIST}$)						
$\overline{CLR/BIST}$ Input Glitch Immunity			50			ns
$\overline{CLR/BIST}$ Input Pulse Width to Clear OV Latch	t_{CLR}	From falling edge of $\overline{CLR/BIST}$ to $\overline{OV}$ rising edge	0.4			µs
$\overline{CLR/BIST}$ Pulse Width to Initiate BIST	t_{BIST}	From falling edge of $\overline{CLR/BIST}$ to start of BIST (Note2)	150			µs
$\overline{CLR/BIST}$ Internal Pull Up Resistance				50		kΩ
On-Demand $\overline{CLR/BIST}$ to $\overline{BIST}$ Assert Delay		From the falling edge of the $\overline{CLR/BIST}$ to $\overline{BIST}$ asserting			380	µs
RESET OUTPUT ($\overline{RST}$)						
Reset Timeout Period Accuracy	t_{RP}	From time V_{IN} enters overvoltage/ undervoltage threshold-window to time $\overline{RST}$ goes high, V_{DD} = 3.3V	-20		+20	%
IN-to-$\overline{RST}$ Propagation Delay	t_{DOV}	(V_{OVTH} - 1%) to V_{OVTH} + 1%)		5		µs
	t_{DUV}	(V_{UVTH} + 1%) to (V_{UVTH} - 1%)		12		
$\overline{RST}$ Leakage Current		$V_{\overline{RST}}$ = $V_{\overline{OV}}$ = 5.5V		0.01	1	µA
INPUT VOLTAGE ($\overline{CLR/BIST}$, NR)						
$\overline{CLR/BIST}$, NR Input Voltage Low	V_{IL}				0.3 x V_{DD}	V
$\overline{CLR/BIST}$, NR Input Voltage High	V_{IH}		0.7 x V_{DD}			V
$\overline{CLR/BIST}$, NR Leakage Current		$V_{\overline{CLR/BIST}}$ = V_{DD}, V_{NR} = V_{DD}	-0.1		+0.1	µA

Electrical Characteristics (continued)

(V_{DD} = 1.71V to 5.5V. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT VOLTAGE ($\overline{RST}$, $\overline{OV}$, $\overline{BIST}$)						
Output Voltage Low	V_{OL}	$\overline{RST}$, $\overline{OV}$, $\overline{BIST}$, V_{DD} = 5V, I_{SINK} = 3mA		0.1	0.3	V
		$\overline{RST}$, $\overline{OV}$, $\overline{BIST}$, V_{DD} = 1.71V, I_{SINK} = 8µA		0.1	0.3	
		$\overline{RST}$ V_{DD} = 1.1V, I_{SINK} = 8µA		0.1	0.3	

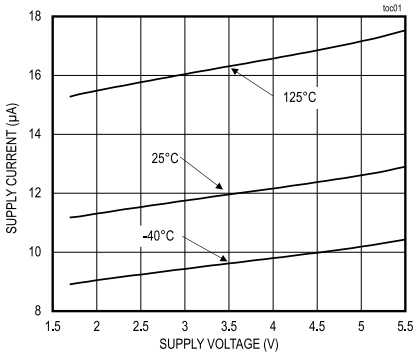
Note 1: Outputs are guaranteed to be in correct state down to V_{DD} = 1.1V.

Note 2: Minimum pulse required to clear $\overline{OV}$ latched state. No overvoltage fault present and $\overline{RST}$ = high.

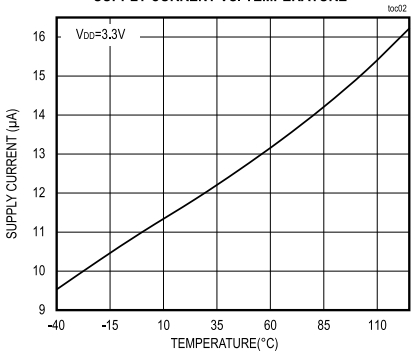
Typical Operating Characteristics

(V_{DD} = 1.71V to 5.5V, T_A = -40°C to 125°C, Typical values are at V_{DD} = 3.3V, unless otherwise specified.)

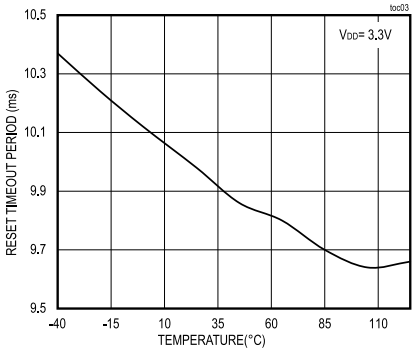
SUPPLY CURRENT VS. SUPPLY VOLTAGE



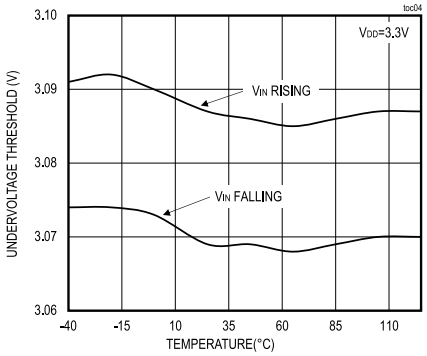
SUPPLY CURRENT VS. TEMPERATURE



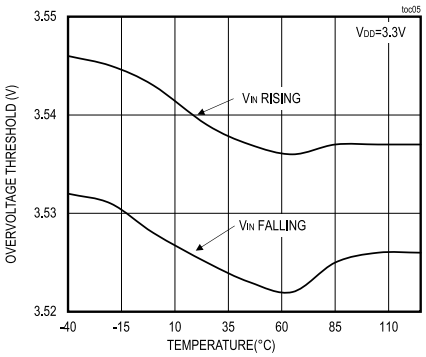
RESET TIMEOUT PERIOD VS. TEMPERATURE



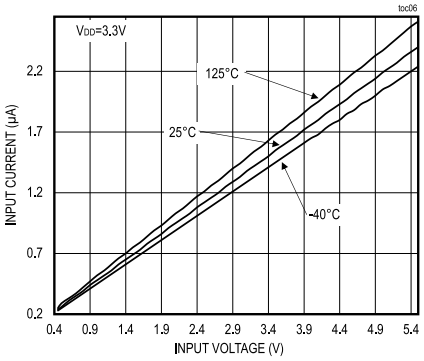
UNDERVOLTAGE THRESHOLD VS. TEMPERATURE



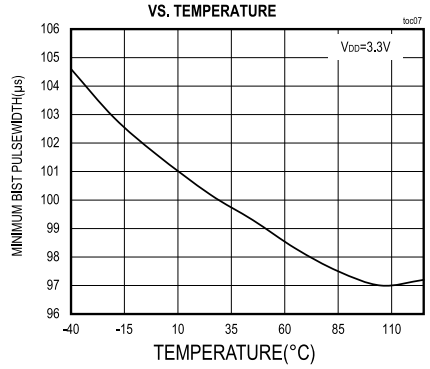
OVERVOLTAGE THRESHOLD VS. TEMPERATURE



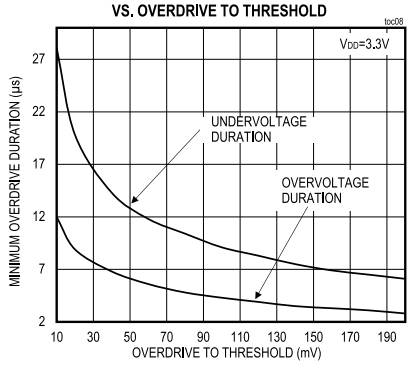
INPUT CURRENT VS. INPUT VOLTAGE



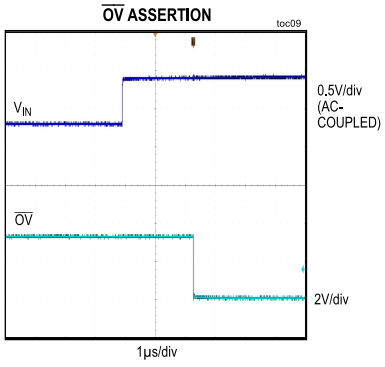
MINIMUM BIST PULSEWIDTH VS. TEMPERATURE



MINIMUM OVERDRIVE DURATION VS. OVERDRIVE TO THRESHOLD

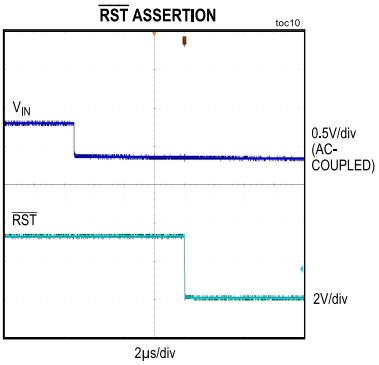


$\overline{OV}$ ASSERTION



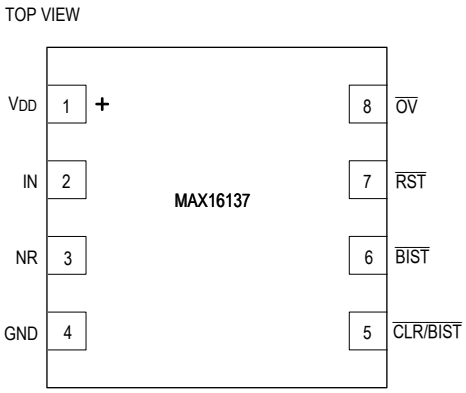
Typical Operating Characteristics (continued)

(V_{DD} = 1.71V to 5.5V, T_A = -40°C to 125°C, Typical values are at V_{DD} = 3.3V, unless otherwise specified.)



Pin Configuration

8 TDFN



Pin Description

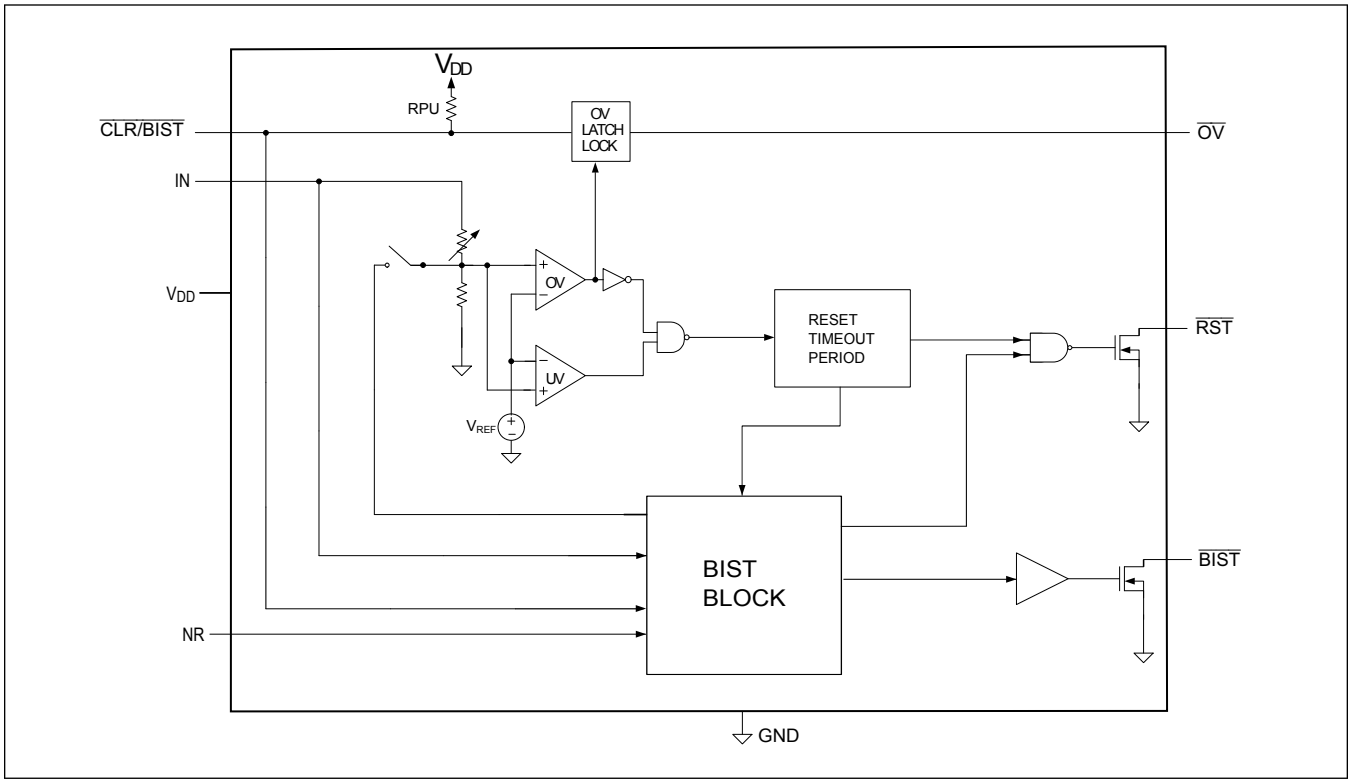
PIN	NAME	FUNCTION
1	VDD	Supply Input. Bypass V_{DD} to ground with a 0.1µF capacitor.
2	IN	Monitoring Input IN is a factory-set threshold monitoring input. When V_{IN} falls outside the factory selected undervoltage/overvoltage threshold window, $\overline{RST}$ asserts and stays asserted for a selected reset timeout period after V_{IN} falls within the undervoltage/overvoltage threshold window. When V_{IN} exceeds the overvoltage threshold, $\overline{OV}$ asserts and indicates an overvoltage fault.
3	NR	No Reset BIST Logic Input. Setting NR to a logic low and driving $\overline{CLR/BIST}$ low for more than 150µs initiates BIST and asserts the reset output and $\overline{BIST}$ if BIST fails. Setting NR to a logic high and driving $\overline{CLR/BIST}$ low for more than 150µs initiates BIST and asserts $\overline{BIST}$ only if BIST fails.
4	GND	Ground.
5	$\overline{CLR/BIST}$	Overvoltage Clear/Built-In-Self-Test Input. $\overline{CLR/BIST}$ is a multiplexed function input. A falling edge on $\overline{CLR/BIST}$ clears $\overline{OV}$ latch.Drving $\overline{CLR/BIST}$ for more than 150µs initiates BIST.

Pin Description (continued)

PIN	NAME	FUNCTION
6	$\overline{BIST}$	Active-Low, Open-Drain Output. $\overline{BIST}$ asserts low if BIST fails. Pull $\overline{BIST}$ to VDD with a pullup resistor.
7	$\overline{RST}$	Open-Drain Reset Output. $\overline{RST}$ asserts low when V_{IN} falls outside of the undervoltage/overvoltage threshold window. The reset output deasserts after the reset timeout period when V_{IN} enters the undervoltage/overvoltage threshold window.
8	$\overline{OV}$	Open-Drain, Active-Low Overvoltage Latched Fault Output. $\overline{OV}$ latches low when the voltage at IN exceeds the overvoltage threshold setting. $\overline{OV}$ latch is cleared on the falling edge of $\overline{CLR/BIST}$.

Functional Diagrams

Internal Block Diagram



Detailed Description

The MAX16137 is a high-accuracy single-channel supervisory reset circuit that monitors the system supply for undervoltage and overvoltage faults within factory-programmable window thresholds. The MAX16137's Buit-In-Self-Test ($\overline{BIST}$) diagnostic capability and overvoltage fault output optimizes system safety in ADAS applications. A reset output ($\overline{RST}$) asserts when the input voltage falls outside of the threshold-window. The reset output deasserts after the reset timeout period when the supply voltage returns back to its nominal voltage level.

Norminal Input Threshold Range

The MAX16137 offers a wide range of nominal input voltages from 0.5V to 5V in approximately 20mV increment. Each selected nominal input voltage is factory-trimmed halfway between the undervoltage and overvoltage threshold window. See the *Undervoltage/Overvoltage Thresholds* section for more details. Contact Maxim sales for options not listed in the *Ordering Information* table.

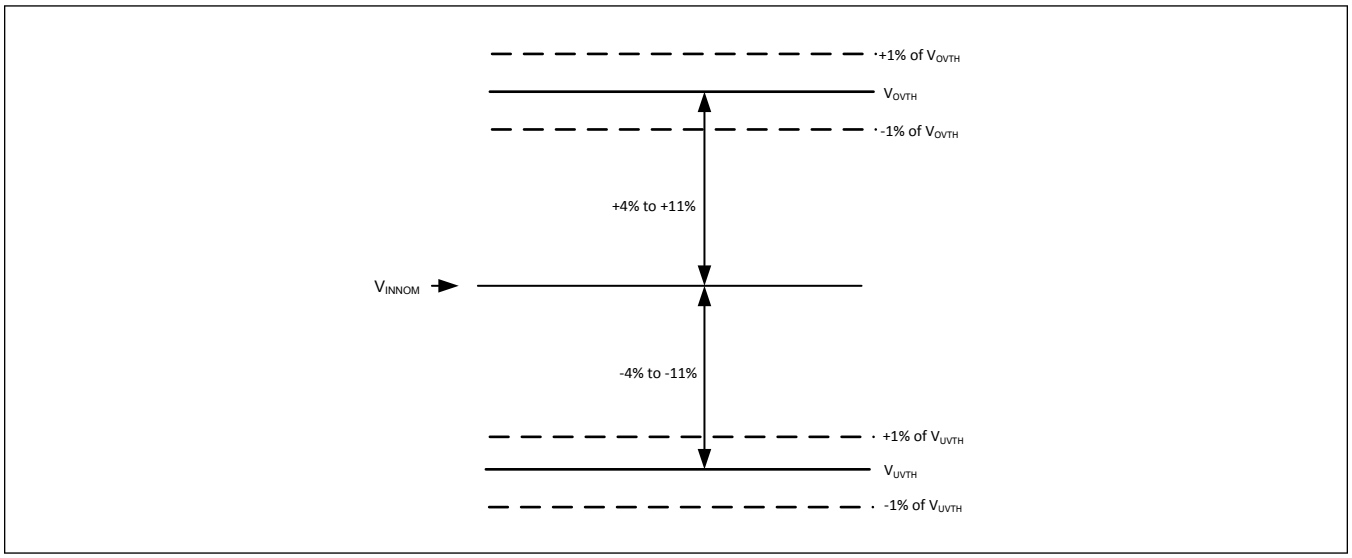


Figure 1. Undervoltage/Overvoltage Threshold Tolerance and Accuracy

Undervoltage/Overvoltage Thresholds

The MAX16137 monitors supply voltage for undervoltage/overvoltge faults with respect to nominal input voltage within ±1% accuracy over the operating temperature and supply ranges. The undervoltage and overvoltage thresholds are factory-trimmed from ±4% to ±11% in ±1% increments. Contact Maxim for threshold not listed in the *Ordering Information* table.

Undervoltage/Overvoltage Threshold Hysteresis

The monitoring input (IN) features undervoltage/overvoltage threshold hysteresis that provides immunity to short input transients. The input hysteresis is factory-set to either 0.25% or 0.5% and is applicable to both the undervoltage and overvoltage thresholds. Contact Maxim for hysteresis option not listed in the *Ordering Information* table.

Overvoltage Fault Output

$\overline{OV}$ is an open-drain, active-low latched output that latches low 5µs after V_{IN} exceeds the overvotlge threshold level. $\overline{OV}$ latch is cleared on the falling edge of $\overline{CLR/BIST}$ after the overvoltage fault is removed. See the Electrical Characteristics table and following Figure 2 for more details.

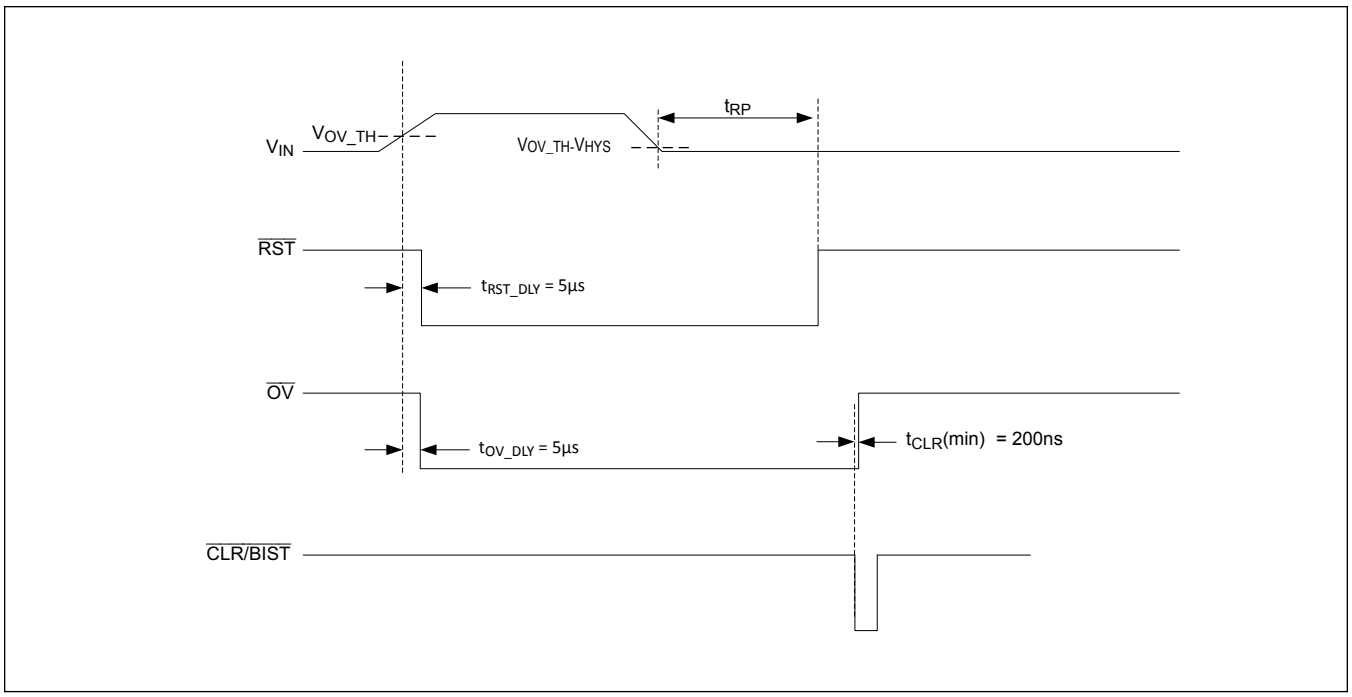


Figure 2. Clear Input Timing Diagram

Built-In-Self-Test (BIST)

BIST is a diagnostic feature that monitors the health of the MAX16137. BIST is initiated during power-up and completes after the expiration of the reset timeout period. During power-up, the MAX16137 monitors the state of the reset output. A high-logic reset output status during power-up indicates a fault either inside or outside the MAX16137, and $\overline{BIST}$ is pulled low. See the following Figure 3 at T1. After the expiration of the reset timeout period, the MAX16137 generates internally fictitious undervoltage and overvoltage fault scenarios, and $\overline{RST}$ deasserts. If the MAX16137 internal circuit does not respond properly to the internally generated undervoltage and overvoltage faults, $\overline{BIST}$ and $\overline{RST}$ are pulled low. See the following Figure 3 at T2 and T3. Then the MAX16137 monitors the state of the reset output again. A low-logic reset output status indicates a fault either inside or outside the MAX16137 and $\overline{BIST}$ is pulled low. See the following Figure 3 at T4.

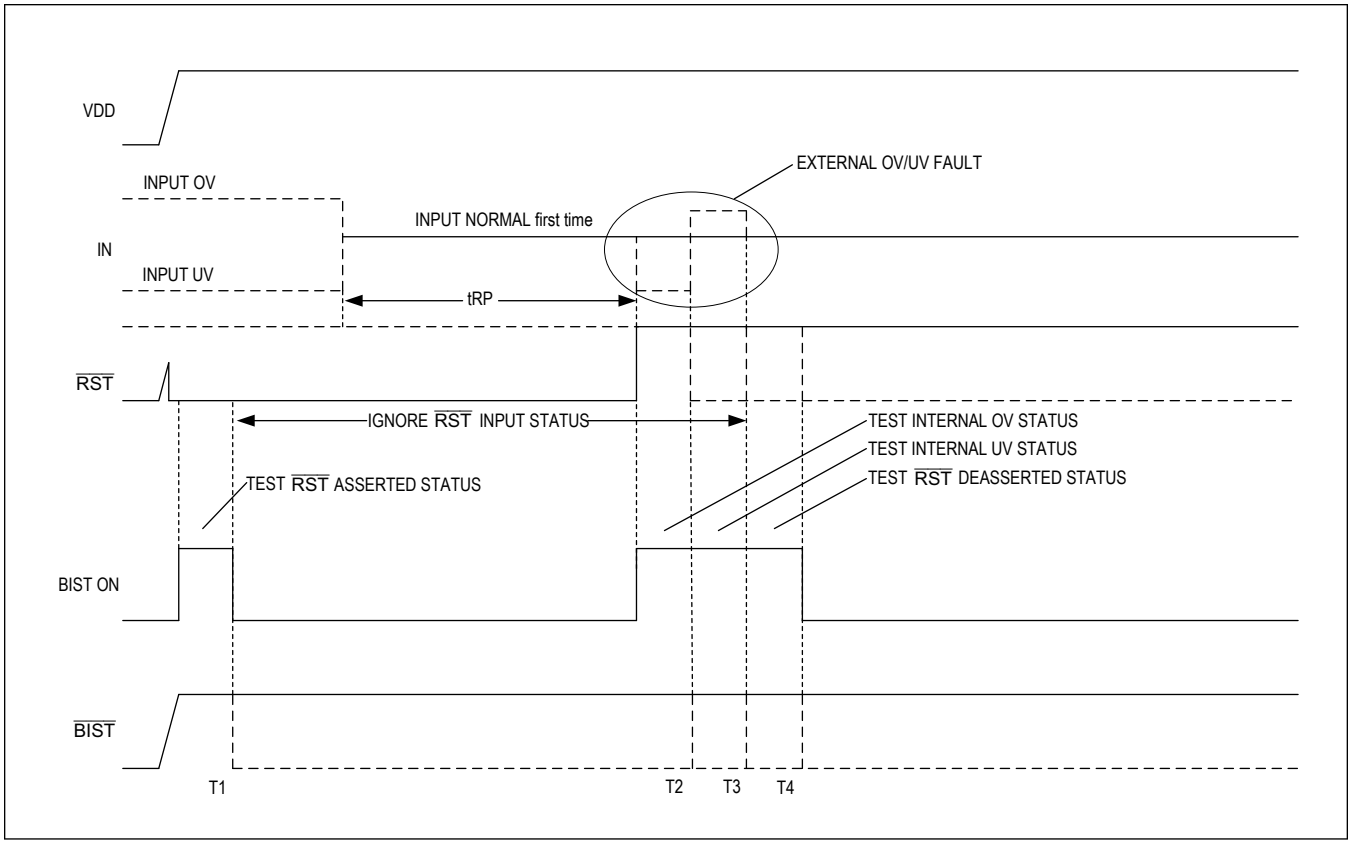


Figure 3. MAX16137 BIST Timing Relationship

On-Demand BIST

On-demand BIST allows the MAX16137 to initiate BIST during normal operation. On-demand BIST is initiated when $\overline{CLR/BIST}$ is pulled low for more than t_{BIST}. See the Electrical Characteristic table for more details. If $\overline{CLR/BIST}$ is pulled low for less than t_{BIST}, or if the input is overvoltage or undervoltage before the expiration of t_{BIST}, on-demand BIST is ignored.

With NR at logic low and $\overline{CLR/BIST}$ is pulled low for more than t_{BIST}, on-demand BIST operation is similar to that of power-up: The MAX16137 pulls the reset output low during the internal OV and UV testing while keeping the system in reset, Figure 4. When NR is at logic high and $\overline{CLR/BIST}$ is pulled low for more than t_{BIST}, on-demand BIST operation is carried out without pulling the reset output low. See the following Figure 5 for more details.

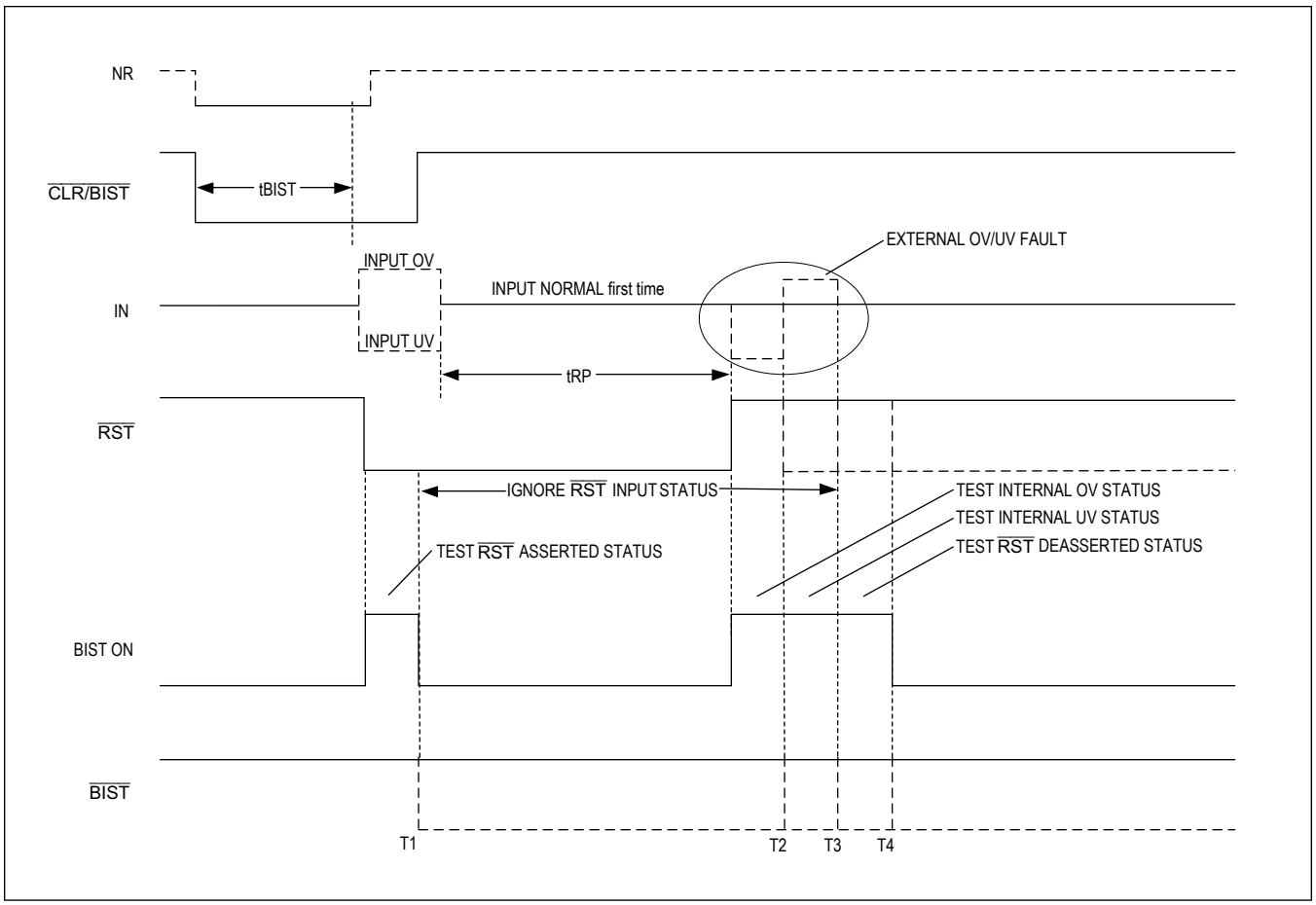


Figure 4. MAX16137 On-Demand BIST Timing with NR = LOW

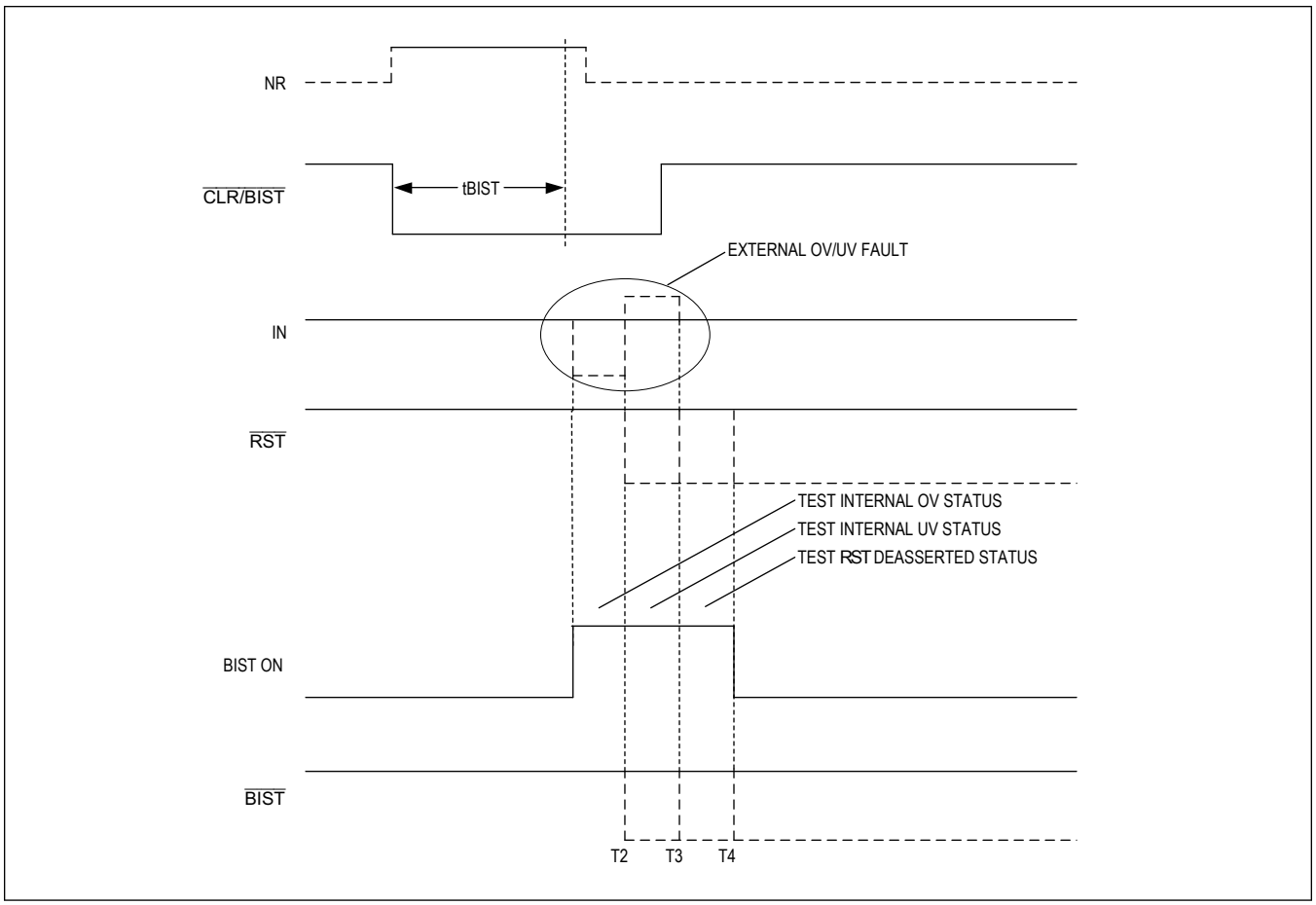


Figure 5. MAX16137 On-Demand BIST Timing with NR = HIGH

Reset Timeout Period

The active-low, open-drain reset output ($\overline{RST}$) asserts low when the input voltage falls outside the set undervoltage and overvoltage window threshold. The reset output deasserts after the reset timeout period when the input voltage falls within the set window threshold. At power-up, the resets stay asserted for the reset timeout period once V_{DD} is above the UVLO. The reset output requires a pullup resistor to V_{DD}. The MAX16137 offers 16 factory-set reset timeout periods.The MAX16137 offers both open-drain and push-pull reset output options. See Table 1 for available options and Figure 6 for more details.

Table 1. Reset Timeout Options

MIN RESET TIMEOUT PERIOD
1ms
5ms
10ms
15ms
20ms
50ms
100ms
150ms

Table 1. Reset Timeout Options (continued)

200ms
250ms
300ms
500ms
750ms
1000ms
15000ms

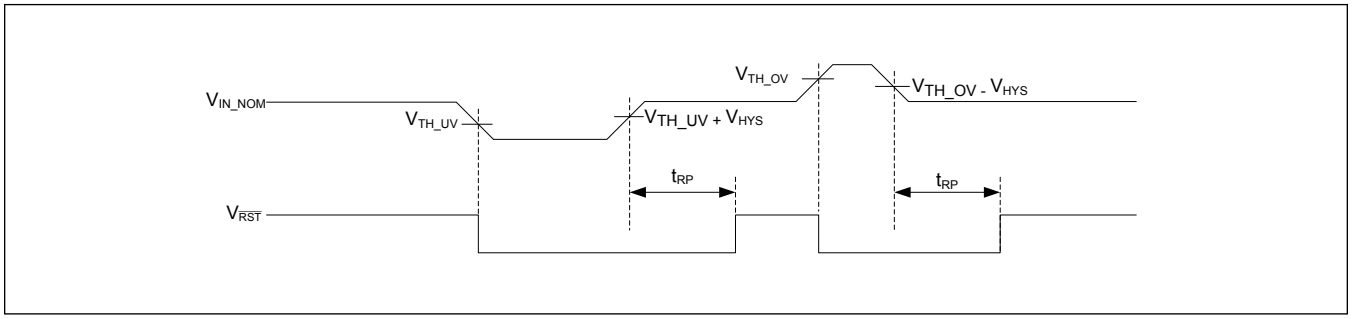


Figure 6. Reset Output Timing Diagram

Applications Information

Setting Input Thresholds and Hystersis

The MAX16137 monitors a system supply voltage for undervoltage/overvoltage window threshold. Depending on the system supply tolerance requirement, the undervoltage/overvoltage thresholds can be factory-trimmed from ±4% to ±11%. The tolerance setting is symmetrical with respect to the selected nominal input threshold voltage (V_{IN_NOM}). A detailed calculation of how to determine the undervoltage/overvoltage threshold levels with ±1% threshold accuracy for 3.3V ±5% supply voltage is presented here:

V_{IN_NOM} = 3.3V

TOL = ± 5%

$V_{UVTH} = V_{IN\_NOM} (1 - 5\%) = 3.3V (1 - 0.05) = 3.135V$

$V_{OVTH} = V_{IN\_NOM} (1 + 5\%) = 3.3V (1 + 0.05) = 3.465V$

where V_{IN_NOM} is the selected nominal input threshold voltage, TOL is the input tolerance, V_{UVTH} is undervotlage threshold voltage, and V_{OVTH} is the overvoltage threshold voltage.

The MAX16137 monitors the supply voltage with ±1% accuracy over the operating temperature and supply range. The accuracy range for the 3.3V ±5% is as following:

$V_{UVTH\_A} = V_{UVTH} (1 \pm 1\%) = 3.135V (1 \pm 0.01) = 3.135V \pm 0.03135V$

$V_{OVTH\_A} = V_{OVTH} (1 \pm 1\%) = 3.465V (1 \pm 0.01) = 3.465V \pm 0.03465V$

where V_{UVTH_A} is the undervoltage threshold accuracy range and V_{OVTH_A} is the overvoltage threshold accuracy range. See Figure 7 for details.

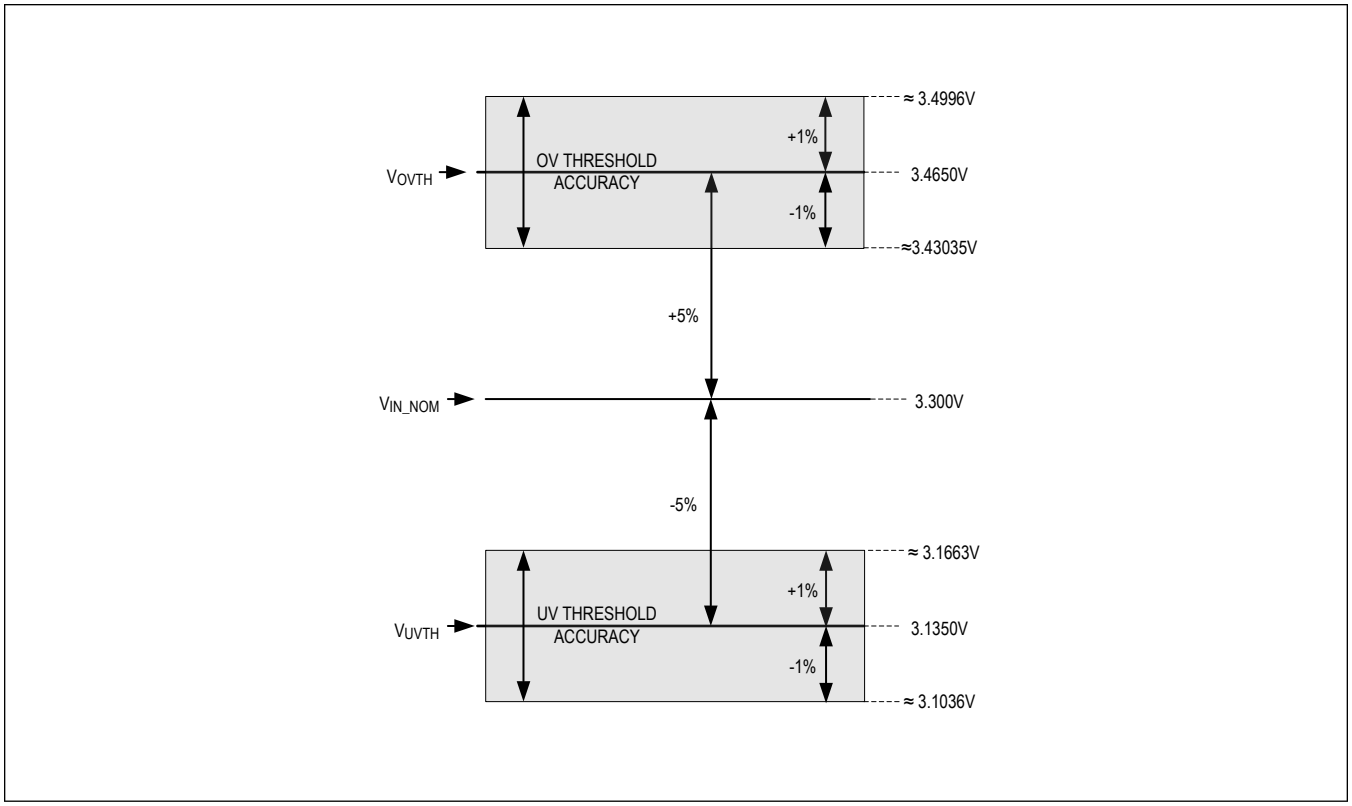


Figure 7. Undervoltage/Overvoltage Threshold Accuracy

Hysteresis adds noise immunity to the voltage monitors and prevents oscillation due to repeated triggering when the monitored voltage is near the threshold trip voltage.

A detailed calculation to get the threshold hysteresis is presented here.

V_{IN_NOM} = 3.3V

Hysteresis = 0.5%

V_{HYST} = 3.3V*0.5%=0.0165V

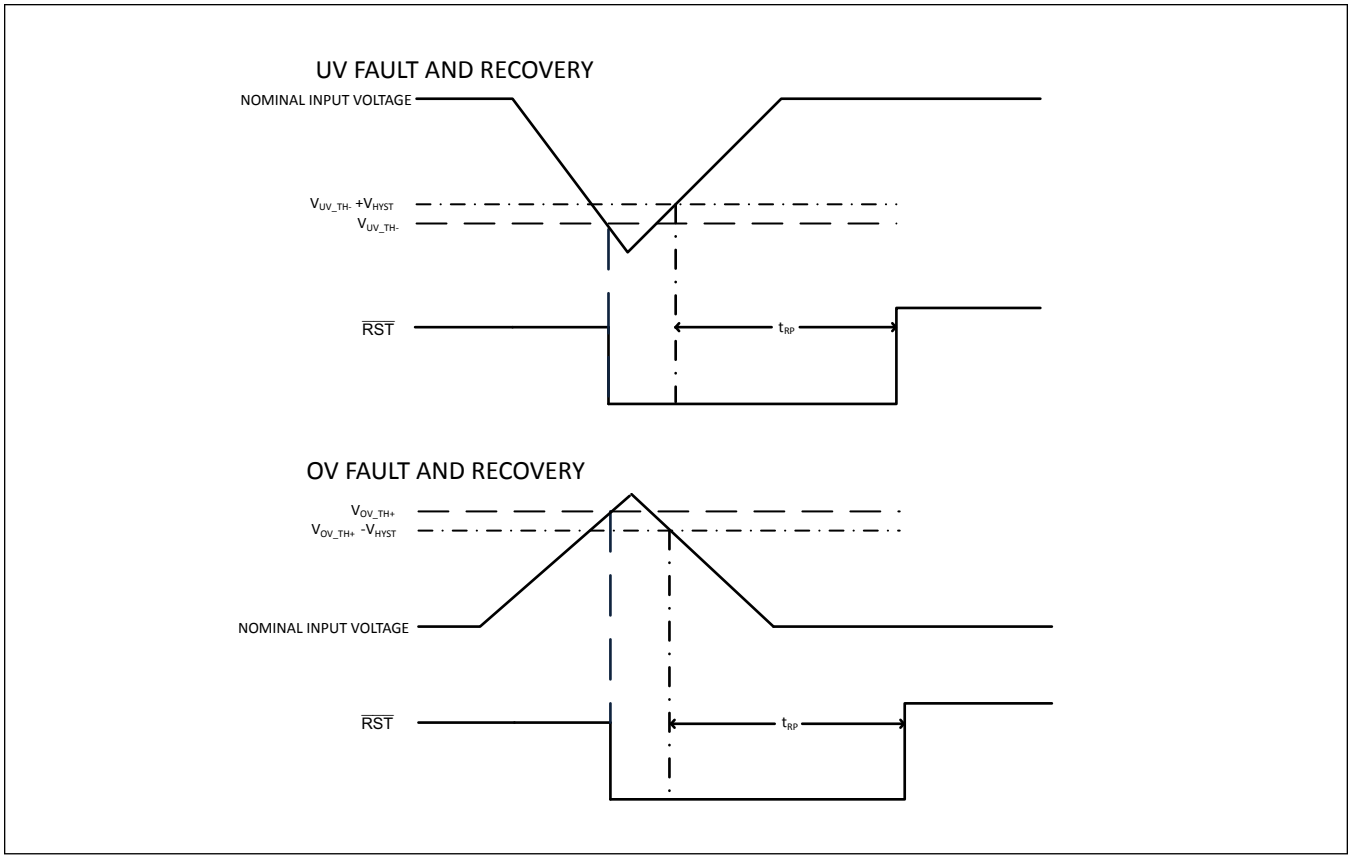


Figure 8. Undervoltage/Overvoltage Threshold Hysteresis

Power-Supply Bypassing/Noise Immunity

The MAX16137 operates from a 1.71V to 5.5V supply.Bypass V_{DD} to ground with a 0.1µF capacitor as close to the device as possible. An additional capacitor improves transient immunity.

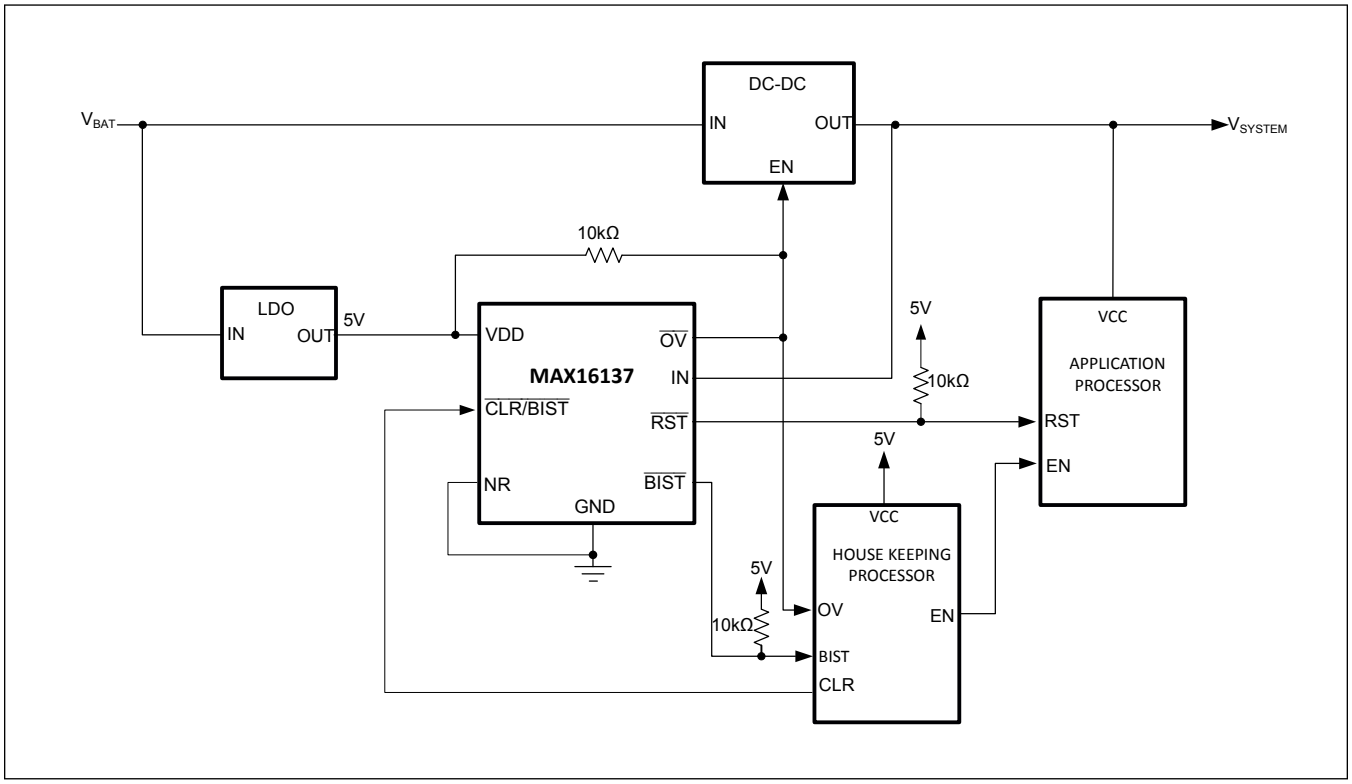
Selector Guide Table

Table 2. Selector Guide Table

PART NUMBER	THRESHOLD VOLTAGE	TOLERANCE	HYSTERESIS	RESET TIMEOUT
MAX1613700/VY+T	3.3V	7%	0.5%	10ms

Typical Application Circuits

Typical Application Circuit



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX1613700/VY+T	-40°C to +125°C	8-TDFN
MAX16137P01/VY+T*	-40°C to +125°C	8-TDFN

/V denotes automotive grade.

Y denotes side-wettable package.

+ denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

** Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	08/20	Initial release	—
	02/21	Release for market intro	—