



Product Change Notification - SYST-24YDSF264

Date:

25 Jun 2020

Product Category:

8-bit Microcontrollers

Affected CPNs:



Notification subject:

ERRATA - AVR32DA28/32/48 Silicon Errata and Data Sheet Clarification

Notification text:

SYST-24YDSF264

Microchip has released a new Product Documents for the AVR32DA28/32/48 Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at [AVR32DA28/32/48 Silicon Errata and Data Sheet Clarification](#).

Notification Status: Final

Description of Change: Initial document release

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 25 Jun 2020

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

[AVR32DA28/32/48 Silicon Errata and Data Sheet Clarification](#)

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Affected Catalog Part Numbers (CPN)

AVR32DA28-I/SO
AVR32DA28-I/SP
AVR32DA28-I/SS
AVR32DA28T-I/SO
AVR32DA28T-I/SS
AVR32DA32-I/PT
AVR32DA32-I/RXB
AVR32DA32T-I/PT
AVR32DA32T-I/RXB
AVR32DA48-I/6LX
AVR32DA48-I/PT
AVR32DA48T-I/6LX
AVR32DA48T-I/PT

SYST-24YDSF264 - ERRATA - AVR32DA28/32/48 Silicon Errata and Data Sheet Clarification

Affected Catalog Part Numbers(CPN)

AVR32DA28-I/SO
AVR32DA28-I/SP
AVR32DA28-I/SS
AVR32DA28T-I/SO
AVR32DA28T-I/SS
AVR32DA32-I/PT
AVR32DA32-I/RXB
AVR32DA32T-I/PT
AVR32DA32T-I/RXB
AVR32DA48-I/6LX
AVR32DA48-I/PT
AVR32DA48T-I/6LX
AVR32DA48T-I/PT



AVR32DA28/32/48

Silicon Errata and Data Sheet Clarification

The AVR32DA28/32/48 devices you have received conform functionally to the current device data sheet (microchip.com/DS40002228), except for the anomalies described in this document. The erratas described in this document will likely be addressed in future revisions of the AVR32DA28/32/48 devices.

Notes:

- This document summarizes all the silicon errata issues from all revisions of silicon, previous as well as current.
- Refer to the Device/Revision ID section in the current device data sheet (microchip.com/DS40002228) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance.

1. Silicon Issue Summary

Legend

- Erratum is not applicable.
- X Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision
		Rev. A3 ^(*)
PORT	2.2.1 Digital Input on Pin Automatically Disabled When Pin Selected for Analog Input	X
TWI	2.3.1 The Output Pin Override Does Not Function as Expected	X
USART	2.4.1 Open-Drain Mode Does Not Work When TXD is Configured as Output	X
ZCD	2.5.1 ZCD Output Selection Bits Should Be Individual Bits	X

Note:

(*) This revision is the initial release of the silicon.

2. Silicon Errata Issues

2.1 Errata Details

- Erratum is not applicable.
- X Erratum is applicable.

2.2 PORT - I/O Pin Configuration

2.2.1 Digital Input on Pin Automatically Disabled When Pin Selected for Analog Input

If an input pin is selected to be analog input, the digital input function for those pins is automatically disabled.

Work around

None.

Affected Silicon Revisions

Rev. A3
X

2.3 TWI - Two-Wire Interface

2.3.1 The Output Pin Override Does Not Function as Expected

When TWI is enabled it overrides the output pin driver, but not the output value. So when the value in the PORT Out (PORTx.OUT) register is '1', for the pins corresponding to the SDA or SCL, the output on the line will always be high.

Work around

Ensure that the value in the PORTx.OUT register corresponding to the SCL and SDA pins are '0' before enabling the TWI.

Affected Silicon Revisions

Rev. A3
X

2.4 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.4.1 Open-Drain Mode Does Not Work When TXD is Configured as Output

When the USART TXD pin is configured as an output, it can drive the pin high regardless of whether the Open-Drain mode is enabled or not.

Work around

Configure the TXD pin as an input by writing the corresponding bit in PORTx.DIR to '0' when using Open-Drain mode.

Affected Silicon Revisions

Rev. A3
X

2.5 ZCD - Zero-Cross Detector**2.5.1 ZCD Output Selection Bits Should Be Individual Bits**

The ZCD1 and ZCD2 output selection bits in the ZCDROUTEA register are tied to the ZCD0 bit. When writing a value to the ZCD0 bit, all three ZCD outputs are switched from the default pin setting to the alternative pin setting. When writing to either ZCD1 or ZCD2 bits, nothing happens.

Work around

None.

Affected Silicon Revisions

Rev. A3
X

3. Data Sheet Clarifications

None.

4. Document Revision History

Note: The data sheet clarification document revision is independent of the die revision and the device variant (last letter of the ordering number).

4.1 Revision History

Doc. Rev.	Date	Comments
A	06/2020	Initial document release

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