MOSFETs Silicon N-channel MOS (U-MOSIX-H)

TPH5R60APL

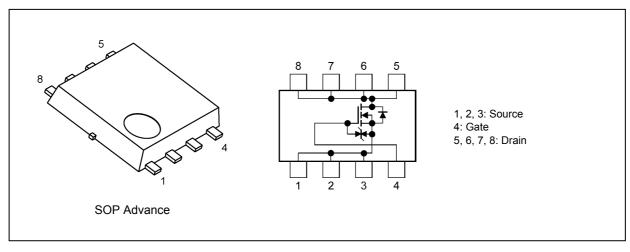
1. Applications

- High-Efficiency DC-DC Converters
- Switching Voltage Regulators
- Motor Drivers

2. Features

- (1) High-speed switching
- (2) Small gate charge: $Q_{SW} = 14 \text{ nC}$ (typ.)
- (3) Small output charge: $Q_{oss} = 46 \text{ nC}$ (typ.)
- (4) Low drain-source on-resistance: $R_{DS(ON)} = 4.7 \text{ m}\Omega$ (typ.) (V_{GS} = 10 V)
- (5) Low leakage current: $I_{DSS} = 10 \ \mu A \ (max) \ (V_{DS} = 100 \ V)$
- (6) Enhancement mode: V_{th} = 1.5 to 2.5 V (V_{DS} = 10 V, I_D = 0.5 mA)

3. Packaging and Internal Circuit



4. Absolute Maximum Ratings (Note) ($T_a = 25 \text{ °C}$ unless otherwise specified)

Characteristics			Symbol	Rating	Unit
Drain-source voltage			V _{DSS}	100	V
Gate-source voltage			V _{GSS}	±20	
Drain current (DC)	(T _c = 25 °C)	(Note 1), (Note 2)	Ι _D	60	A
Drain current (DC)	(Silicon limit)	(Note 1), (Note 2)	Ι _D	110	
Drain current (pulsed)	(t = 100 μs)	(Note 1)	I _{DP}	300	
Power dissipation	(T _c = 25 °C)		PD	132	W
Power dissipation		(Note 3)	PD	3	
Power dissipation		(Note 4)	PD	0.96	
Single-pulse avalanche energy		(Note 5)	E _{AS}	63	mJ
Single-pulse avalanche current		(Note 5)	I _{AS}	60	A
Channel temperature			T _{ch}	175	°C
Storage temperature			T _{stg}	-55 to 175	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

5. Thermal Characteristics

Characteri	Symbol	Max	Unit		
Channel-to-case thermal resistance	(T _c = 25 °C)		R _{th(ch-c)}	1.13	°C/W
Channel-to-ambient thermal resistance	(T _a = 25 °C)	(Note 3)	R _{th(ch-a)}	50	
Channel-to-ambient thermal resistance	(T _a = 25 °C)	(Note 4)	R _{th(ch-a)}	156	

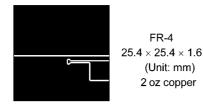
Note 1: Ensure that the channel temperature does not exceed 175 °C.

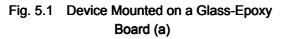
Note 2: Limited by silicon chip capability.

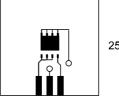
Note 3: Device mounted on a glass-epoxy board (a), Figure 5.1

Note 4: Device mounted on a glass-epoxy board (b), Figure 5.2

Note 5: V_DD = 60 V, T_ch = 25 °C (initial), L = 19 $\mu H, \, I_{AS}$ = 60 A







FR-4 25.4 × 25.4 × 1.6 (Unit: mm) 2 oz copper

Fig. 5.2 Device Mounted on a Glass-Epoxy Board (b)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

6. Electrical Characteristics

6.1. Static Characteristics (Ta = 25 °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current	I _{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	_		±10	μA
Drain cut-off current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V	_		10	μA
Drain-source breakdown voltage	V _{(BR)DSS}	I _D = 10 mA, V _{GS} = 0 V	100	_	—	V
Drain-source breakdown voltage (Note 6)	V _{(BR)DSX}	I _D = 10 mA, V _{GS} = -20 V	65	_	—	
Gate threshold voltage	V _{th}	V _{DS} = 10 V, I _D = 0.5 mA	1.5		2.5	
Drain-source on-resistance	R _{DS(ON)}	V _{GS} = 4.5 V, I _D = 15 A	_	6.3	9.5	mΩ
		V _{GS} = 10 V, I _D = 30 A		4.7	5.6	

Note 6: If a reverse bias is applied between gate and source, this device enters V_{(BR)DSX} mode. Note that the drainsource breakdown voltage is lowered in this mode.

6.2. Dynamic Characteristics ($T_a = 25$ °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Input capacitance	C _{iss}	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz	_	3300	4300	pF
Reverse transfer capacitance	C _{rss}		_	27	56	
Output capacitance	C _{oss}		_	410	_	
Gate resistance	r _g	—	—	2.1	3.2	Ω
Switching time (rise time)	tr	See Fig. 6.2.1	_	8	—	ns
Switching time (turn-on time)	t _{on}		_	19	_	
Switching time (fall time)	t _f]		14	_	
Switching time (turn-off time)	t _{off}			54	_	

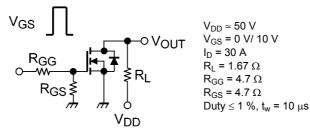


Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics ($T_a = 25$ °C unless otherwise specified)

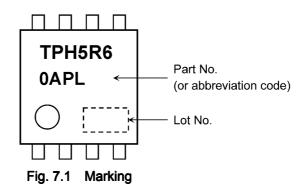
Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Total gate charge (gate-source plus	Qg	$V_{DD}\approx 50$ V, V_{GS} = 10 V, I_{D} = 30 A	_	52	_	nC
gate-drain)		$V_{DD}\approx 50$ V, V_{GS} = 4.5 V, I_{D} = 30 A	—	26	_	
Gate-source charge 1	Q _{gs1}	$V_{DD} \approx 50$ V, V_{GS} = 10 V, I_D = 30 A	_	12	_	
Gate-drain charge	Q _{gd}		_	9	_	
Gate switch charge	Q _{SW}		—	14	_	
Output charge	Q _{oss}	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz	_	46	_	

6.4. Source-Drain Characteristics ($T_a = 25$ °C unless otherwise specified)

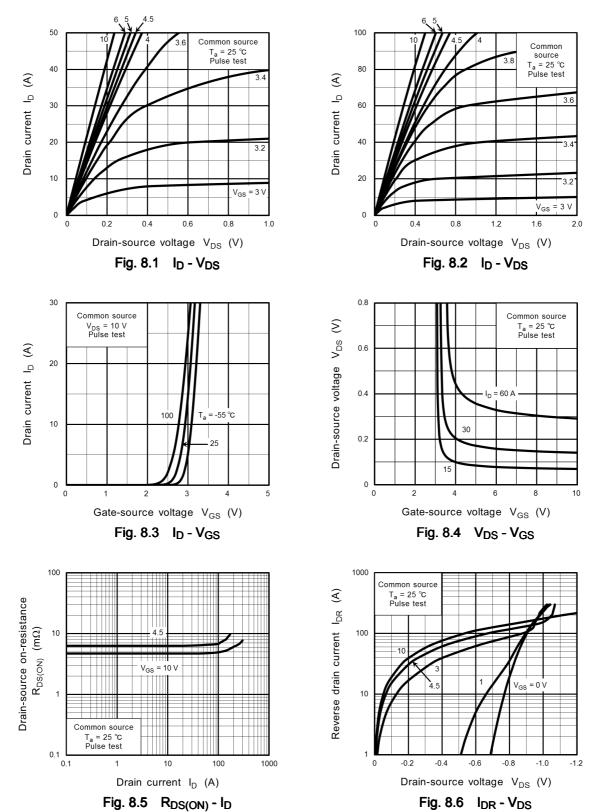
Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Reverse drain current (pulsed) (Note	') I _{DRP}	t = 100 μs	_	—	300	A
Diode forward voltage	V _{DSF}	I _{DR} = 60 A, V _{GS} = 0 V	_	_	-1.2	V
Reverse recovery time	t _{rr}	I _{DR} = 15 A, V _{GS} = 0 V,	_	44	_	ns
Reverse recovery charge	Q _{rr}	-dl _{DR} /dt = 100 A/μs	—	55	_	nC

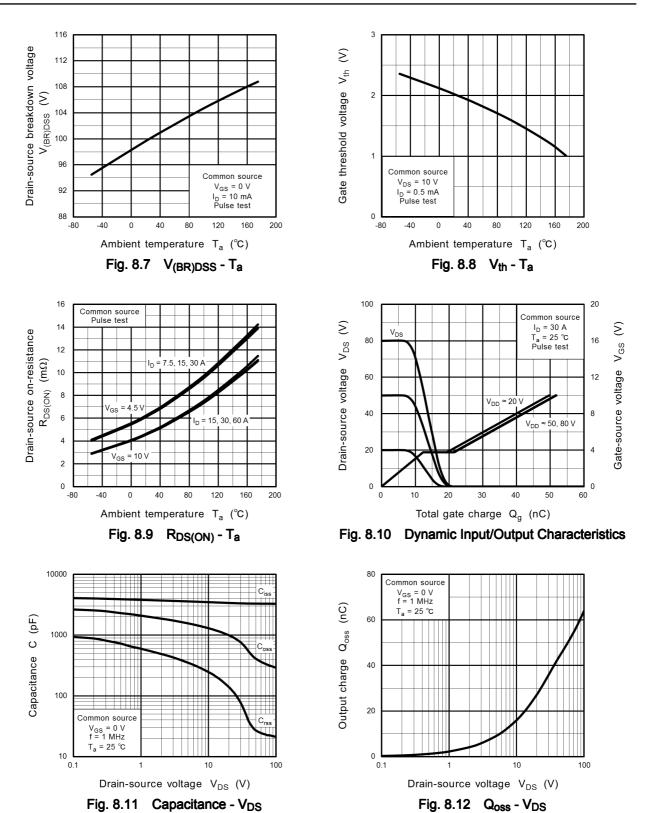
Note 7: Ensure that the channel temperature does not exceed 175 °C.

7. Marking



8. Characteristics Curves (Note)

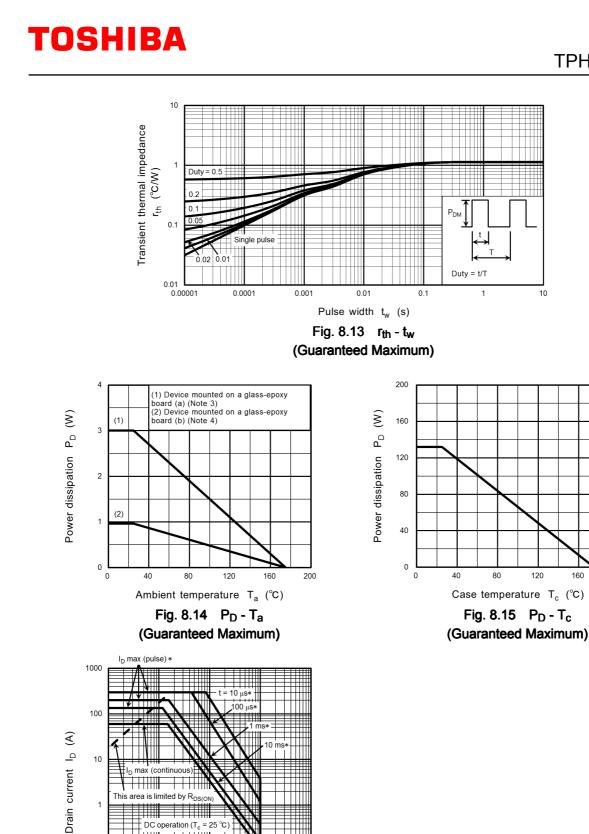




10

160

200



DSS max

100

1111

1000

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

*: Single pulse T_c = 25 °C Curves must be derated linearly with increase in temperature.

1

10

0.1

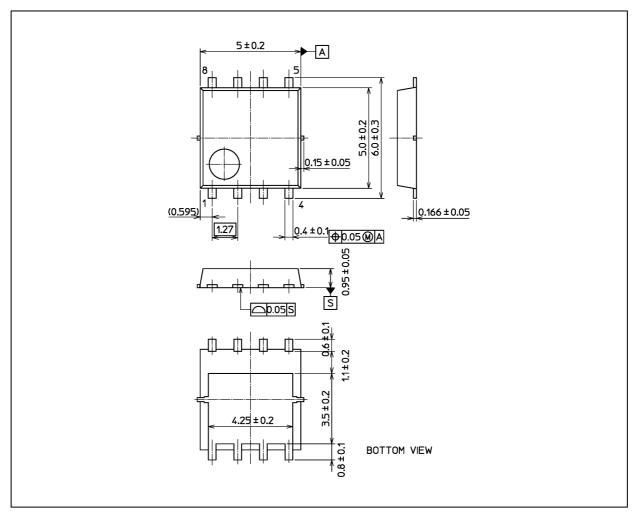
0.01

0.1

TPH5R60APL

Package Dimensions

Unit: mm



Weight: 0.079 g (typ.)

TOSHIBA: 2-5Q1S

Nickname: SOP Advance

Package Name(s)

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