0 Hz/dc to 14 GHz, Single-Pole, Four-Throw MEMS Switch with Integrated Driver

Data Sheet **ADGM1304**

FEATURES

- Fully operational down to 0 Hz/dc
  - On resistance: 2.9 Ω (maximum)
  - Off leakage: 0.5 nA (maximum)
- −3 dB bandwidth
  - 11 GHz (typical) for RF1, RF4
  - 14 GHz (typical) for RF2, RF3
- RF performance characteristics
  - Insertion loss: 0.26 dB (typical) at 2.5 GHz
  - Isolation: 24 dB (typical) at 2.5 GHz
  - IIP3: 69 dBm (typical)
  - RF power: 36 dBm (maximum)
- Actuation lifetime: 1 billion cycles (minimum)
  - Hermetically sealed switch contacts
  - On switching time: 75 µs (maximum)
- Integrated driver removes the need for an external driver
  - Supply voltage: 3.0 V to 3.6 V
  - CMOS/LVTTL compatible
  - Parallel and SPI interface
  - Independently controllable switches
- Switch is in an open state with no power supply present
- Requirement to avoid floating nodes on all RFx pins (see the Floating Node section)
- 24-lead, 5 mm × 4 mm × 0.95 mm, LFCSP
- Operating temperature range: 0°C to 85°C

APPLICATIONS

- Relay replacements
- Automatic test equipment: RF/high speed digital and mixed signals
- Load and probe boards: RF/high speed digital and mixed signals
- RF test instrumentation
- Reconfigurable filters and attenuators
- High performance RF switching

GENERAL DESCRIPTION

The ADGM1304 is a wideband, single-pole, four-throw (SP4T) switch, fabricated using Analog Devices, Inc., microelectromechanical system (MEMS) switch technology. This technology enables a small form factor, wide RF bandwidth, highly linear, low insertion loss switch that is operational from 0 Hz/dc to 14 GHz, making the ADGM1304 an ideal solution for a wide range of RF and precision equipment switching needs.

An integrated driver chip generates a high voltage to electrostatically actuate a switch that can be controlled by a parallel interface and a serial peripheral interface (SPI). All four switches are independently controllable.

The device is packaged in a 24-lead, 5 mm × 4 mm × 0.95 mm, lead frame chip-scale package (LFCSP).

To ensure optimum operation of the ADGM1304, the Critical Operational Requirements section must be followed exactly.

The on resistance (R_{ON}) performance of the ADGM1304 is affected by device to device variation, channel to channel variation, cycle actuations, settling time post turn on, bias voltage, and temperature changes.

COMPANION PRODUCTS

Quad Parametric Measurement Unit (PMU): AD5522
SP4T MEMS Switch: ADGM1004
Low Noise, LDO Regulators: ADP7142, LT1962, LT3045-1
Additional companion products on the ADGM1304 product page

Rev. H
Document Feedback

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TABLE OF CONTENTS

REVISION HISTORY

2/2022—Rev. G to Rev. H

Changes to Insertion Loss Parameter, Table 1 ... 5
Changes to Figure 5 ... 10
Added Figure 14; Renumbered Sequentially ... 13
Changes to Hot Switching Section ... 30

2/2021—Rev. F to Rev. G

Changes to Features Section ... 1
Added Companion Products Section ... 1
Changes to Note 3, Table 1 ... 6
Added Note 4, Table 1; Renumbered Sequentially ... 6
Deleted Figure 6; Renumbered Sequentially ... 12
Changes to Figure 38 and Figure 39 ... 18
Changes to Figure 42 ... 19
Changes to Figure 44, Figure 45, and Figure 46 ... 20
Changes to Table 6 ... 23
Changes to Addressable Mode Section and Figure 49 Caption ... 24
Added Figure 50; Renumbered Sequentially ... 24
Moved Daisy-Chain Mode Section ... 25
Changes to Typical Operating Circuit Section ... 26
Added Power Supply Rails Section, Power Supply Recommendations Section, Figure 55, and Table 7; Renumbered Sequentially ... 28
Changes to System Error Considerations Due to On-Resistance Drift Section ... 30
Added On-Resistance Shift Due to Temperature Shock Post Actuations Section, Figure 59, Hot Switching Section, and Figure 60 ... 30
Added Figure 61 ... 31
Deleted Table 8; Renumbered Sequentially ... 31
Changes to Mechanical Shock Precautions Section ... 32

1/2020—Rev. E to Rev. F

Changes to Figure 1 ... 4

1/2020—Rev. D to Rev. E

Reorganized Layout ... Universal
Changes to Features Section and General Description Section ... 1
Changes to Table 1 ... 5
Added Timing Characteristics and Table 2; Renumbered Sequentially ... 7
Added Figure 2 to Figure 4; Renumbered Sequentially ... 8

3/2018—Rev. C to Rev. D

10/2016—Revision C: Initial Version

FUNCTIONAL BLOCK DIAGRAM

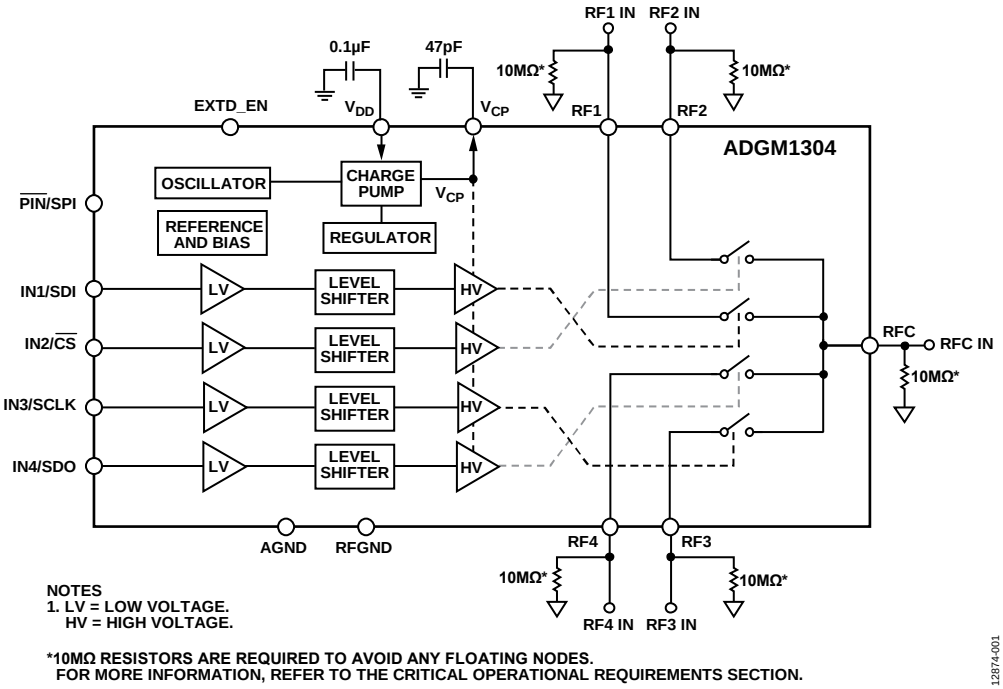

Figure 1.

SPECIFICATIONS

V_{DD} = 3.0 V to 3.6, AGND = 0 V, RFGND = 0 V, all specifications minimum temperature (T_{MIN}) to maximum temperature (T_{MAX}) = 0°C to 85°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions/Comments[2]
ON-RESISTANCE PROPERTIES						See Figure 6 to Figure 12 for more details
Initial On-Resistance Properties						
On Resistance	R_{ON}			2.9	Ω	Drain source current (I_{DS}) = 50 mA, 0 V input bias, at 1 ms after first actuation
On-Resistance Match Between Channels	$\Delta R_{ON\ CH\_CH}$			1	Ω	
On-Resistance Drift						
Over Time[3, 4]	$\Delta R_{ON\ TIME}$			−0.25	Ω	R_{ON} changed from 1 ms to 100 ms after first actuation
Over Actuations[5]	ΔR_{ON}		0.5		Ω	10^9 actuations, switch is actuated at 25°C and R_{ON} is measured at 25°C
				5	Ω	10^9 actuations, switch is actuated at 85°C and R_{ON} is measured at 25°C, 1 kHz actuating frequency, 220 mA load applied between toggles[6]
RELIABILITY PROPERTIES						
Continuously On Lifetime			7.2		Years	Median time before failure at 50°C[7], see Figure 70 for more details
Actuation Lifetime						
Cold Switched		10^9			Actuations	Load between toggling is 220 mA, tested at 85°C
Hot Switched						RF power = continuous wave, terminated into 50 Ω, see Figure 13 for details
10 dBm			5.16×10^9		Actuations	50% of test population failure point (T50)
15 dBm			3.21×10^6		Actuations	50% of test population failure point (T50)
20 dBm			390×10^3		Actuations	50% of test population failure point (T50)
DYNAMIC CHARACTERISTICS						
Operating Frequency		0 Hz/dc		14	GHz	Operating frequency
−3 dB Bandwidth	BW					
RF1, RF4		9.3	11		GHz	RF1 to RFC and RF4 to RFC channels
RF2, RF3		12	14		GHz	RF2 to RFC and RF3 to RFC channels
Insertion Loss	IL		0.26	0.55	dB	At 2.5 GHz, RFC to RFx, maximum specification tested at 25°C
			0.4	0.9	dB	At 6.0 GHz, RFC to RFx, maximum specification tested at 25°C
Isolation	I_{SO}					
RFx To RFC (All Off)		23	24		dB	At 2.5 GHz, RFx to RFC (all channels off)
		16	19		dB	At 6.0 GHz, RFx to RFC (all channels off)
RF1 to RFC			25			At 6 GHz, RF2 to RFC is on, RF1 to RFC is off
RF2 to RFC			23			At 6 GHz, RF1 to RFC is on, RF2 to RFC is off
Crosstalk	C_{TK}	27	30		dB	At 2.5 GHz, RFx to RFx
		22	24		dB	At 6.0 GHz, RFx to RFx
Return Loss	RL	13	18		dB	DC to 6.0 GHz
Input Third-Order Intermodulation Intercept	IP3		69		dBm	Input: 900 MHz and 901 MHz, input power = 27 dBm
Input Second-Order Intermodulation Intercept	IP2		111		dBm	Input: 900 MHz and 901 MHz, input power = 27 dBm
Second Harmonic	HD2		−90		dBc	Input: 5.4 MHz, input power = 0 dBm
			−85		dBc	Input: 150 MHz and 800 MHz, input power = 27 dBm
Third Harmonic	HD3		−85		dBc	Input: 150 MHz and 800 MHz, input power = 27 dBm
Total Harmonic Distortion Plus Noise	THD + N		−110		dBc	Load resistance (R_L) = 300 Ω, f = 1 kHz, RFx = 2.5 V p-p
Maximum RF Power				36	dBm	Switch in the on state and terminated into 50 Ω, maximum specification tested at 25°C
DC Voltage Range		−6		+6	V	On switch dc voltage operation range
On Switching Time[8]	t_{ON}	0		75	µs	50% INx to 90% (0.05 dB of final IL value) RFx, 50 Ω termination

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions/Comments[2]
Off Switching Time[8]	t_{OFF}	0		75	µs	50% INx to 10% (0.05 dB of final IL value) RFx, 50 Ω termination
Actuation Frequency				5	kHz	All switches toggled simultaneously
Power-Up Time			0.75		ms	Charge pump capacitor (C_{CP}) = 47 pF, 95% V_{DD} to 90% RFx
Video Feedthrough			16		mV peak	1 MΩ load at RFx pin
Internal Oscillator Frequency		8	10	12	MHz	
Internal Oscillator Feedthrough[9]			−123		dBm	Spectrum analyzer resolution bandwidth (RBW) = 200 Hz; one switch in on state, all other switches off with 50 Ω terminations[10]
			−146		dBm/Hz	
CAPACITANCE PROPERTIES						At 1 MHz, includes LFCSP package capacitance
On Switch Channel Capacitance	$C_{RF\ ON}$		3.3		pF	
Off Switch Channel Capacitance	$C_{RF\ OFF}$		1.6		pF	
LEAKAGE PROPERTIES						
On Leakage				5	nA	RFx (off channels) = −6 V, RFC to RFx (on channel) = −6 V
Off Leakage				0.5	nA	RFx = 6 V, RFC = −6 V
DIGITAL INPUTS						
Input High Voltage	V_{INH}	2			V	
Input Low Voltage	V_{INL}			0.8	V	
Input Current	I_{INL}/I_{INH}		0.025	1	µA	V_{IN} = V_{INL} or V_{INH}
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	V_{DD} − 0.4 V			V	Source current (I_{SOURCE}) = 1 mA
Output Low Voltage	V_{OL}			0.4	V	Sink current (I_{SINK}) = 1 mA
POWER REQUIREMENTS						
Supply Voltage	V_{DD}	3.0		3.6	V	
Supply Current	I_{DD}			2.5	mA	Digital inputs = 0 V or V_{DD}, serial data out (SDO) is floating in SPI mode
Low Power Mode Current[11]	$I_{DD\ EXT\ VCP}$			50	µA	This value is I_{DD} in low power mode
External Drive Voltage[12]	VCP_{EXT}	79.2	80	80.8	V	
External Drive Current	$I_{CP\ EXT\ VCP}$			20	µA	

[1] Typical specifications tested at 25°C with V_{DD} = 3.3 V.
[2] RFx is RF1, RF2, RF3, and RF4. INx is IN1, IN2, IN3, and IN4.
[3] Typically, the on resistance over time drifts by −0.05 Ω per decade.
[4] Maximum R_{ON} over time is R_{ON} (max) + $\Delta R_{ON\ TIME}$ (max) = 2.65 Ω.
[5] Maximum R_{ON} after 1 billion actuations is R_{ON} (max) + ΔR_{ON} (max) = 7.9 Ω.
[6] Actuating the switch at 85°C and measuring R_{ON} at 25°C is the most severe condition for ADGM1304 R_{ON} drift over actuations.
[7] Failure occurs when 50% of a sample lot fails. For more details, see the Cumulative On Switch Lifetime section.
[8] Switch is settled after 75 µs. Do not apply RF power between 0 µs to 75 µs.
[9] Disable the internal oscillator to eliminate feedthrough. When the internal oscillator and charge pump circuitry are disabled, the V_{CP} pin (Pin 24) must be driven with 80 V dc (VCP_{EXT}) from an external voltage supply, as outlined in Table 5, required for MEMS switch actuation.
[10] The spectrum analyzer setup is as follows: RBW = 200 Hz, video bandwidth (VBW) = 2 Hz, span = 100 kHz, input attenuator = 0 dB, the detector type is peak, and the maximum hold is off. The fundamental feedthrough noise or harmonic thereof (whichever is higher) is tested.
[11] For more details, see the Low Power Mode section.
[12] For more details, see the Internal Oscillator Feedthrough Mitigation section.

TIMING CHARACTERISTICS

V_{DD} = 3.0 V to 3.6 V, AGND = 0 V, RFGND = 0 V, all specifications T_{MIN} to T_{MAX} = 0°C to 85°C, unless otherwise noted.

Table 2.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Conditions/Comments
t_1	100	ns min	Serial clock (SCLK) period
t_2	45	ns min	SCLK high pulse width
t_3	45	ns min	SCLK low pulse width
t_4	25	ns min	Chip select ($\overline{CS}$) falling edge to SCLK active edge
t_5	20	ns min	Data setup time
t_6	20	ns min	Data hold time
t_7	25	ns min	SCLK active edge to $\overline{CS}$ rising edge
t_8	20	ns max	$\overline{CS}$ falling edge to SDO data available
t_9[1]	40	ns max	SCLK falling edge to SDO data available
t_{10}	25	ns max	$\overline{CS}$ rising edge to SDO returns to high impedance
t_{11}	100	ns min	$\overline{CS}$ high time between SPI commands
t_{12}	25	ns min	SCLK edge rejection to chip select ($\overline{CS}$) falling edge
t_{13}	25	ns min	$\overline{CS}$ rising edge to SCLK edge rejection

[1] Measured with a 20 pF load. t_9 determines the maximum SCLK frequency when SDO is used.

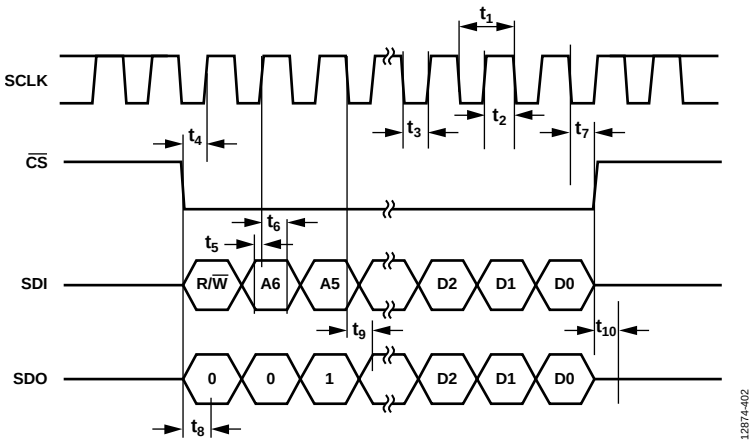

Figure 2. Addressable Mode Timing Diagram

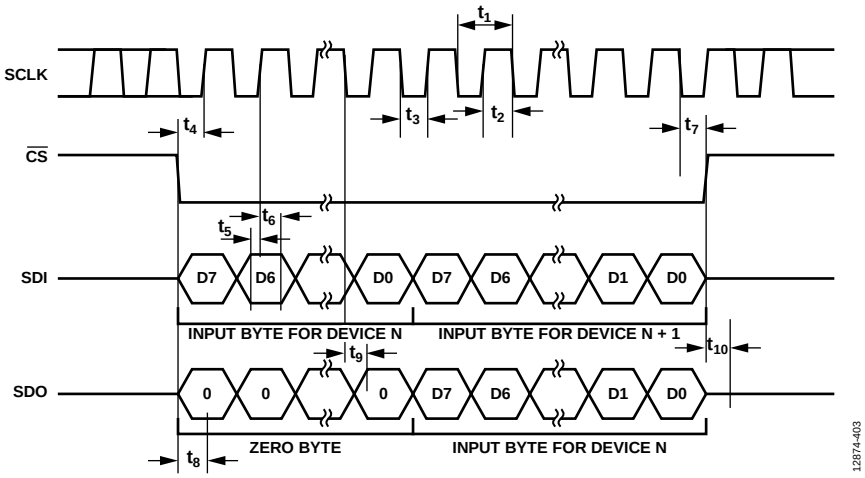

Figure 3. Daisy Chain Timing Diagram

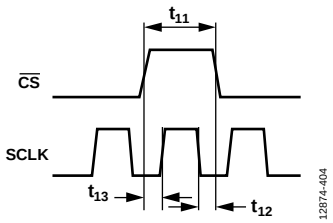

Figure 4. SCLK and $\overline{CS}$ Timing Relationship

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +6 V
Digital Inputs[1]	−0.3 V to V_{DD} + 0.3 V or 30 mA (whichever occurs first)
DC Voltage Rating[2]	±7 V
VCP_{EXT}	82 V
Current Rating[2]	250 mA
RF Power Rating	37 dBm
Standoff Voltage[3]	
RFx to AGND	±10 V
RFC to AGND	±10 V
RFx to RFC	20 V
Operating Temperature Range	0°C to +85°C
Storage Temperature Range	−65°C to +150°C
Reflow Soldering (Pb-Free)	
Peak Temperature	260(+0/−5)°C
Time at Peak Temperature	10 sec to 30 sec
Electrostatic Discharge (ESD)	
Human Body Model (HBM)[4]	
RF1, RF2, RF3, RF4 and RFC	100 V
All Other Pins	2.5 kV
Field-Induced Charged-Device Model (FICDM)[5]	
All Pins	500 V
Group D	
Mechanical Shock[6]	1500 *g* with 0.5 ms pulse
Vibration	20 Hz to 2000 Hz acceleration at 50 *g*
Constant Acceleration	30,000 *g*

[1] Clamp overvoltages at INx pin by internal diodes. Limit the current to the maximum ratings given.
[2] This rating is with respect to the switch in the on position with no RF signal applied.
[3] This rating is with respect to the switch in the off position.
[4] Take proper precautions during handling, as detailed in the Handling Precautions section.
[5] A safe automated handling and assembly process is achieved at this rating level by implementing industry-standard ESD controls.
[6] If the device is dropped during handling, do not use the device.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the junction to ambient thermal resistance.

θ_{JC} is the junction to case thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-24-9[1]	49.1	11.5	°C/W

[1] See JEDEC standard JESD51-2 for additional information on optimizing the thermal impedance (PCB with 3 × 3 vias).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

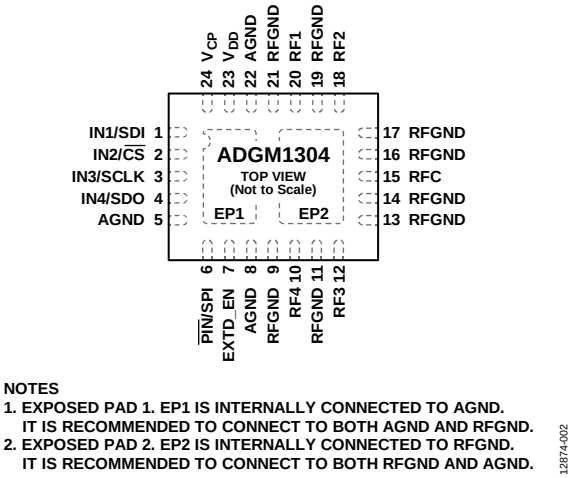

Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	IN1/SDI	Parallel Logic Digital Control Input 1. The voltage applied to this pin controls the gate of the RF1 to RFC MEMS switch. In parallel mode, if the IN1 pin is low, the RF1 to RFC switch is open (off). If the IN1 pin is high, the RF1 to RFC switch is closed (on). In SPI mode, this pin is the serial data input (SDI) pin.
2	IN2/$\overline{CS}$	Parallel Logic Digital Control Input 2. The voltage applied to this pin controls the gate of the RF2 to RFC MEMS switch. In parallel mode, if IN2 is low, the RF2 to RFC switch is open (off). If IN2 is high, the RF2 to RFC switch is closed (on). In SPI mode, this pin is the chip select ($\overline{CS}$) pin. $\overline{CS}$ is an active low signal that selects the slave device with which the master device intends to communicate. Typically, there is a dedicated $\overline{CS}$ between the master device and each slave device. The $\overline{CS}$ pin also functions to synchronize and frame the communications to and from the slave device.
3	IN3/SCLK	Parallel Logic Digital Control Input 3. The voltage applied to this pin controls the gate of the RF3 to RFC MEMS switch. In parallel mode, if IN3 is low, the RF3 to RFC switch is open (off). If IN3 is high, the RF3 to RFC switch is closed (on). In SPI mode, this pin is the serial clock (SCLK) pin that synchronizes the slave device(s) to the master device. Typically, the SCLK signal is shared for all slave devices on the serial bus. The SCLK signal is always driven by the master device.
4	IN4/SDO	Parallel Logic Digital Control Input 4. The voltage applied to this pin controls the gate of the RF4 to RFC MEMS switch. In parallel mode, if IN4 is low, the RF4 to RFC switch is open (off). If IN4 is high, the RF4 to RFC switch is closed (on). In SPI mode, this pin is the serial data output (SDO) pin. Typically, the SDO pin is shared for all slave devices on the serial bus. The SDO pin is driven by only one slave device at a time, otherwise it is high impedance. The SDO pin is always high impedance when $\overline{CS}$ is deasserted high.
5, 8, 22	AGND	Analog Ground Connection.
6	$\overline{PIN}$/SPI	Parallel Mode Enable/SPI Mode Enable. The SPI interface is enabled when this pin is high, and the parallel interface (IN1, IN2, IN3, IN4) is enabled when this pin is low.
7	EXTD_EN	External Voltage Drive Enable. In normal operation, set EXTD_EN low to enable the built in 10 MHz oscillator, which enables the internal driver IC voltage boost circuitry. Setting EXTD_EN high disables the internal 10 MHz oscillator and driver boost circuitry. With the oscillator disabled, the switch can still be controlled via the logic interface pins (IN1 to IN4) or via the SPI interface, but the V_{CP} pin must be driven with 80 V dc from an external voltage supply. In this mode, the ADGM1304 only consumes 50 µA maximum supply current. Disabling the internal oscillator eliminates the associated 10 MHz noise feedthrough from the switch.
9, 11, 13, 14, 16, 17, 19, 21	RFGND	RF Ground Connection.
10	RF4	RF4 Port. This pin can be an input or an output. If unused, the pin must be connected to RFGND or terminate the pin with a 50 Ω resistor to RFGND.
12	RF3	RF3 Port. This pin can be an input or an output. If unused, the pin must be connected to RFGND or terminate the pin with a 50 Ω resistor to RFGND.
15	RFC	Common RF Port. This pin can be an input or an output.
18	RF2	RF2 Port. This pin can be an input or an output. If unused, the pin must be connected to RFGND or terminate the pin with a 50 Ω resistor to RFGND.

Pin No.	Mnemonic	Description
20	RF1	RF1 Port. This pin can be an input or an output. If unused, the pin must be connected to RFGND or terminate the pin with a 50 Ω resistor to RFGND.
23	V_{DD}	Positive Power Supply Input. The recommended decoupling capacitor to ground value is 0.1 µF. For the recommended input voltage for this chip, see the Specifications section.
24	V_{CP}	Charge Pump Capacitor Terminal. The recommended shunt capacitor to ground value is 47 pF (100 V rated). If EXTD_EN is high, an 80 V dc drive voltage must be input into V_{CP} to drive the switches.
	EP1	Exposed Pad 1. EP1 is internally connected to AGND. It is recommended to connect to both AGND and RFGND.
	EP2	Exposed Pad 2. EP2 is internally connected to RFGND. It is recommended to connect to both RFGND and AGND.

TYPICAL PERFORMANCE CHARACTERISTICS

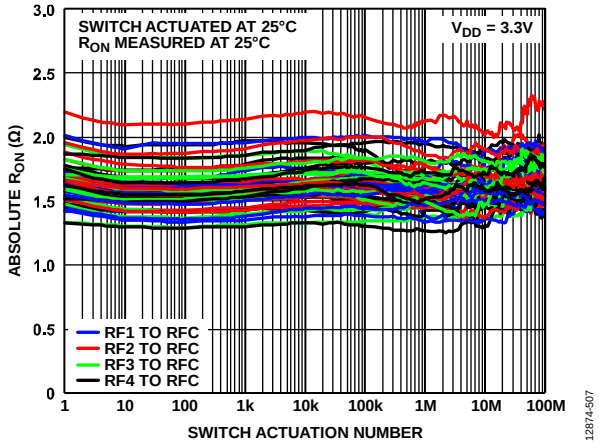

Figure 6. Absolute R_{ON} vs. Switch Actuation Number, Switch Actuated at 25°C and R_{ON} Measured at 25°C

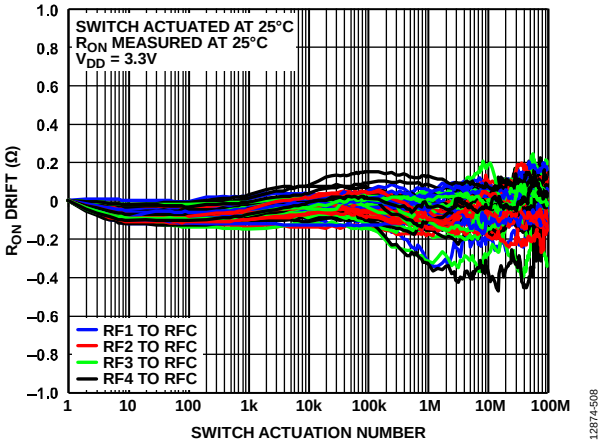

Figure 7. R_{ON} Drift vs. Switch Actuation Number, Normalized at Zero, Switch Actuated at 25°C and R_{ON} Measured at 25°C

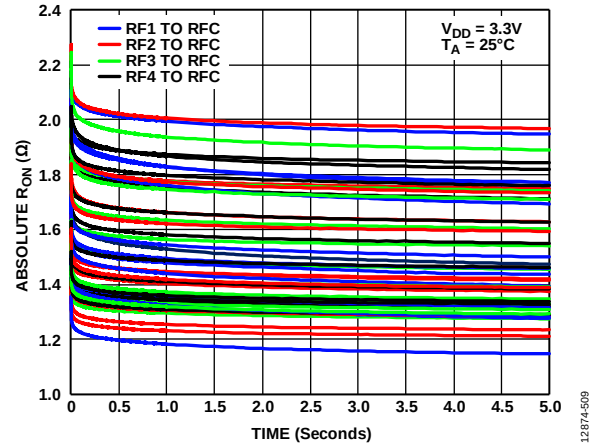

Figure 8. Absolute R_{ON} vs. Time (1 ms to 5 sec) on Linear Scale

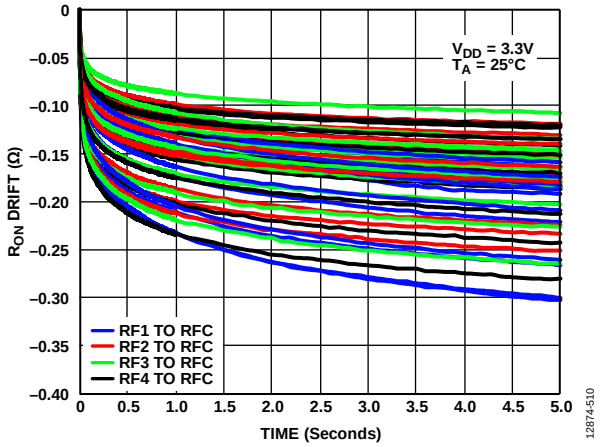

Figure 9. R_{ON} Drift vs. Time (1 ms to 5 sec) on Linear Scale, Normalized at Zero

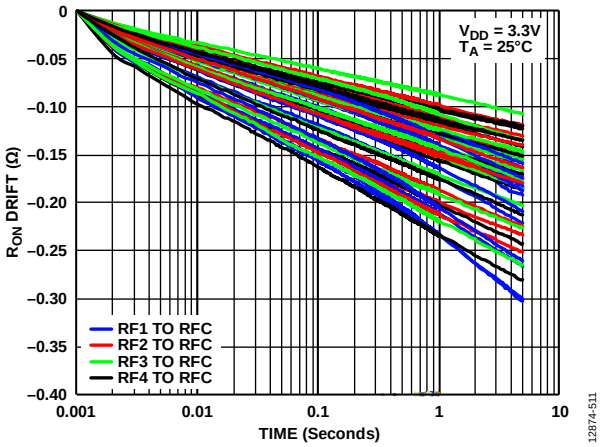

Figure 10. R_{ON} Drift vs. Time (1 ms to 5 sec) on Log Scale, Normalized at Zero

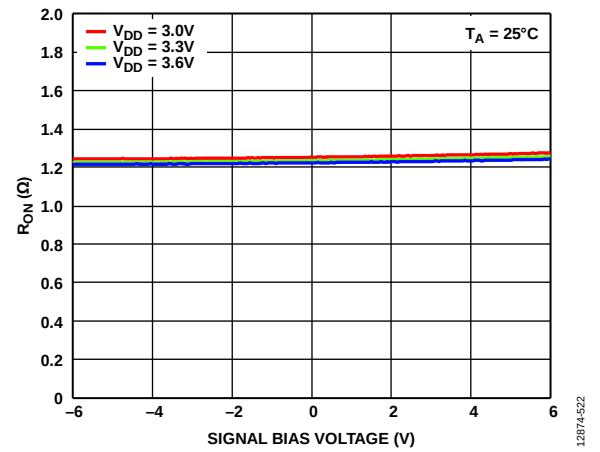

Figure 11. R_{ON} vs. Signal Bias Voltage over Supply Voltages (Measured 5 sec Post Switch Turn On Time, RF1 to RFC On)

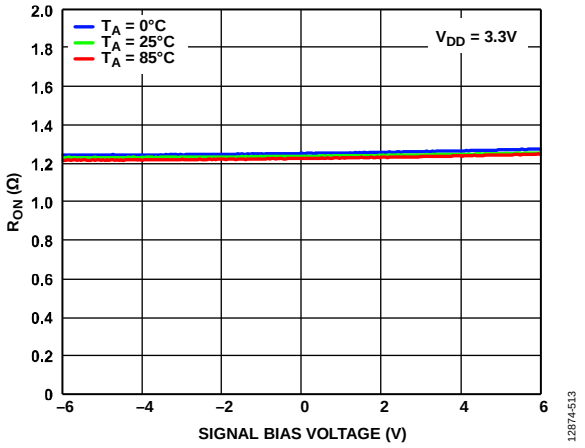

Figure 12. R_{ON} vs. Signal Bias Voltage over Temperature (Measured 5 sec Post Switch Turn On Time, RF1 to RFC On)

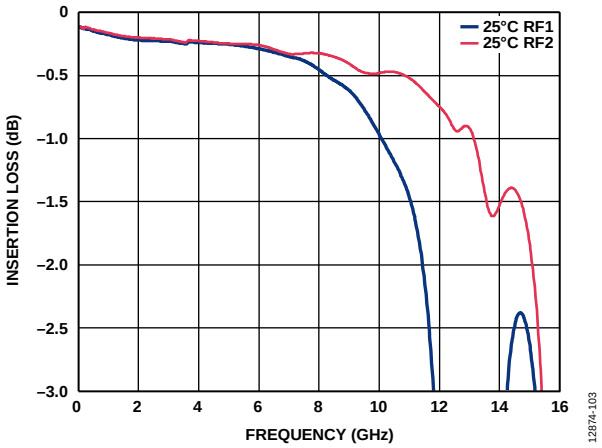

Figure 15. Insertion Loss vs. Frequency on Linear Scale (V_{DD} = 3.3 V)

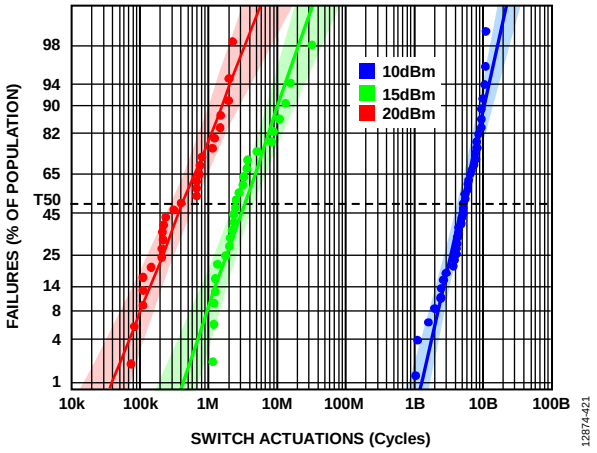

Figure 13. Hot Switching Probability Distribution on Log Normal with 95% Confidence Interval (CI), RF Power = Continuous Wave, Terminated into 50 Ω, T_A = 25°C, V_{DD} = 3.3 V

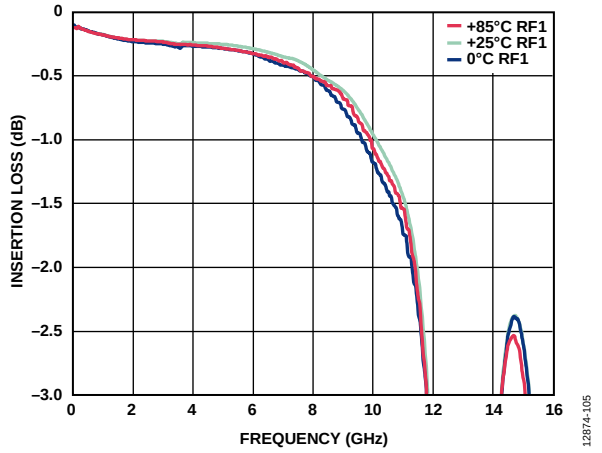

Figure 16. Insertion Loss vs. Frequency over Temperature on Linear Scale (V_{DD} = 3.3 V, RF1 to RFC)

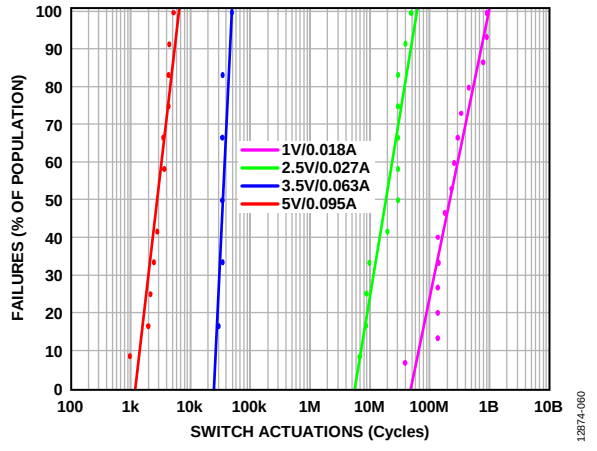

Figure 14. DC Hot Switching Probability Distribution, Terminated into 50 Ω, RFx Load Capacitance = 10 µF, T_A = 25°C, V_{DD} = 3.3 V

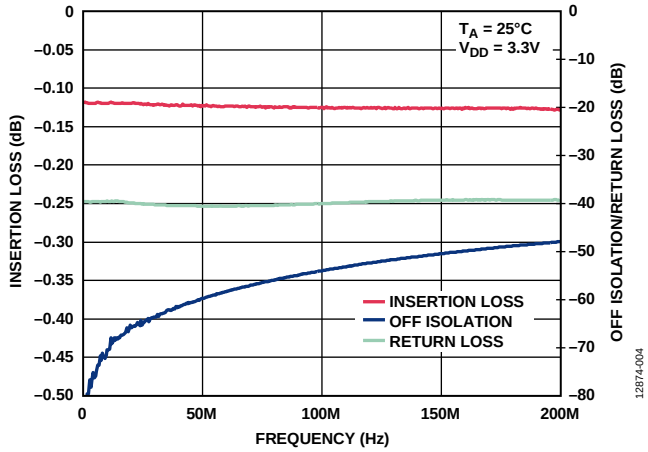

Figure 17. Insertion Loss and Off Isolation/Return Loss vs. Frequency (V_{DD} = 3.3 V, RF1 to RFC)

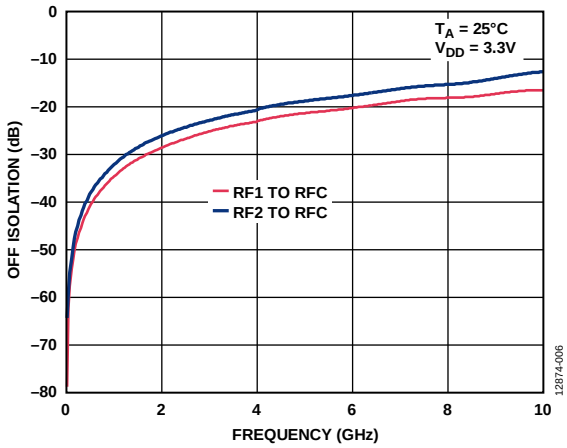

Figure 18. Off Isolation vs. Frequency, All Switches Off (V_{DD} = 3.3 V)

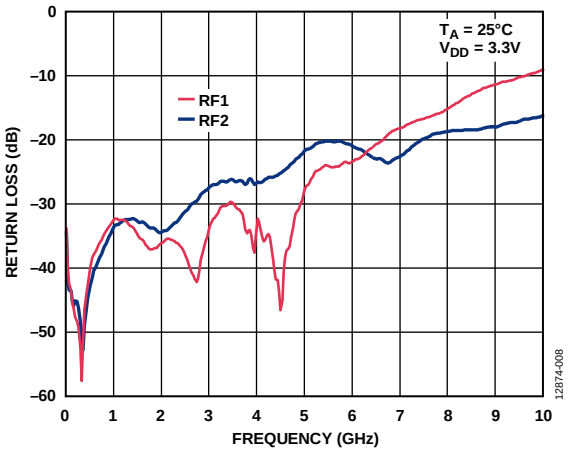

Figure 21. Return Loss vs. Frequency (V_{DD} = 3.3 V)

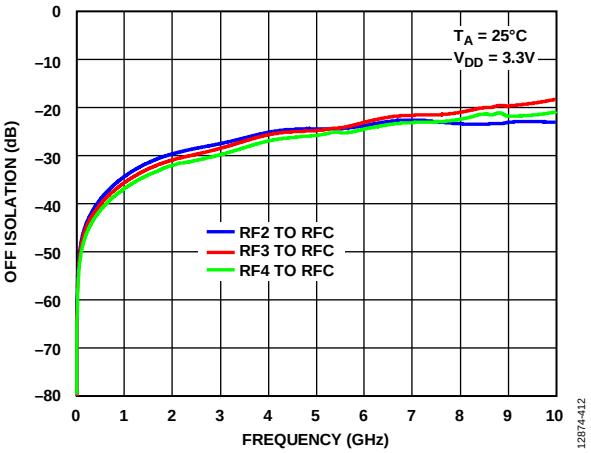

Figure 19. Off Isolation vs. Frequency, RF1 to RFC On (V_{DD} = 3.3 V)

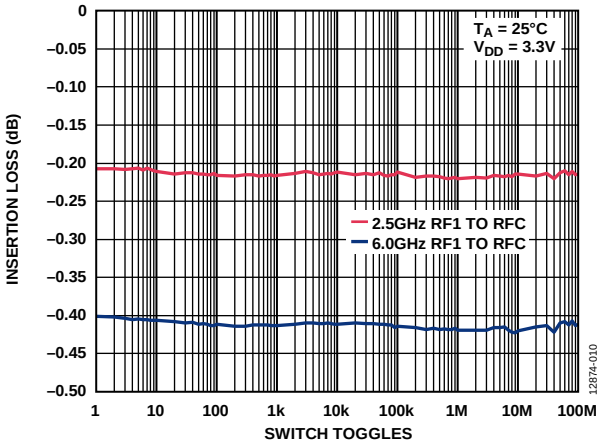

Figure 22. Insertion Loss vs. Switch Toggles (V_{DD} = 3.3 V)

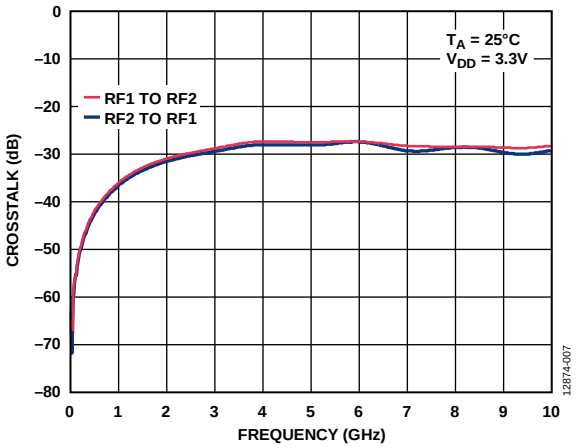

Figure 20. Crosstalk vs. Frequency (V_{DD} = 3.3 V)

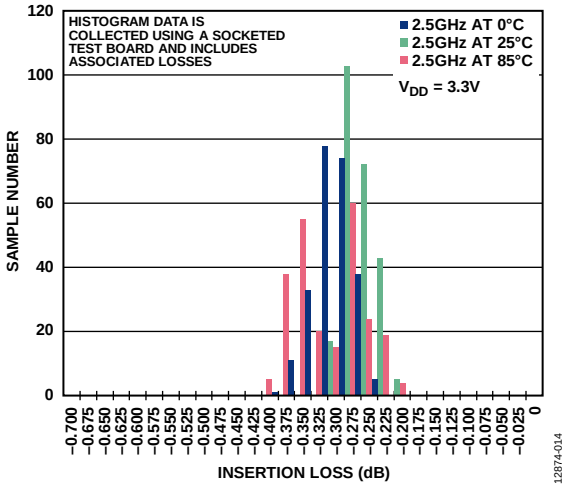

Figure 23. 2.5 GHz Insertion Loss Histogram at Various Temperatures, V_{DD} = 3.3 V

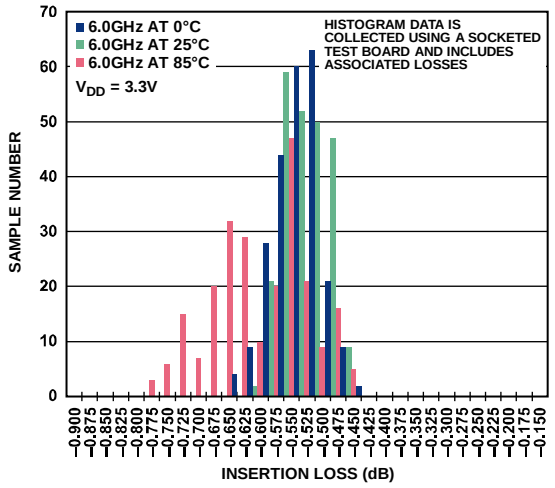

Figure 24. 6.0 GHz Insertion Loss Histogram at Various Temperatures, (V_{DD} = 3.3 V

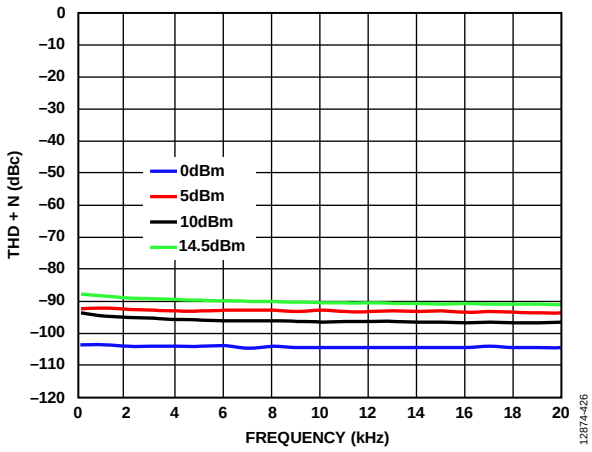

Figure 27. THD + N vs. Frequency, V_{DD} = 3.3 V, R_{LOAD} = 300 Ω, T_A = 25°C, Signal Source Impedance = 20 Ω

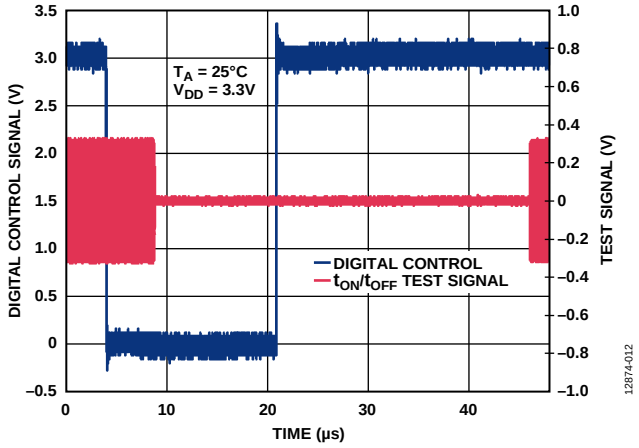

Figure 25. Digital Control Signal and Test Signal vs. Time (V_{DD} = 3.3 V)

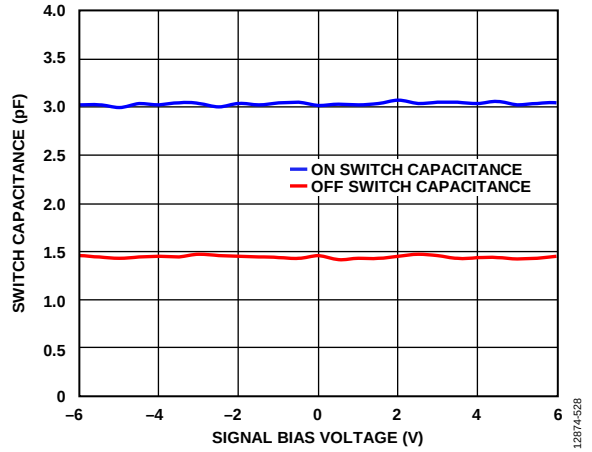

Figure 28. Switch Capacitance vs. Signal Bias Voltage

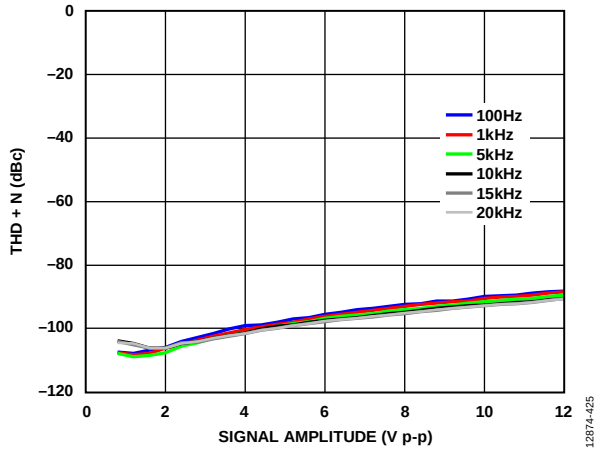

Figure 26. THD + N vs. Signal Amplitude, V_{DD} = 3.3 V, R_{LOAD} = 300 Ω, T_A = 25°C, Signal Source Impedance = 20 Ω

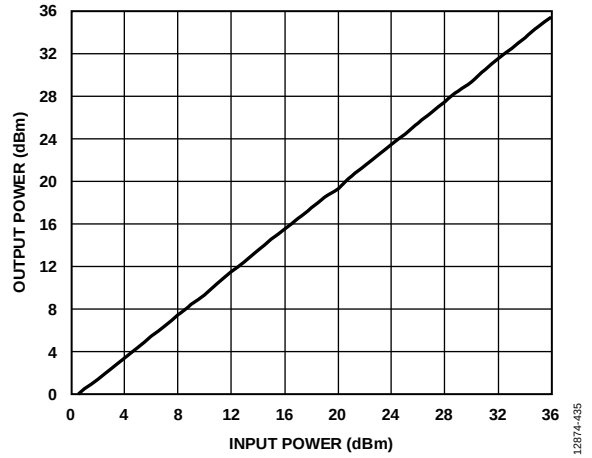

Figure 29. Output Power vs. Input Power (Signal Frequency = 4 GHz, V_{DD} = 3.3 V, T_A = 25°C)

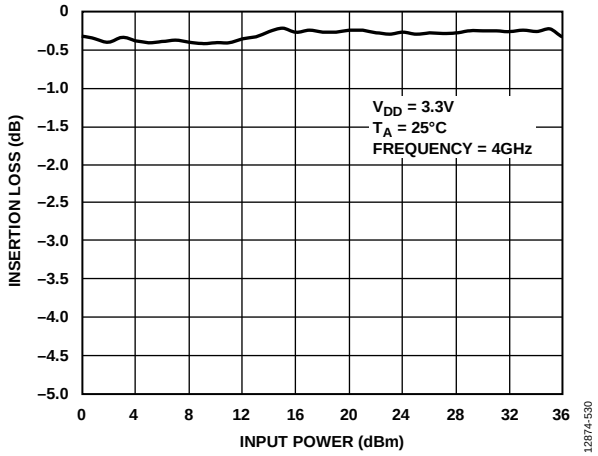

Figure 30. Insertion Loss vs. Input Power

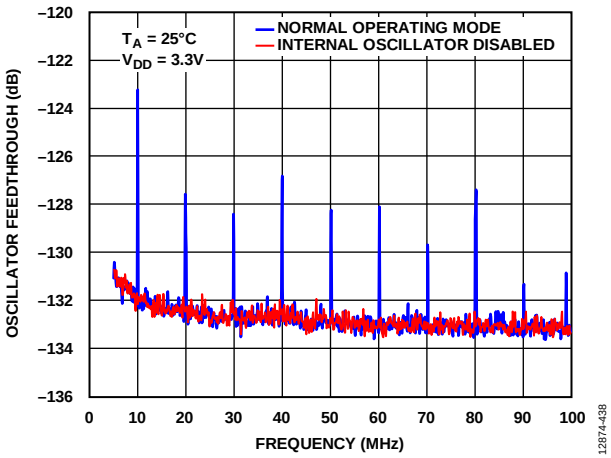

Figure 32. Oscillator Feedthrough Wide Bandwidth

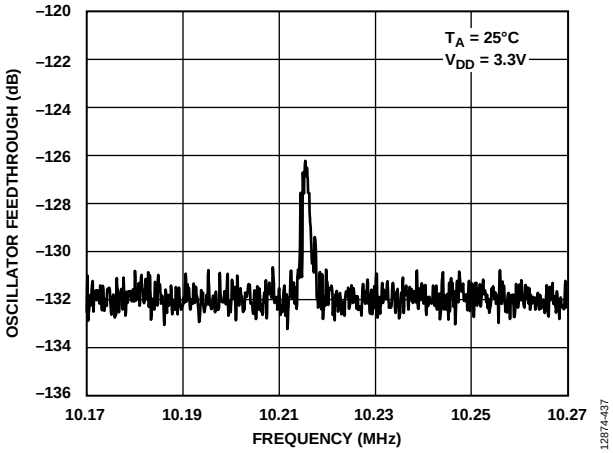

Figure 31. Oscillator Feedthrough, Zoomed In at 10.2 MHz

EYE DIAGRAMS

Pattern used for eye diagram measurements = pseudorandom binary sequence (PRBS) $2^{23} - 1$.

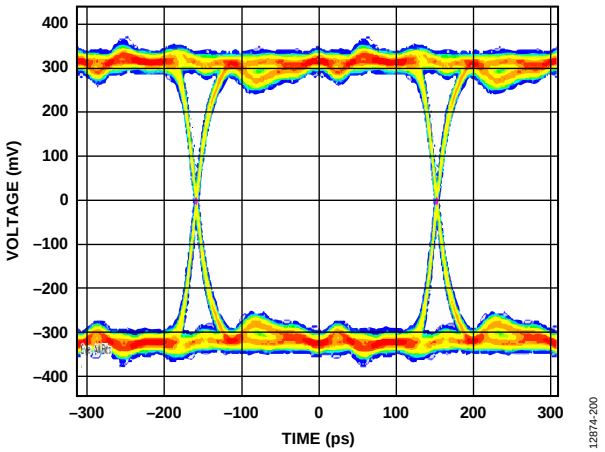

Figure 33. RF1 to RFC with Reference Trace at 3.2 Gbps

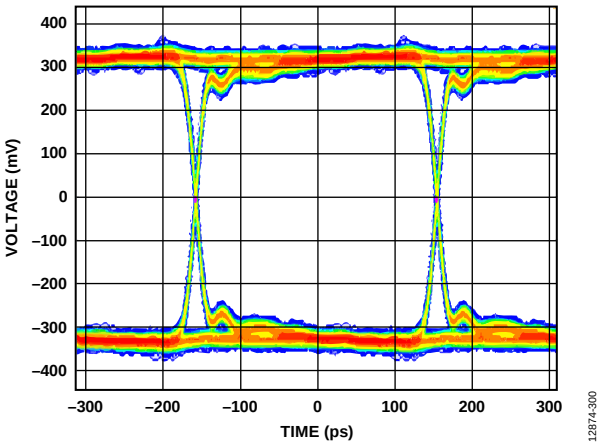

Figure 35. Eye Diagram Reference Trace at 3.2 Gbps

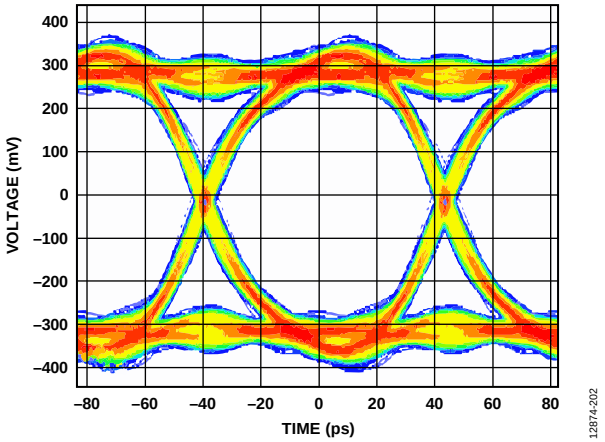

Figure 34. RF1 to RFC with Reference Trace at 12.5 Gbps

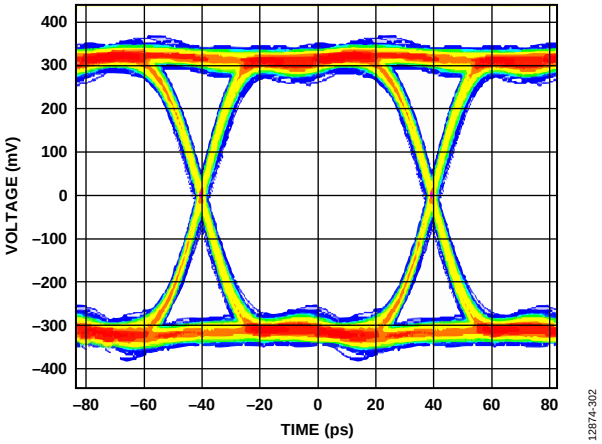

Figure 36. Eye Diagram Reference Trace at 12.5 Gbps

TEST CIRCUITS

Test circuits applicable to all channels; additional pins omitted for clarity.

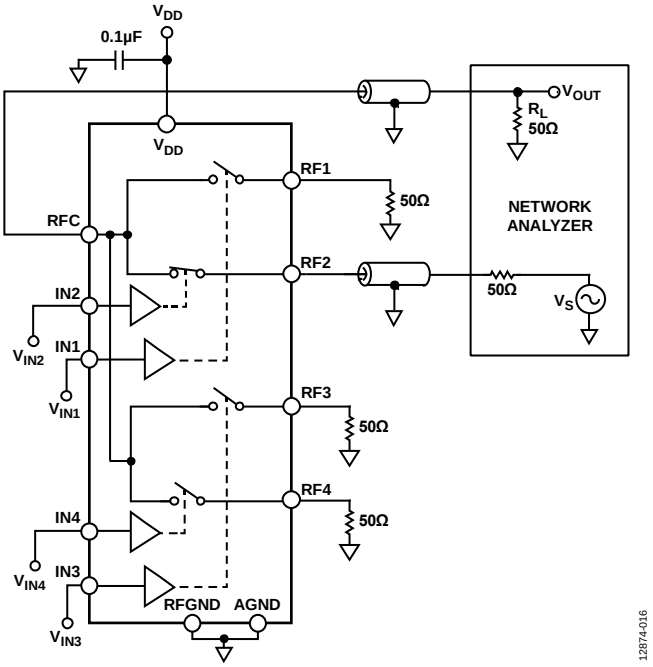

Figure 37. Insertion Loss/Return Loss

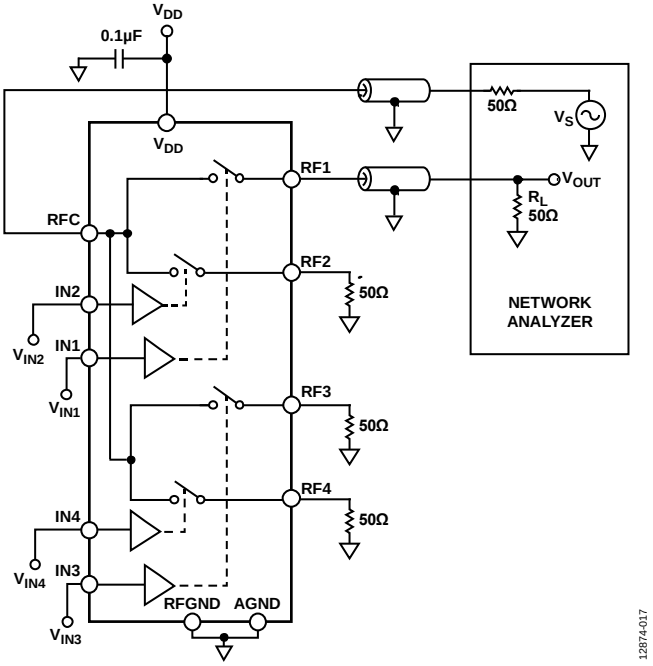

Figure 38. Isolation

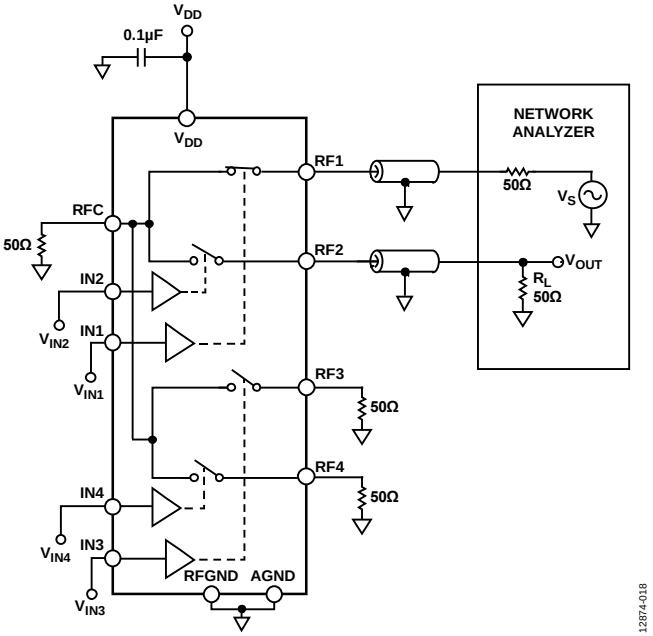

Figure 39. Crosstalk

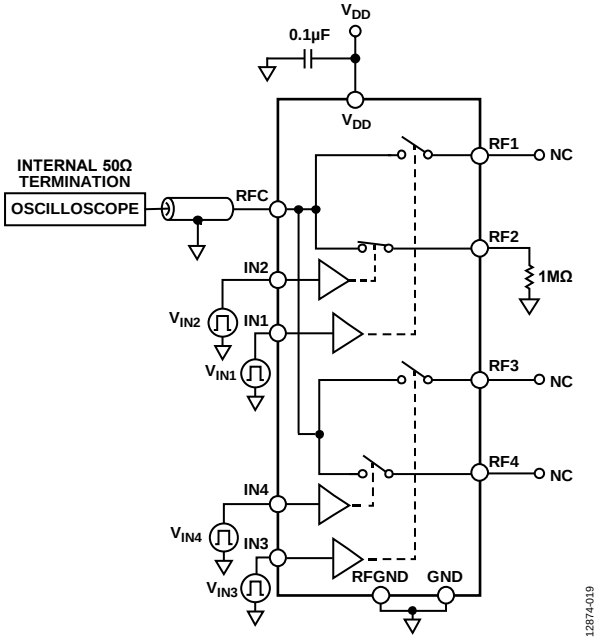

Figure 40. Video Feedthrough

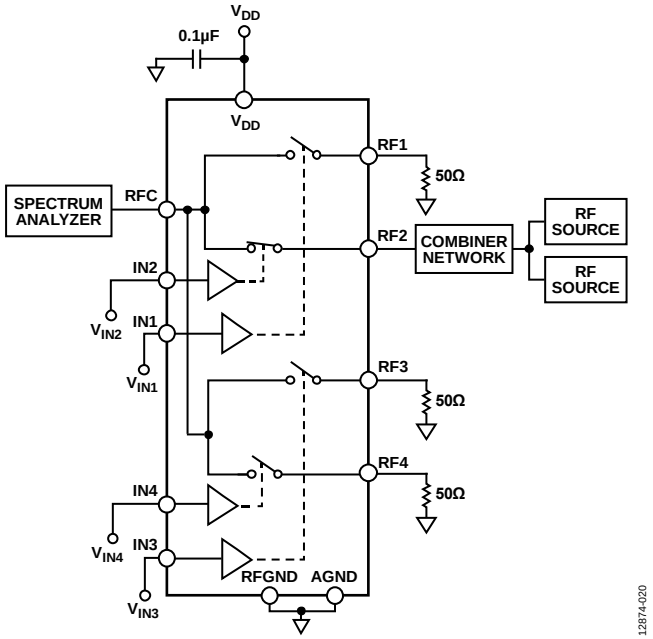

Figure 41. Input Second-Order Intermodulation Intercept (IIP2) and Input Third-Order Intermodulation Intercept (IIP3)

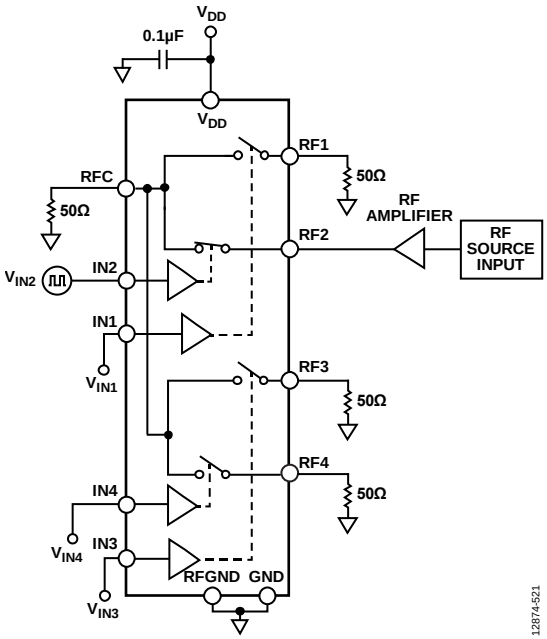

Figure 43. Hot Switching Evaluation Setup, 2 GHz RF Source, 50% Duty Cycle, 5 kHz Switching Frequency

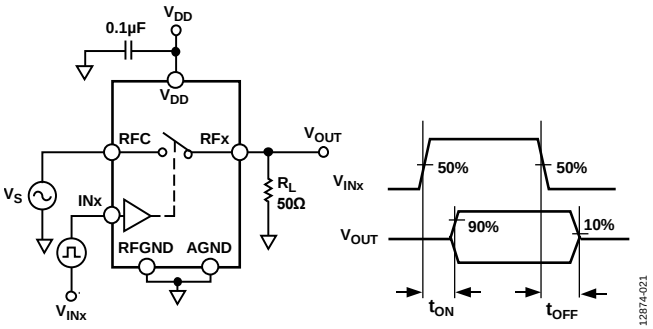

Figure 42. Switch Timings, t_{ON} and t_{OFF}

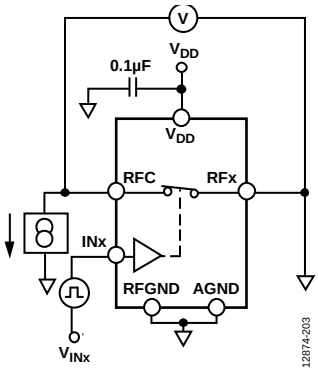

Figure 44. On Resistance

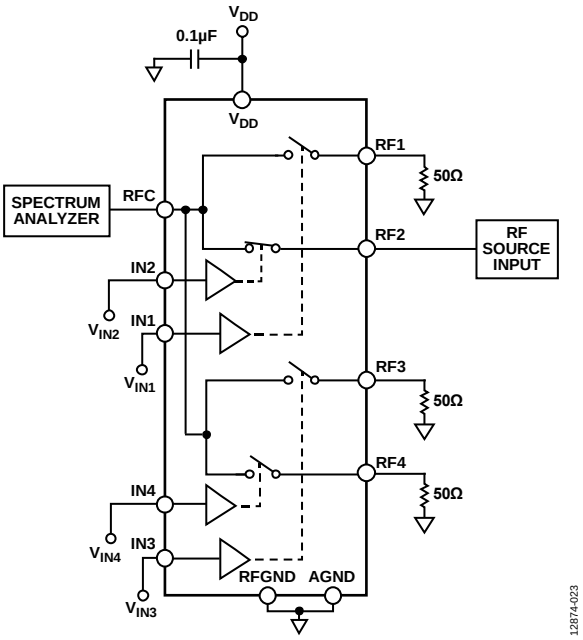

Figure 45. Second and Third Harmonics, RF Power

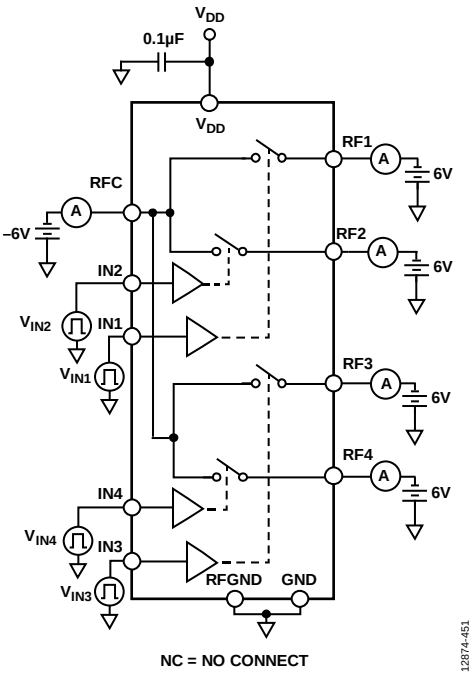

Figure 47. Off Leakage

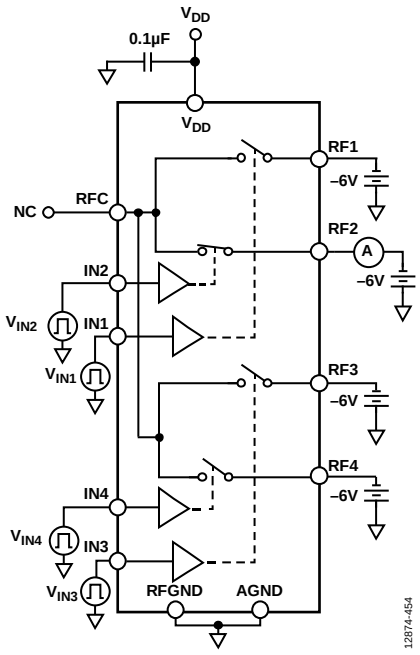

Figure 46. On Leakage

TERMINOLOGY

Insertion Loss (IL)
IL is the amount of signal attenuation between the input and output ports of the switch when the switch is in the on state. IL is expressed in decibels. Ensure that insertion loss is as small as possible for maximum power transfer.

An example calculation of insertion loss based on the setup in Figure 37 is as follows:

$$IL = -20\log_{10}|S_{RF2RFC}|$$

where S_{RF2RFC} is the transmission coefficient measured from RF2 to RFC with RF2 in the on position.

All unused switches are in the off position and terminated in a purely resistive load of 50 Ω.

Isolation (I_{SO})
I_{SO} is the amount of signal attenuation between the input and output ports of the switch when the switch is in the off state. I_{SO} is expressed in decibels. Ensure that isolation is as large as possible.

An example calculation of isolation based on the setup in Figure 38 is as follows:

$$I_{SO} = -20\log_{10}|S_{RFCRF1}|$$

where S_{RFCRF1} is the transmission coefficient measured from RFC to RF1 with RF1 in the off position.

All unused switches are in the off position and terminated in a purely resistive load of 50 Ω.

Crosstalk (C_{TK})
C_{TK} is a measure of unwanted signals coupled through from one channel to another because of parasitic capacitance. C_{TK} is expressed in decibels.

An example calculation of crosstalk based on the setup in Figure 39 is as follows:

$$C_{TK} = -20\log_{10}|S_{RF1RF2}|$$

where S_{RF1RF2} is the transmission coefficient measured from RF1 to RF2 with RF1 in the off position and RF2 in the on position.

All unused switches are in the off position and terminated in a purely resistive load of 50 Ω.

Return Loss (RL)
RL is the magnitude of the reflection coefficient (expressed in decibels), and the amount of reflected signal relative to the incident signal.

An example calculation of return loss based on the setup in Figure 37 is as follows:

$$RL = -20\log_{10}|S_{11}|$$

where S_{11} is the reflection coefficient of the port under test.

Third-Order Intermodulation Intercept (IIP3)
IP3 is the intersection point of the fundamental output power (P_{OUT}) vs. input power (P_{IN}) extrapolated line and the third-order intermodulation products extrapolated line of a two-tone test. IIP3 is a figure of merit that characterizes the switch linearity.

Second-Order Intermodulation Intercept (IIP2)
IIP2 is the intersection point of the fundamental P_{OUT} vs. P_{IN} extrapolated line and the second-order intermodulation products extrapolated line of a two-tone test. IIP2 is a figure of merit that characterizes the switch linearity.

Second Harmonic (HD2)
HD2 is the amplitude of the second harmonic, where, for a signal whose fundamental frequency is f, the second harmonic has a frequency 2f. This measurement is a single tone test, expressed with reference to the carrier signal (dBc).

Third Harmonic (HD3)
HD3 is the amplitude of the third harmonic, where, for a signal whose fundamental frequency is f, the third harmonic has a frequency 3f. This measurement is a single tone test, expressed with reference to the carrier signal (dBc).

RF Power Rating
The RF power rating is the maximum level of RF power that passes through the switch without degradation to the switch lifetime when it is in the on state.

On Switching Time (t_{ON})
t_{ON} is the time it takes for the switch to turn on. It is measured from 50% of the control signal (INx) to 90% of the on level. No power is applied through the switch during this test (cold switched). The switch is terminated into a 50 Ω load.

Off Switching Time (t_{OFF})
t_{OFF} is the time it takes for the switch to turn off. It is measured from 50% of the control signal (INx) to 10% of the on level. No power is applied through the switch during this test (cold switched). The switch is terminated into a 50 Ω load.

Actuation Frequency
The actuation frequency refers to the speed at which the ADGM1304 can be switched on and off. It is dependent on both settling times and on to off switching times.

Wake-Up Time
The wake-up time is a measure of the time required for the voltage on V_{CP} to reach the typical voltage of 80 V after the device exits sleep mode.

Video Feedthrough
Video feedthrough is a measure of the spurious signals present at the RF ports of the switch when the control voltage is switched from high to low or from low to high without an RF signal present.

Internal Oscillator Frequency
The internal oscillator frequency is the value of the on-board oscillator that drives the gate control chip of the ADGM1304.

Internal Oscillator Feedthrough
The internal oscillator feedthrough is the amount of internal oscillator signal that feeds through to the RF pins of the switch. This signal appears as a noise spur on the RFx pin and RFC pin of the switch at the oscillator operating frequency and oscillator harmonics.

On Resistance (R_{ON})
R_{ON} is the resistance of a switch in the closed (on) state measured between the package pins. Measure on resistance in 4-wire mode to eliminate any cabling or PCB series resistances.

On Resistance Drift
On resistance drift is the change in the on resistance of the switch over the specified criteria in Table 1.

Continuously on Lifetime
The continuously on lifetime measures how long the switch is left in a continuously on state. If the switch is left in the on position for an extended period, it affects the turn off mechanism of the device.

Actuation Lifetime
Actuation lifetime is the number of consecutive open to close to open cycles that can complete without the on resistance exceeding a specified limit and no occurrence of failures to open (FTO) or failures to close (FTC).

Cold Switching
Cold switching operates the switch in a mode so that no voltage differential exists between source and drain when the switch is closed or no current is flowing from source to drain when the switch opens. All switches have longer lives when cold switched.

Hot Switching
Hot switching is operating the switch in a mode where a voltage differential exists between source and drain when the switch is closed and/or current is flowing from RFx channel to RFC channel when the switch is opened. Hot switching results in a reduced switch life, depending on the magnitude of the open circuit voltage between the source and the drain.

Input High Voltage (V_{INH})
V_{INH} is the minimum input voltage for Logic 1.

Input Low Voltage (V_{INL})
V_{INL} is the maximum input voltage for Logic 0.

Input Current (I_{INL}, I_{INH})
I_{INL} and I_{INH} are the low and high input currents of the digital inputs.

Output High Voltage (V_{OH})
V_{OH} is the minimum output voltage for Logic 1.

Output Low Voltage (V_{OL})
V_{OL} is the maximum output voltage for Logic 0.

Low Power Mode Current ($I_{DD\ EXT\ VCP}$)
$I_{DD\ EXT\ VCP}$ is the amount of supply current used by the gate driver circuity when the internal oscillator and the charge pump circuitry are turned off by setting the EXTD_EN pin high.

External Drive Current ($I_{CP\ EXT\ VCP}$)
$I_{CP\ EXT\ VCP}$ is the amount of current used by the ADGM1304 from the external 80 V power supply when the internal oscillator and charge pump circuitry are turned off by setting the EXTD_EN pin high.

THEORY OF OPERATION

The ADGM1304 is an SP4T switch fabricated using Analog Devices MEMS switch technology. This technology enables high power, low loss, low distortion GHz switches for use in demanding RF applications.

Figure 48 shows a stylized cross section graphic of the switch with dimensions. The switch is an electrostatically actuated cantilever beam connected in a 3-terminal configuration. Functionally, the switch is analogous to a field effect transistor (FET), and the terminals can be used as a source, gate, and drain.

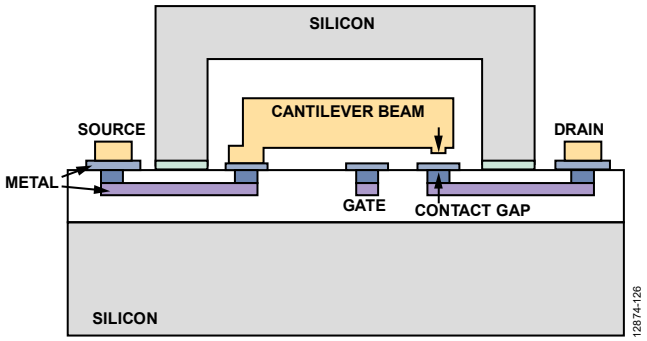

Figure 48. Cross Section of the MEMS Switch Design Showing the Cantilever Switch Beam (Not to Scale)

When a dc actuation voltage is applied between the gate electrode and the source (the switch beam), an electrostatic force is generated, which attracts the beam toward the substrate. A separate on-board charge pump IC generates the bias voltage, and 80 V is used for actuation.

When the bias voltage between the gate and the source exceeds the threshold voltage of the switch, V_{TH}, the contacts on the beam touch the drain, which completes the circuit between the source and the drain and turns the switch on. When the bias voltage is removed (0 V on the gate electrode), the beam acts as a spring to generate a sufficient restoring force to open the connection between the source and the drain, break the circuit, and turn the switch off.

Figure 49 shows the SP4T MEMS switch and controller die within the LFCSP. Some of the LFCSP plastic molding material is removed to allow the MEMS switch die (right) and controller die (left) with associated wire bonds to be visible. The silicon hermetically sealed cap covering the switch die is the black rectangle on the right. Hermetically sealing the switches improves the reliability and lifetime of the switches by keeping them in a controlled atmosphere. The switch contacts do not suffer from dry switching or low power switching lifetime degradation.

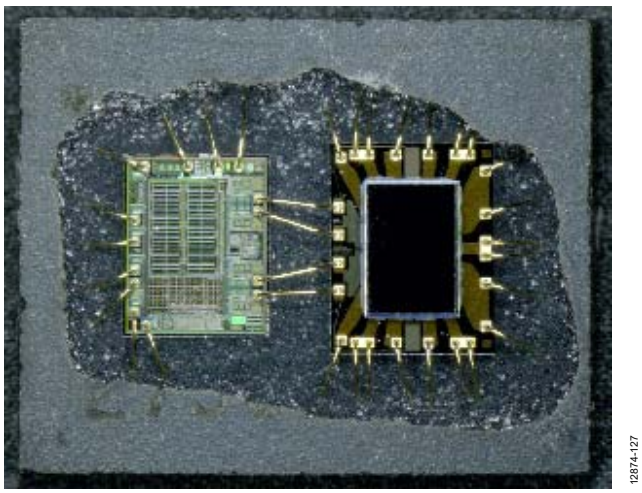

Figure 49. ADGM1304 LFCSP Package with Molding Compound Partially Removed to Show MEMS Switch Die (Right), Controller Die (Left), and Associated Wire Bonds

PARALLEL DIGITAL INTERFACE

The ADGM1304 is controlled via a parallel interface. Standard CMOS/LVTTL signals applied through this interface control the actuation and release of all the switch channels of the ADGM1304. Applied gate signals are boosted to give the required voltages needed to actuate the MEMS switches.

Setting the $\overline{\text{PIN}}$/SPI pin low enables the parallel digital interface in 4-wire SP4T mode. In parallel mode, Pin 1 to Pin 4 (IN1 to IN4) control the switching functions of the ADGM1304. When a Logic 1 is applied to one of these pins, the gate of the corresponding switch is activated and the switch turns on. Conversely, when a Logic 0 is applied to one of these pins, the switch turns off. Note that it is possible to connect more than one RFx input to RFC at a time. Table 6 is the truth table for the ADGM1304.

Table 6. Truth Table When in Parallel Digital Interface Mode

IN1	IN2	IN3	IN4	RF1 to RFC	RF2 to RFC	RF3 to RFC	RF4 to RFC
0	0	0	0	Off	Off	Off	Off
0	0	0	1	Off	Off	Off	On
0	0	1	0	Off	Off	On	Off
0	0	1	1	Off	Off	On	On
0	1	0	0	Off	On	Off	Off
0	1	0	1	Off	On	Off	On
0	1	1	0	Off	On	On	Off
0	1	1	1	Off	On	On	On
1	0	0	0	On	Off	Off	Off
1	0	0	1	On	Off	Off	On
1	0	1	0	On	Off	On	Off
1	0	1	1	On	Off	On	On
1	1	0	0	On	On	Off	Off
1	1	0	1	On	On	Off	On
1	1	1	0	On	On	On	Off
1	1	1	1	On	On	On	On

SPI DIGITAL INTERFACE

The ADGM1304 can be controlled via an SPI digital interface when Pin 6 ($\overline{\text{PIN}}$/SPI) is high. The SPI is compatible with SPI Mode 0 (clock polarity (CPOL) = 0, clock phase (CPHA) = 0) and Mode 3 (CPOL = 1, CPHA = 1) and it operates with SCLK frequencies up to 10 MHz. When the SPI is active, the default mode is addressable, in which, the device registers are accessed by a 16-bit SPI command that is bound by the state of the $\overline{\text{CS}}$ pin. The ADGM1304 can also operate in daisy-chain mode.

The SPI interface pins of the ADGM1304 are $\overline{\text{CS}}$, SCLK, SDI, and SDO. Hold $\overline{\text{CS}}$ low when using the SPI interface. The data on SDI is captured on the rising edge of SCLK and data is propagated out on SDO on the falling edge of SCLK. SDO has push-pull output driver architecture that does not require pull-up resistors.

Addressable Mode

Addressable mode is the default mode for the ADGM1304 on power up. A single SPI frame in addressable mode is bounded by a $\overline{\text{CS}}$ falling edge and the succeeding$\overline{\text{CS}}$ rising edge. It comprises 16 SCLK cycles. The timing diagram for addressable mode, in SPI Mode 0, is shown in Figure 51.

The first SDI bit indicates if the SPI command is a read or write command. The next seven bits determine the target register address. The remaining eight bits provide the data to the addressed register. The last eight bits are ignored during a read command, during which time the SDO propagates out the data contained in the addressed register.

In Mode 0, during any SPI command, SDO sends out eight alignment bits on the $\overline{\text{CS}}$ falling edge and the first seven SCLK falling edges (in Mode 3, the first SCLK falling edge is ignored as shown in Figure 51). The alignment bits observed at SDO are 0x25.

The target register address of an SPI command is determined on the eighth SCLK rising edge. Data from the target register propagates out on the SDO pin from the eighth to the 15th SCLK falling edge during SPI reads. A register write occurs on the 16th SCLK rising edge during SPI writes.

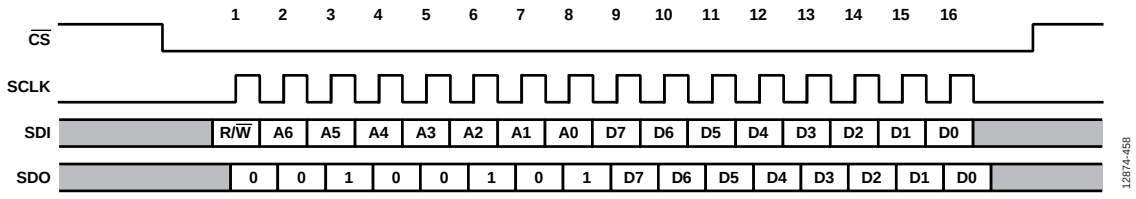

Figure 50. Addressable Mode Timing Diagram (Mode 0)

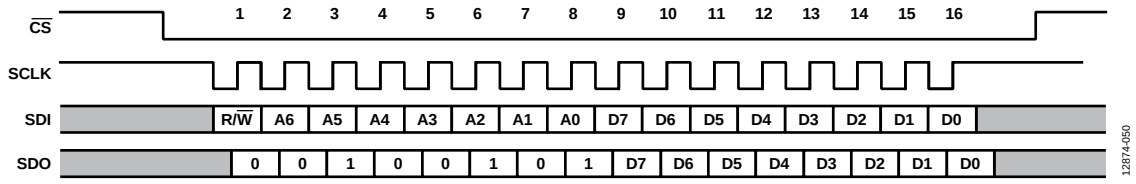

Figure 51. Addressable Mode Timing Diagram (Mode 3)

Daisy-Chain Mode

The connection of several ADGM1304 devices in a daisy-chain configuration is possible. All devices share the same $\overline{CS}$ and SCLK lines while the SDO pin of one device forms a connection to the SDI pin of the next device, creating a shift register. In daisy-chain mode, the SDO signal is an 8-cycle delayed version of the SDI signal (see Figure 53).

The ADGM1304 can only enter daisy-chain mode from addressable mode by sending the 16-bit SPI command, 0x2500. See Figure 53 for an example of this command. When the ADGM1304 receives this command, the SDO pin of the devices sends out the same command because the alignment bits at the SDO pin are 0x25. This command allows multiple daisy-chained devices to enter daisy-chain mode in a single SPI frame. A hardware reset is required to exit daisy-chain mode.

For the timing diagram of a typical daisy-chain SPI frame, see Figure 54. When the $\overline{CS}$ pin goes high, Device 1 writes Command 0 to Bits[7:0] to the SWITCH_DATA register, Device 2 writes Command 1 to Bits[7:0] to the switches, and so on. The SPI block uses the last eight bits received through the SDI pin to update the switches. After entering daisy-chain mode, the first eight bits sent out by the SDO pin are 0x00. When $\overline{CS}$ goes high, the internal shift register value does not reset back to 0.

An SCLK rising edge reads in data on the SDI pin while data is propagated out of the SDO pin on an SCLK falling edge. The expected number of SCLK cycles are a multiple of eight before the $\overline{CS}$ pin goes high. When this is not the case, the SPI interface sends the last eight bits received to the SWITCH_DATA register.

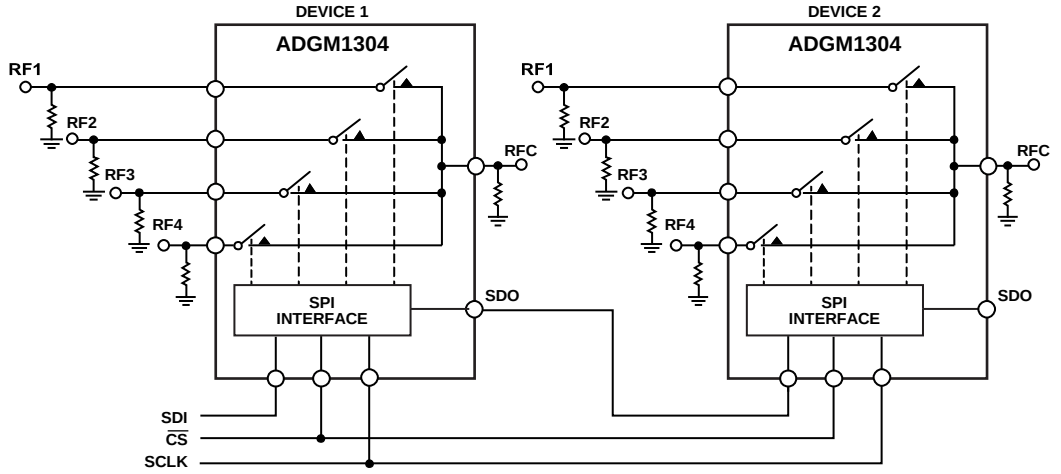

Figure 52. Two SPI-Controlled ADGM1304 Switches Connected in a Daisy-Chain Configuration

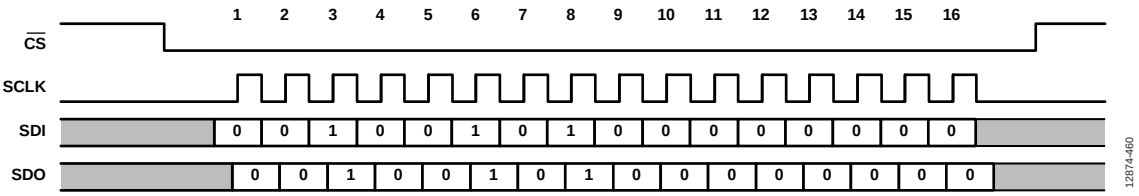

Figure 53. SPI Command to Enter Daisy-Chain Mode

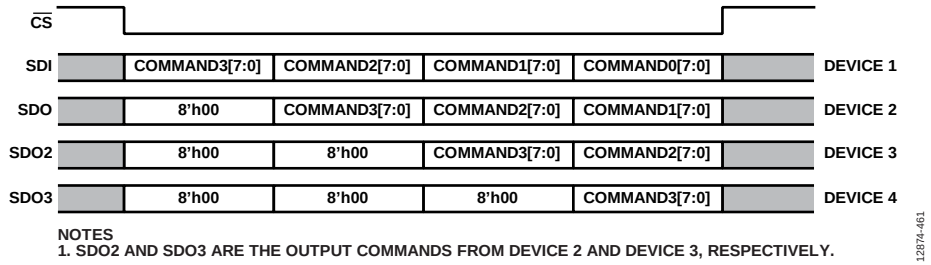

Figure 54. Example of a SPI Frame when Three ADGM1304 Devices are Connected in Daisy-Chain Mode

Hardware Reset

The digital portion of the ADGM1304 goes through an initialization phase during V_{DD} power up. To hardware reset the ADGM1304, power cycle the V_{DD} input. After power-up or a hardware reset, ensure there is a minimum of 10 µs before any SPI command is issued. Ensure that V_{DD} does not drop out during the 10 µs initialization phase because it may result in incorrect operation of the ADGM1304.

Internal Error Status

When an internal error is detected in the device, the internal error is flagged by the INTERNAL_ERROR bits (Bits[7:6]) of the SWITCH_DATA register (Register 0x20), as shown in Table 10. An internal error results from an error in the configuration of the device at power up.

INTERNAL OSCILLATOR FEEDTHROUGH

The ADGM1304 has an internal oscillator running at a nominal 10 MHz. This oscillator drives the charge pump circuitry that provides the actuation voltage for each of the switch gate electrodes. Although this oscillator is very low power, the 10 MHz signal is coupled to the switch and can be considered a noise spur on the switch channels. The magnitude of this feedthrough noise spur is specified in Table 1 and is typically −123 dBm or −146 dBm/Hz when one switch is on. When all four switches are simultaneously on, the feedthrough goes up to −120 dBm. V_{DD} level and temperature changes affect the frequency of the noise spur. For the maximum and minimum frequency range over temperature and voltage supply range, see Table 1.

INTERNAL OSCILLATOR FEEDTHROUGH MITIGATION

In normal operation, the 80 V actuation voltage is supplied by the driver IC. Setting the EXTD_EN pin (Pin 7) low enables the built in 10 MHz oscillator. This setting enables the charge pump circuitry to generate the 80 V required for MEMS switch actuation. The internal oscillator is a source of noise which couples through to the RF ports. The magnitude of this feedthrough noise spur is specified in Table 1 and is typically −123 dBm or −146 dBm/Hz when one switch is on. The internal oscillator feedthrough can be eliminated by setting the EXTD_EN pin high, which disables the internal oscillator and charge pump circuitry. When the internal oscillator and charge pump circuitry is disabled, the V_{CP} pin (Pin 24) must be driven with 80 V dc (VCP_{EXT}) from an external voltage supply, as outlined in Table 5, required for MEMS switch actuation. The switch can still be controlled via the digital logic interface pins or via SPI interface pins

LOW POWER MODE

Setting the EXTD_EN pin high shuts down the internal oscillator. The ADGM1304 enters low power quiescent state, drawing only 50 µA maximum supply current. When the internal oscillator and charge pump circuitry is disabled, the V_{CP} pin (Pin 24) must be driven with 80 V dc (VCP_{EXT}) from an external voltage supply, as outlined in Table 5, required for MEMS switch actuation. The switch can still be controlled via the digital logic interface pins or via SPI interface.

TYPICAL OPERATING CIRCUIT

Figure 55 shows the typical operating circuit for the ADGM1304 as used in the EVAL-ADGM1304SDZ. A 47 pF (100 V rated) external capacitor is required on the V_{CP} pin as a holding capacitor for the 80 V gate drive voltage. The V_{DD} pin is connected to a 3.3 V supply. However, V_{DD} can operate from 3.0 V to 3.6 V. RFGND is separated from AGND internally in the device.

It is recommended to connect RFGND to AGND using one large pad on the PCB to short together EP1 and EP2. Figure 55 shows the ADGM1304 configured to use the internal oscillator as the reference to the driver IC control circuit.

Alternatively, set Pin 7 (EXTD_EN) high and apply 80 V dc directly to Pin 24 to disable the internal oscillator and eliminate all oscillator feedthrough. The switches can then be controlled normally via the logic control interface (Pin 1 to Pin 4) or via the SPI interface.

To avoid any floating nodes, connect a 10 MΩ shunt resistor to RFGND on all RFx pins (RF1 to RF4, and RFC), as shown in Figure 55. See the Floating Node section for more information. An example of a 10 MΩ resistor that can be used with the MEMS switch is the Multicomp MCRE000262. The MCRE000262 is tested with the switch and has very small (negligible) impact on the RF performance of the MEMS switch.

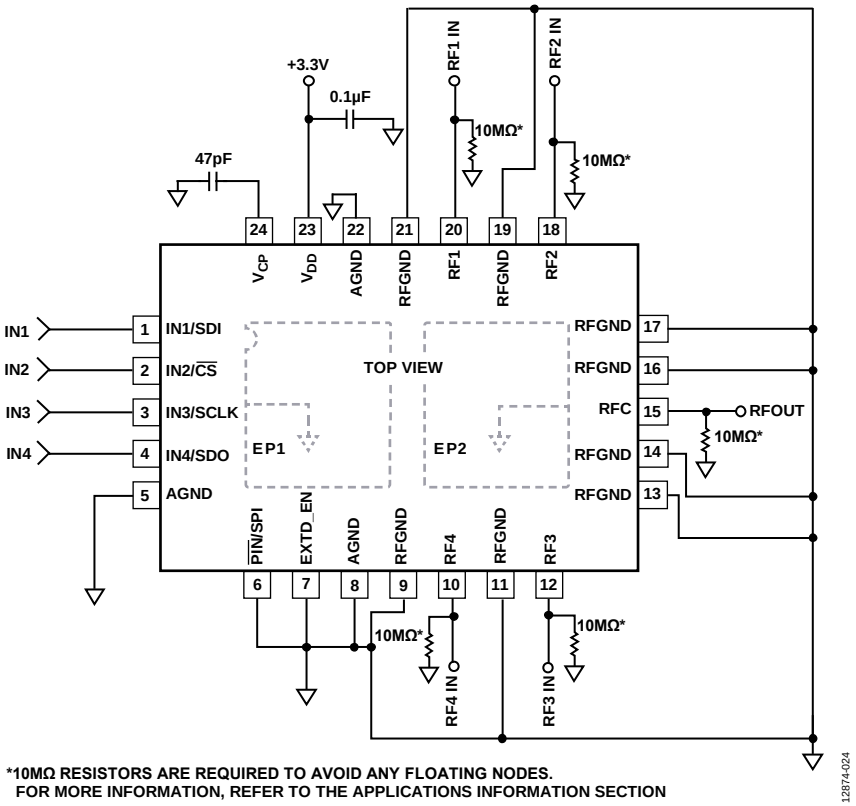

Figure 55. Typical Operating Circuit in Parallel Digital Interface Mode

APPLICATIONS INFORMATION

POWER SUPPLY RAILS

It is recommended that a 0.1 µF decoupling capacitor be added to the power supply port of the ADGM1304.

The ADGM1304 can operate with unipolar supplies between 3.0 V and 3.6 V.

The device is fully specified at a 3.3 V analog supply voltage.

POWER SUPPLY RECOMMENDATIONS

Analog Devices has a wide range of power management products to meet the requirements of most high performance signal chains.

An example of a unipolar power solution for the ADGM1304 is shown in Figure 56. The ADP7142 is a low dropout linear regulator that operates from 2.7 V to 40 V and is ideal for regulation of high performance analog and mixed-signal circuits operating from 39 V down to 1.2 V rails. The ADP7142 has 11 µV rms output noise independent of the output voltage. The ADP7142 can be used to power the supply rail for the ADGM1304, a microcontroller, and/or other devices in the signal chain.

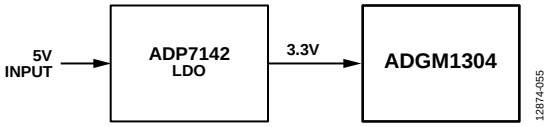

Figure 56. Unipolar Power Solution

If low noise performance at the power supply is required, the ADP7142 can be replaced by the LT1962 or the LT3045-1.

Table 7. Recommended Power Management Devices

Product	Description
ADP7142	40 V, 200 mA, low noise, CMOS LDO linear regulator
LT1962	300 mA, low noise, micropower, LDO regulator
LT3045-1	20 V, 500 mA, ultralow noise, ultrahigh PSRR linear regulator with VIOC control

SWITCHABLE RF ATTENUATOR

It is common to see RF attenuator networks used in RF instrumentation equipment such as vector network analyzers, spectrum analyzers, and signal generators. Routing RF signals through an attenuator enables the equipment to accept higher power signals and increase the dynamic range of the instrument. In RF attenuation applications like the vector network analyzers, spectrum analyzers, and signal generators, maintaining the bandwidth of the signal after it passes through the network is critical. Any degradation of the signal reduces the performance of the equipment. Therefore, the RF characteristics of the switches used for routing are integral to the quality of an attenuator network.

The ADGM1304 MEMS switch is suited for use as a switchable RF attenuator due to its low flat insertion loss, very wide RF bandwidth, and high reliability. The ADGM1304, as an SP4T switch, also provides added flexibility. Figure 57 shows an example attenuation network configuration using two ADGM1304 switches and three different attenuators. The fourth channel of the switches is used as a nonattenuated route.

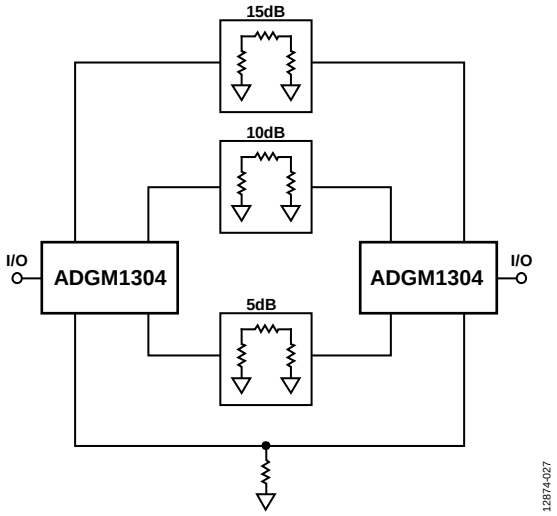

Figure 57. Switching RF Attenuators Using ADGM1304 MEMS Switches

RECONFIGURABLE RF FILTER

A reconfigurable RF filter is advantageous in many RF front-end applications. A reconfigurable RF filter provides more saved space. As space becomes more constrained in applications, it is useful to have the option of using an economical reconfigurable RF filter instead of individual frequency dependent filters.

The ADGM1304 has low flat insertion loss, very wide RF bandwidth, low parasitic, low capacitance, and high linearity, and as such, is needed to turn on the lump components (capacitor and inductor). As such, the MEMS switch is suited for reconfigurable filter application.

In applications such as wireless communications or mobile radios, the number of bands and modes constantly increases. A reconfigurable RF filter allows more bands and modes to be covered using the same components.

Figure 58 shows an example of a reconfigurable band-pass filter. The topology shown is of a generalized two section, inductively coupled, single-ended band-pass filter that is nominally centered on 400 MHz (ultrahigh frequency (UHF) band). The MEMS switches are positioned in series with each of the shunt inductors.

Different functions of the switches include or omit a shunt inductor from the circuit. Changing the shunt inductor value affects the bandwidth and center frequency of the filter. Using inductance values from 15 nH to 30 nH significantly alters the bandwidth and center frequency, allowing the filter to dynamically configure to operate in the UHF band or very high frequency (VHF) band while preserving the 50 Ω match on the input and output ports. The low R_{ON} value and large bandwidth of the MEMS switch makes it an ideal choice for dynamic configuration. The low R_{ON} reduces the negative effect a series resistance has on the quality of the shunt inductor. The large bandwidth enables higher frequency band-pass filters.

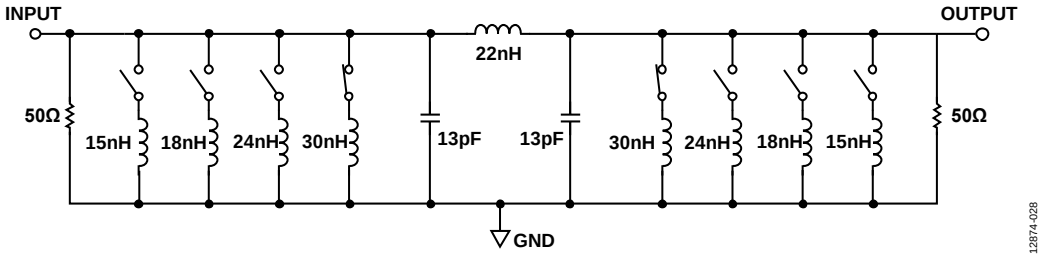

Figure 58. Reconfigurable Band-Pass Filter Realized Using Two ADGM1304 MEMS Switches

CRITICAL OPERATIONAL REQUIREMENTS

SYSTEM ERROR CONSIDERATIONS DUE TO ON-RESISTANCE DRIFT

The R_{ON} performance of the ADGM1304 is affected by device to device variation, channel to channel variation, cycle actuations, settling time post turn on, bias voltage, and temperature changes (see Figure 6 to Figure 12 and Figure 60).

In a 50 Ω system, the on-resistance drift over switch actuations (ΔR_{ON}) can introduce system inaccuracy. Figure 59 shows the ADGM1304 connected with the load in a 50 Ω system, where R_S is the source impedance. To calculate the system error caused by the ADGM1304 on-resistance drift, use the following equation:

$$System\ Error\ (\%) = \Delta R/R_{LOAD}$$

where:
ΔR is the ADGM1304 on-resistance drift.
R_{LOAD} is the load impedance.

The ADGM1304 on-resistance drift also affects insertion loss, which must be considered when using the device. To calculate the on-resistance impact on insertion loss, use the following equation:

$$Insertion\ Loss = 10\log(1 + (\Delta R/R_{LOAD}))$$

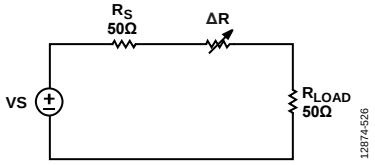

Figure 59. 50 Ω System Representation Where the ADGM1304 Is Connected with the Load

Table 8. System Error and Insertion Loss Error Due to ADGM1304 R_{ON} Drift

On-Resistance Drift	System Error (%)	Insertion Loss Error (dB)
4.75	9.5	0.39
5	10	0.41

The on-resistance drift over time specification is −0.25 Ω measured after 100 ms, as shown in Figure 8 to Figure 10. According to the plots, the on-resistance drift over time is −0.12 Ω after 100 ms. The on resistance of the ADGM1304 typically drifts by −0.05 Ω per decade. For example, after 100 ms, the on resistance drifts −0.12 Ω. After 1 sec, the on resistance drifts −0.17 Ω, and after 10 sec, it drifts −0.22 Ω. Therefore, after 1000 sec, the on resistance is expected to drift by −0.32 Ω.

ON-RESISTANCE SHIFT DUE TO TEMPERATURE SHOCK POST ACTUATIONS

When the switch is actuated multiples times at one temperature, and if there is a sudden shift in this temperature, a large shift is shown in the switch R_{ON}. Figure 60 shows the absolute R_{ON} performance of the population of devices over actuation lifetime. Figure 60 shows how the absolute R_{ON} of the device drifts over actuation lifetime. During this measurement, the switch is actuated at 85°C and the switch R_{ON} is measured at 25°C. Actuating the switch at 85°C and measuring R_{ON} at 25°C is the most severe condition for the ADGM1304 R_{ON} drift over actuations.

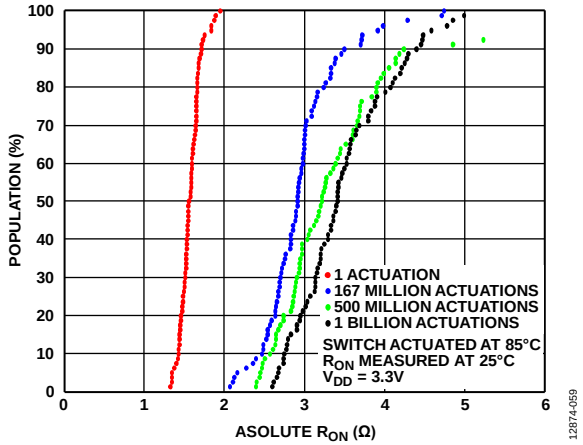

Figure 60. Population vs. Absolute R_{ON}, Switch Actuated at 85°C and R_{ON} Measured at 25°C

HOT SWITCHING

Hot switching is caused by cycling the switch on or off with a signal applied to the switch. The presence of the applied signal during switching cycle damages the switch contacts. Hot switching damage is dependent on the current or the voltage levels. Hot switching causes a significant reduction in the cycle lifetime of the switch, as shown in Table 1, Figure 13, and Figure 14.

Figure 61 shows the hot switching condition when the switch is turned on with a 1 V signal present at the switch terminal during switching.

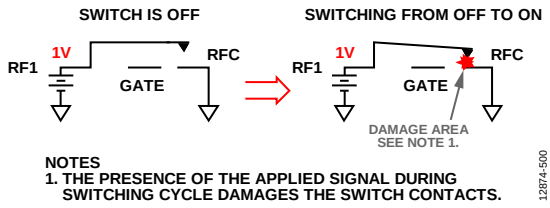

Figure 61. Hot Switching Condition When Turning the Switch from Off to On State

Figure 62 shows the hot switching condition when the switch is turned off with 10 mA passing through the switch during switching.

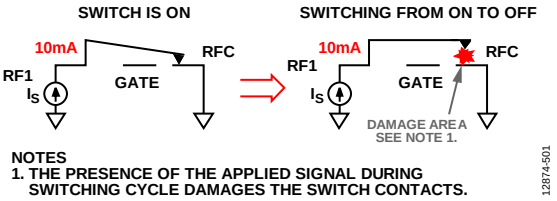

Figure 62. Hot Switching Condition When Turning the Switch from On to Off State

FLOATING NODE

The ADGM1304 has no internal impedance to ground, and charges can develop on the switch terminals, leading to unreliable switch behavior. To mitigate this behavior, provide a discharge path to all switch nodes. Figure 63 to Figure 66 show examples of cases to avoid where floating nodes can occur when using the switch. Conditions to avoid include the following:

- Leaving the RFx pins open circuit (see Figure 63).
- Connecting a series capacitor directly to the switch (see Figure 64).
- Connecting the RFx pin of two switches together directly or connecting the RFC pin to the RFx pin (see Figure 65 and Figure 66).

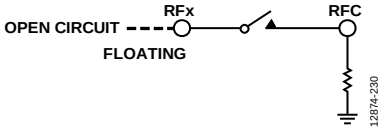

Figure 63. RFx Pins Left Open Circuit

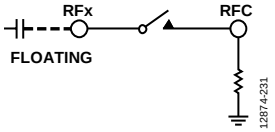

Figure 64. Series Capacitor Directly Connected to MEMS Switch

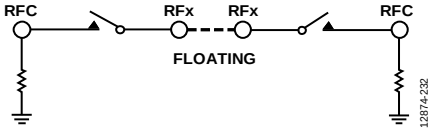

Figure 65. RFx Pins of Two MEMS Switches Directly Connected

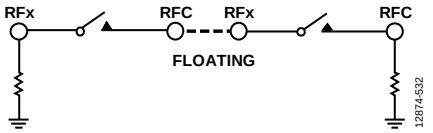

Figure 66. RFC Connected to RFx

Provide a discharge path to the switch nodes to avoid floating nodes. In a typical application, a 50 Ω termination connected to the switch provides this path. Driving switch nodes with a device of adequate impedance (<10 MΩ) provides a discharge path. If there is no discharge path in the application circuit, add a 10 MΩ shunt resistor or inductor on the source RFx pin of the MEMS switch to provide the discharge path. Note that the shunt resistors introduce leakage. Figure 67 shows an example of a configuration providing a discharge path.

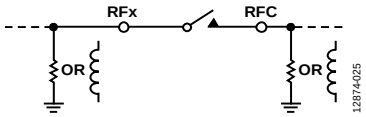

Figure 67. Switch Configuration Providing a Discharge Path

Figure 68 and Figure 69 illustrate typical cascaded switch use cases and the corresponding schemes to mitigate floating node risks.

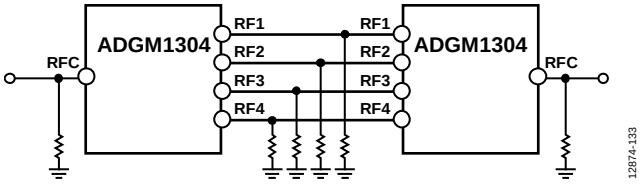

Figure 68. Two ADGM1304 Devices Connected in Path Selection Configuration with 10 MΩ Shunt Resistors to Mitigate Floating Nodes

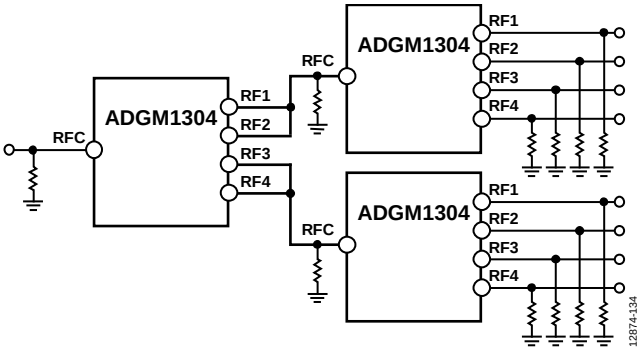

Figure 69. Three ADGM1304 Devices Connected in Fanout Configuration with 10 MΩ Shunt Resistors to Mitigate Floating Nodes

Avoid connecting shunt capacitors directly to the switch. A capacitor can store a charge and potentially lead to hot switching events when the switch opens or closes if there are no alternative discharge paths. These events affect the cycle lifetime of the switch.

CUMULATIVE ON SWITCH LIFETIME

Leaving the switch in an on state for a long period affects the lifetime of the switch because of mechanical degradation effects. These effects can result in the switch failing to turn off. Figure 70 shows a failure rate at 50°C where the mean time to failure is 7.2 years (2628 days), resulting in 50% of the sample lot failing at this point.

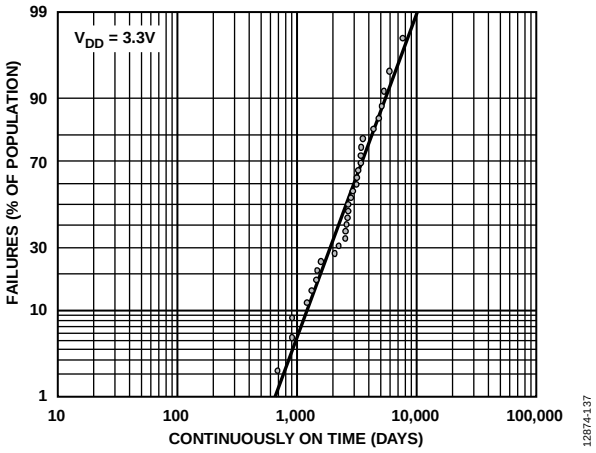

Figure 70. Cumulative On Switch Lifetime at 50°C, V_{DD} = 3.3 V, Sample Size = 31 Devices

Temperatures above 50°C further reduce the switch lifetime. The cumulative on switch lifetime specification is also duty cycle dependent. If the user operates the MEMS switch with a duty cycle of less than 50%, the lifetime of the MEMS switch improves.

HANDLING PRECAUTIONS

ESD Precautions

All RFx pins of the ADGM1304 pass the following ESD limits:

- 100 V, Class 0 HBM, ANSI/ESDA/JEDEC JS-001-2010
- 500 V, Class C2 FICDM, JEDEC JESD22_C101E

All the RFx pins are rated to 500 V FICDM, making the device safe for automated handling and assembly process. Standard ESD precautions should be taken during manufacturing.

100 V HBM rating of ADGM1304 is susceptible to ESD surge due to human body contact. ESD protection should be added if human body contact is expected.

Electrical Overstress (EOS) Precautions

The ADGM1304 is susceptible to EOS. Therefore, take the following precautions:

- The ADGM1304 is an ESD sensitive device. Ensure to take all normal handling precautions, including working only on static dissipative surfaces, wearing wrist straps or other ESD control devices, and storing unused devices in conductive foam.
- Avoid running measurement instruments, such as digital multimeters (DMMs), in autorange modes. Some instruments generate large transient compliance voltages when switching between ranges.
- Use the highest practical DMM range setting (the lowest resolution) for resistance measurements to minimize compliance voltages, particularly during switching.
- Discharge coaxial cables before connecting directly to the switch. Note that coaxial cables can store charge and lead to EOS when directly connected to the switch.
- Avoid connecting large capacitive terminations directly to the switch, as shown in Figure 71. A shunt capacitor can store a charge that potentially leads to hot switching events when the switch opens or closes, affecting the lifetime of the switch.

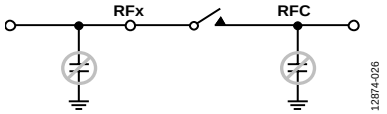

Figure 71. Avoid Having a Large Capacitor Directly Connected to the MEMS Switch

Mechanical Shock Precautions

The ADGM1304 passes Group D mechanical shocks tests, as detailed in Table 3 in the Absolute Maximum Ratings section. These tests validate the robustness of the device to typical mechanical shocks.

Do not use the device if dropped. To reduce excessive mechanical shock and ESD events, avoid handling of loose devices, as shown in Figure 72.

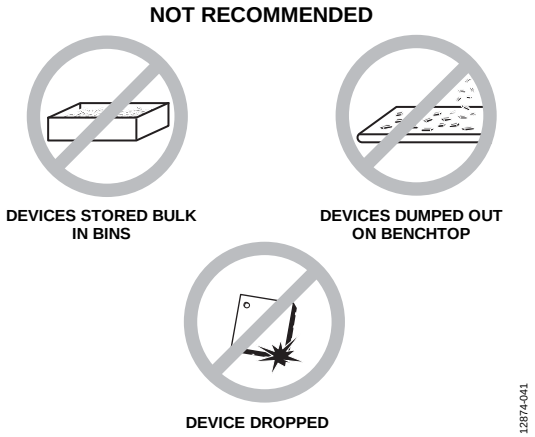

Figure 72. Situations to Avoid During Handling

REGISTER SUMMARY AND DETAILS

Table 9. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x20	SWITCH_DATA	[7:0]	INTERNAL_ERROR		RESERVED		SW4_EN	SW3_EN	SW2_EN	SW1_EN	0x00	R/W

SWITCH DATA REGISTER

Address: 0x20, Reset: 0x00, Name: SWITCH_DATA

The switch data register controls the status of the four switches of the ADGM1304.

Table 10. Bit Descriptions for SWITCH_DATA

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	INTERNAL_ERROR		Internal Error Detection. These bits determine if an internal error has occurred.	0x0	R
		00	No error detected.		
		01	Error detected.		
		10	Error detected.		
		11	Error detected.		
[5:4]	RESERVED		Reserved. These bits are reserved. Set these bits to 0.	0x0	R
3	SW4_EN		Enable for Switch 4.	0x0	R/W
		0	Switch 4 open.		
		1	Switch 4 closed.		
2	SW3_EN		Enable for Switch 3.	0x0	R/W
		0	Switch 3 open.		
		1	Switch 3 closed.		
1	SW2_EN		Enable for Switch 2.	0x0	R/W
		0	Switch 2 open.		
		1	Switch 2 closed.		
0	SW1_EN		Enable for Switch 1.	0x0	R/W
		0	Switch 1 open.		
		1	Switch 1 closed.		

OUTLINE DIMENSIONS

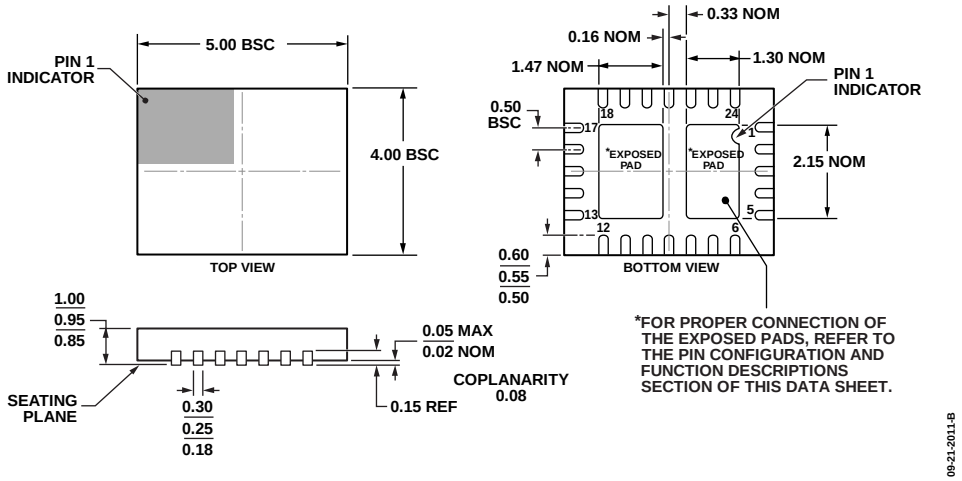

Figure 73. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 4 mm Body, Very Thin Quad
(CP-24-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADGM1304JCPZ-R2	0°C to 85°C	24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-24-9
ADGM1304JCPZ-RL7	0°C to 85°C	24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-24-9
EVAL-ADGM1304SDZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

D12874-2/22(H)