

1 Channel Compact High Side Switch ICs

Automotive 1ch Adjustable Current Limit High Side Switch ICs

BD22441G-C

General Description

BD22441G-C is low on-resistance N-channel MOSFET high-side power switch, optimized for Universal Serial Bus (USB) applications. BD22441G-C is equipped with the function of over-current detection, thermal shutdown, under-voltage lockout and soft-start. Moreover, the range of Current limit threshold can be adjusted from 0.2A to 1.7A by changing the external resistance.

Key Specifications

- IN Operating Voltage: 2.8V to 5.5V
- On Resistance: (VIN=5V) 100mΩ(Typ)
- Current Limit Threshold: 0.2A to 1.7A adjustable
- Standby Current: 0.01 μA (Typ)
- Operating Temperature Range: -40°C to +125°C

Features

- AEC-Q100 Qualified^(Note 1)
 - Adjustable Current Limit Threshold: 0.2A to 1.7A
 - Built-in Low On-Resistance (Typ 100mΩ) N-channel MOSFET Built-in
 - Soft-Start Circuit
 - Output Discharge Function
 - Open-Drain Fault Flag Output
 - Thermal Shutdown
 - Under-Voltage Lockout
 - Reverse Current Protection when Power Switch Off
- (Note 1: Grade1)

Package

SSOP6

W(Typ) x D(Typ) x H(Max)
2.90mm x 2.80mm x 1.25mm



Applications

Car accessory

Typical Application Circuit

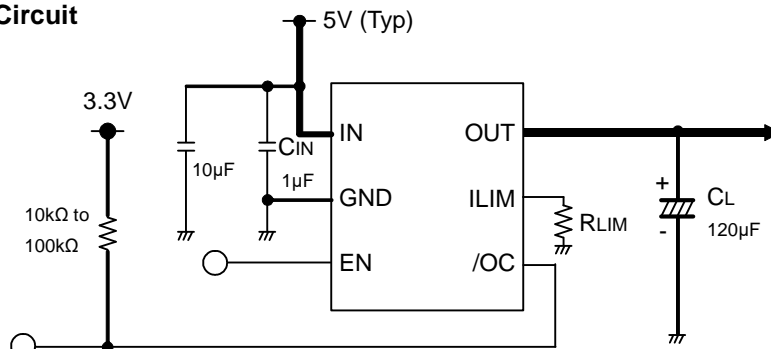


Figure 1. Typical Application Circuit

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays

Block Diagram

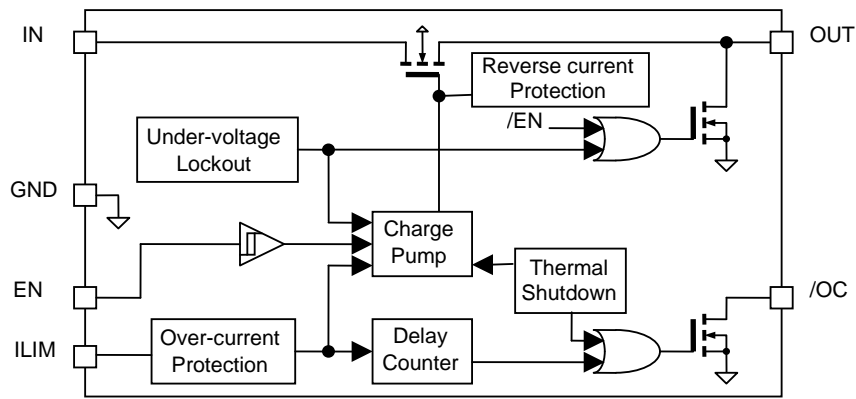


Figure 2. Block Diagram

Pin Configuration

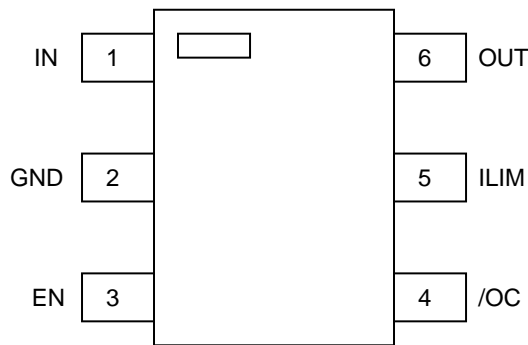


Figure 3. Pin Configuration (TOP VIEW)

Pin Descriptions

Pin No.	Symbol	I/O	Function
1	IN	I	Switch input and the supply voltage for the IC.
2	GND	-	Ground.
3	EN	I	Enable input. High-level input turns on the switch.
4	/OC	O	Over-current detection terminal. Low level output during over-current or over-temperature condition. Open-drain fault flag output.
5	ILIM	O	Current limit threshold set Pin. External resistor used to set Current limit threshold. Recommended $11.97\text{ k}\Omega \leq R_{LIM} \leq 106.3\text{ k}\Omega$
6	OUT	O	Power switch output.

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
IN Supply Voltage	V _{IN}	-0.3 to +7.0	V
EN Input Voltage	V _{EN}	-0.3 to +7.0	V
ILIM Voltage	V _{ILIM}	-0.3 to +7.0	V
ILIM Source Current	I _{ILIM}	1	mA
/OC Voltage	V _{/OC}	-0.3 to +7.0	V
/OC Sink Current	I _{/OC}	10	mA
OUT Voltage	V _{OUT}	-0.3 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _d	0.67 ^(Note1)	W

(Note 1) Mounted on 70mm x 70mm x 1.6mm glass epoxy board. Reduce 5.4mW per 1°C above 25°C

Caution1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Recommended Operating Conditions

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
IN Operating Voltage	V _{IN}	2.8	5.0	5.5	V
Operating Temperature	T _{OPR}	-40	-	+125	°C

Electrical Characteristics (V_{IN} = 5V, R_{LIM} = 20kΩ, -40°C ≤ T_j ≤ +125°C, unless otherwise specified.)

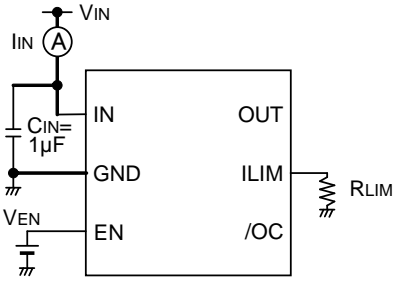
DC Characteristics

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Operating Current	I _{DD}	-	120	220	μA	V _{EN} = 5V, V _{OUT} = open
Standby Current	I _{STB}	-	0.01	10	μA	V _{EN} = 0V, V _{OUT} = open
EN Input Voltage	V _{ENH}	2.3	-	-	V	High input
	V _{ENL}	-	-	0.7	V	Low input
EN Input Leakage	I _{EN}	-1	0.01	1	μA	V _{EN} = 0V or 5V
On-Resistance	R _{ON}	-	100	280	mΩ	I _{OUT} = 500mA
Reverse Leak Current	I _{REV}	-	-	10	μA	V _{OUT} = 5V, V _{IN} = 0V
Current Limit Threshold	I _{TH}	122	212	330	mA	R _{LIM} = 100kΩ
		822	1028	1234		R _{LIM} = 20kΩ
		1405	1696	1987		R _{LIM} = 12kΩ
Output Discharge Resistance	R _{DISC}	-	60	180	Ω	I _{OUT} = 1mA, V _{EN} = 0V
/OC Output Low Voltage	V _{/OC}	-	-	0.4	V	I _{/OC} = 1mA
UVLO Threshold	V _{TUVH}	2.30	2.55	2.80	V	V _{IN} increasing
	V _{TUVL}	2.25	2.50	2.75	V	V _{IN} decreasing

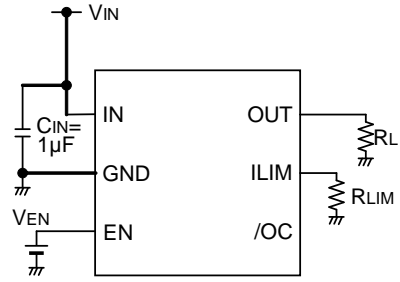
AC Characteristics

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Output Rise Time	t _{ON1}	-	0.6	1.8	ms	R _L = 100Ω
Output Turn-On Time	t _{ON2}	-	1	3	ms	
Output Fall Time	t _{OFF1}	-	1.8	20	μs	
Output Turn-Off Time	t _{OFF2}	-	3.2	40	μs	
/OC Delay Time	t _{/OC}	4	7	12	ms	

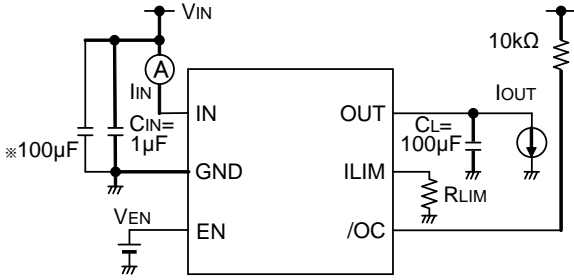
Measurement Circuit



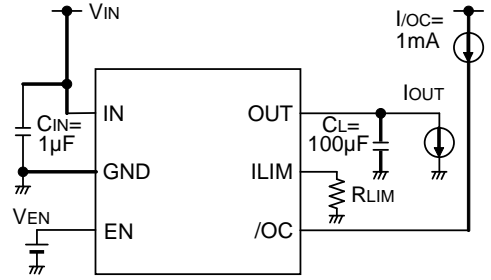
A. Operating Current, Standby Current



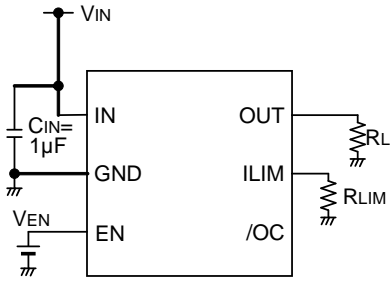
B. EN Input Voltage, Output Rise/Fall Time
Output Turn-On/ Turn-Off Time



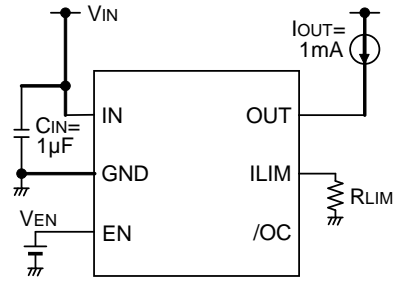
C. On-Resistance, Current Limit Threshold, /OC Delay Time
* Use capacitance more than 100µF at output short circuit test by using external power supply.



D. /OC Output Low Voltage



E. UVLO Threshold



F. Output Discharge Resistance

Figure 4. Measurement Circuit

Timing Diagram

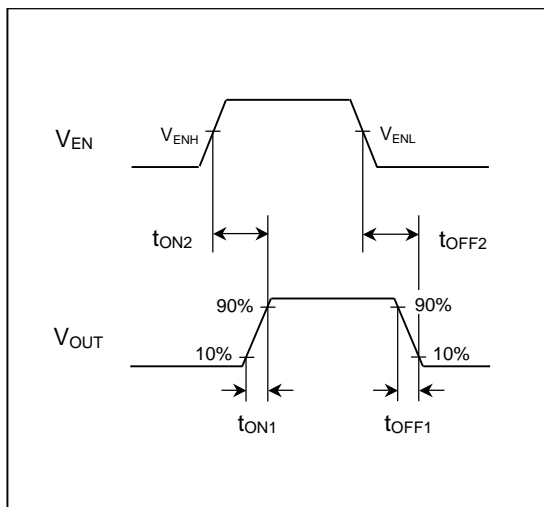


Figure 5. Output Rise/Fall Time

Typical Performance Curves

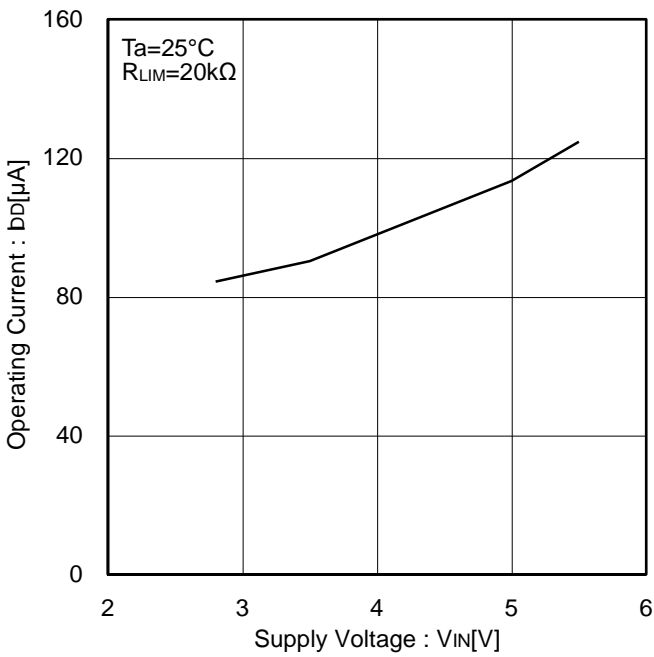


Figure 6. Operating Current vs Supply Voltage (EN Enable)

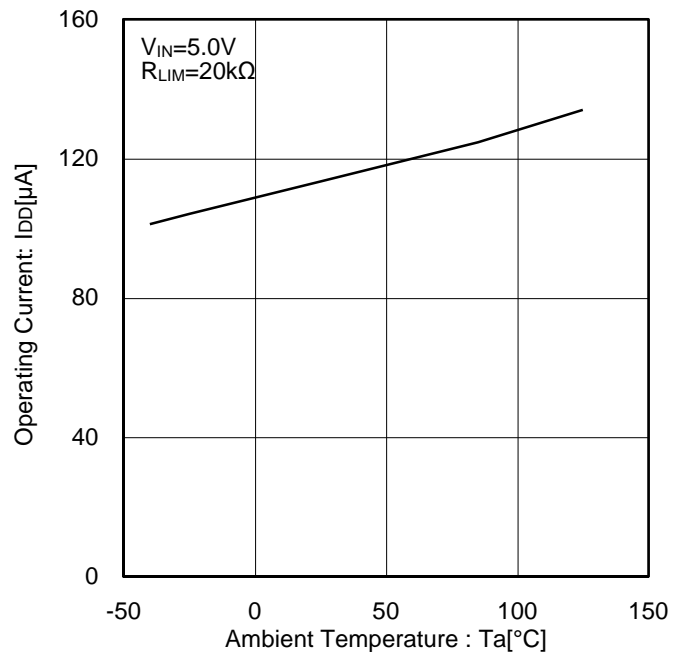


Figure 7. Operating Current vs Ambient Temperature (EN Enable)

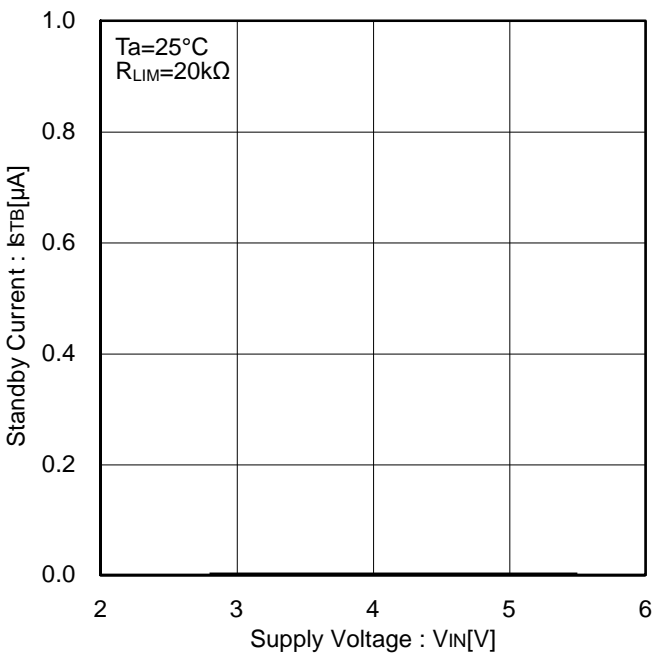


Figure 8. Standby Current vs Supply Voltage (EN Disable)

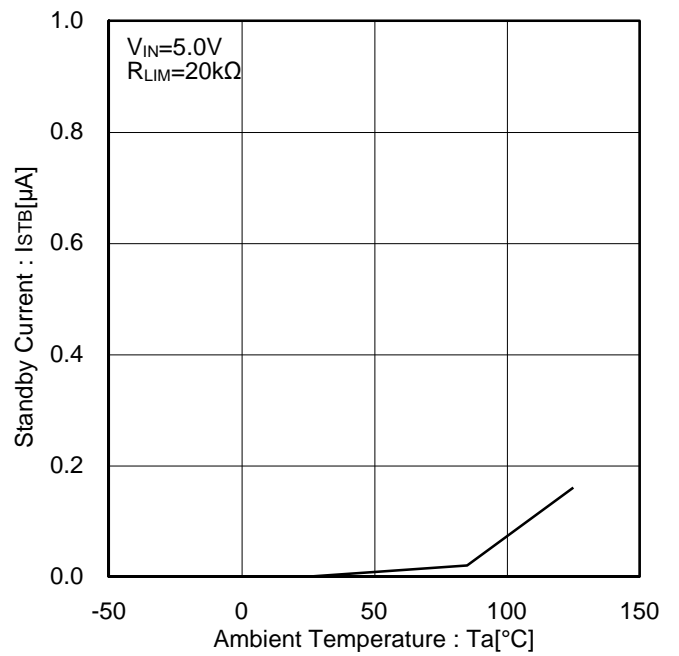


Figure 9. Standby Current vs Ambient Temperature (EN Disable)

Typical Performance Curves - continued

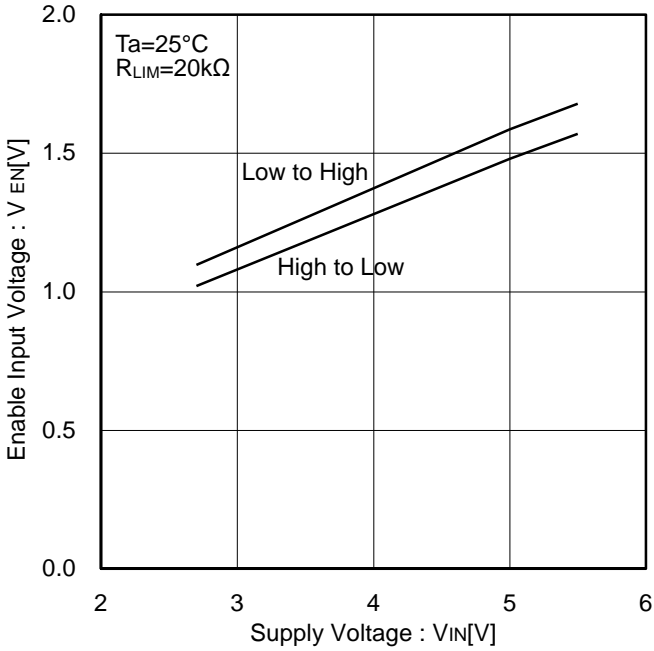


Figure 10. EN Input Voltage vs Supply Voltage

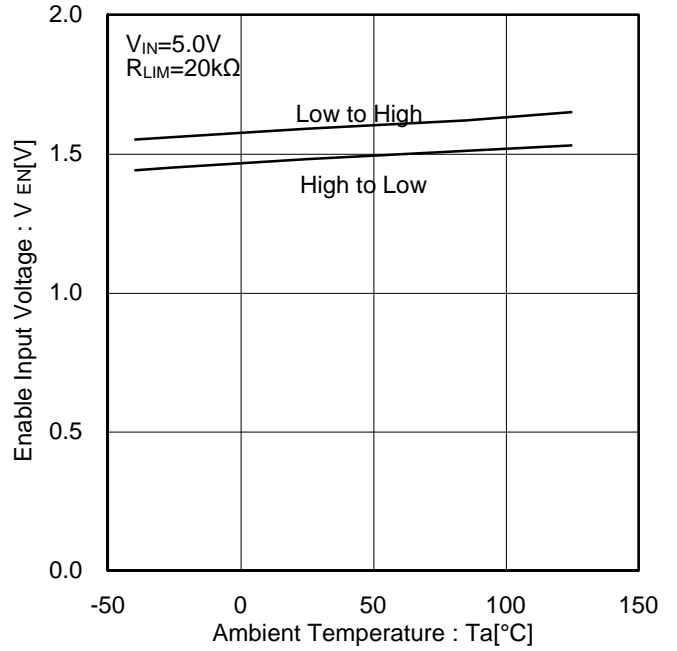


Figure 11. EN Input Voltage vs Ambient Temperature

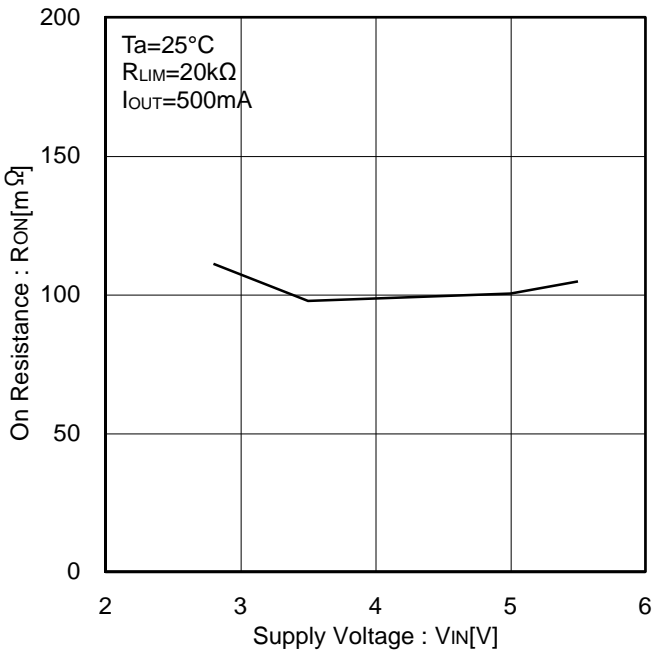


Figure 12. On-Resistance vs Supply Voltage

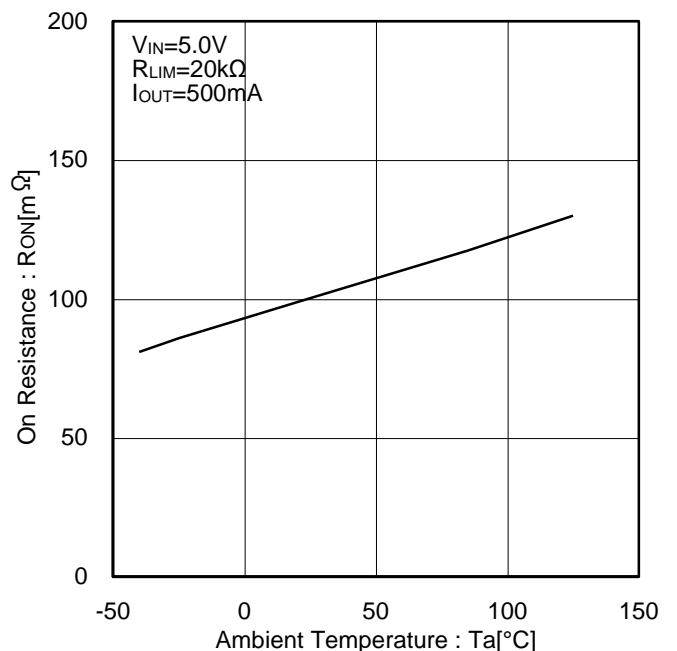


Figure 13. On-Resistance vs Ambient Temperature

Typical Performance Curves - continued

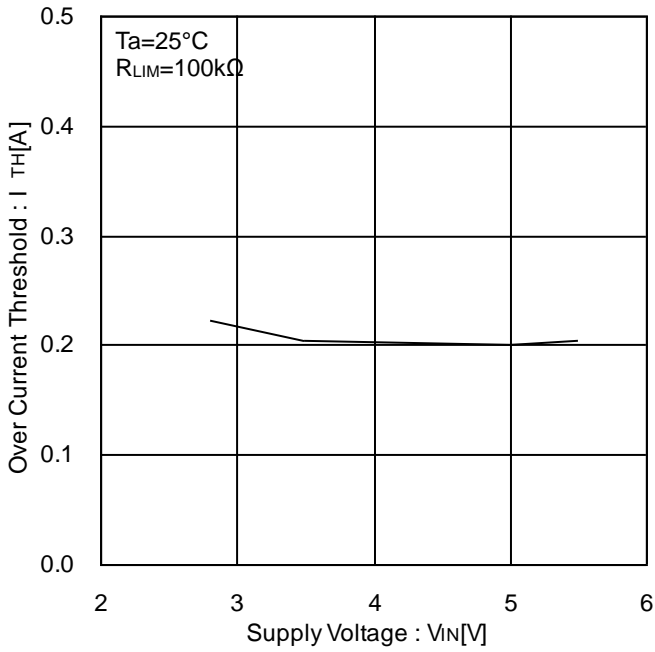


Figure 14. Over Current Threshold 1 vs Supply Voltage

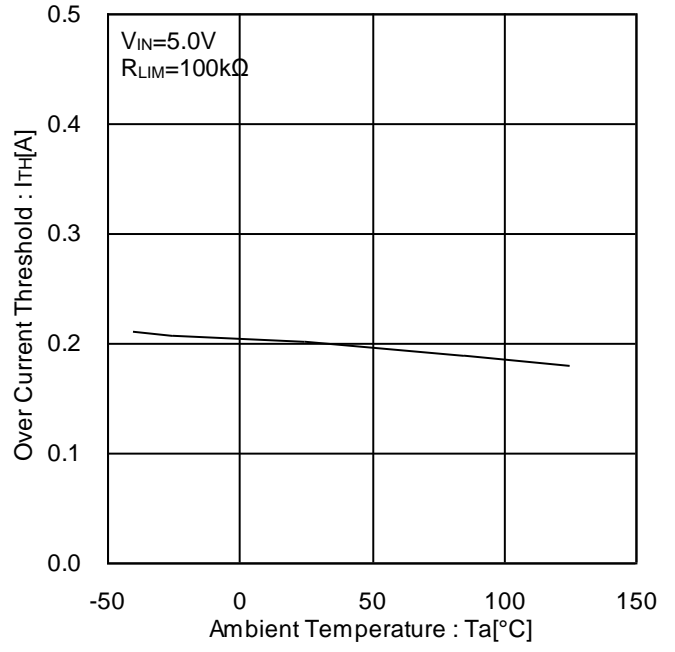


Figure 15. Over Current Threshold 1 vs Ambient Temperature

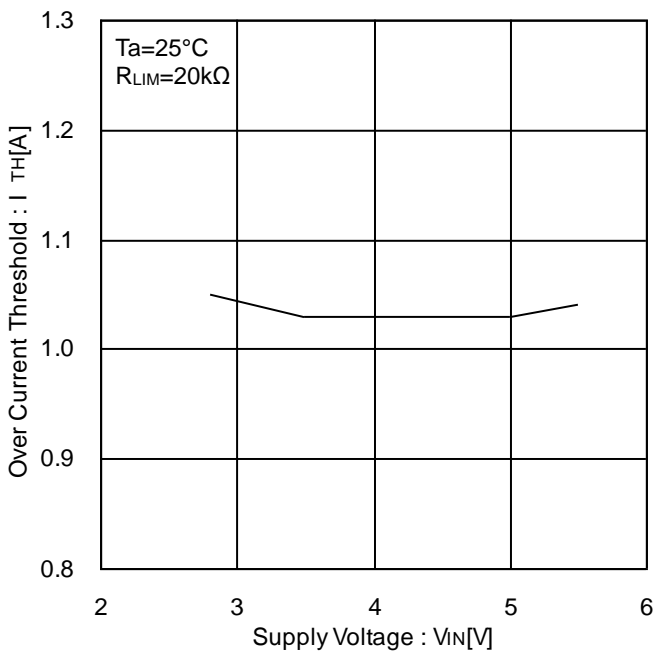


Figure 16. Over Current Threshold 2 vs Supply Voltage

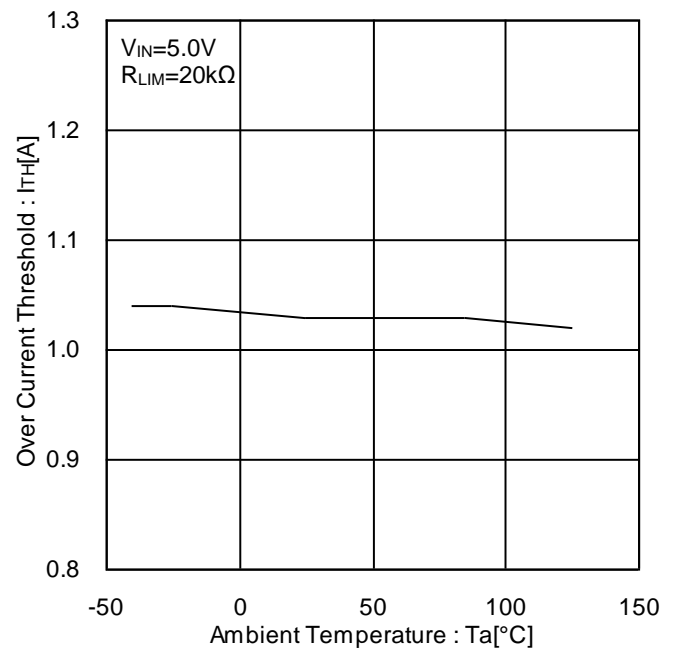


Figure 17. Over Current Threshold 2 vs Ambient Temperature

Typical Performance Curves - continued

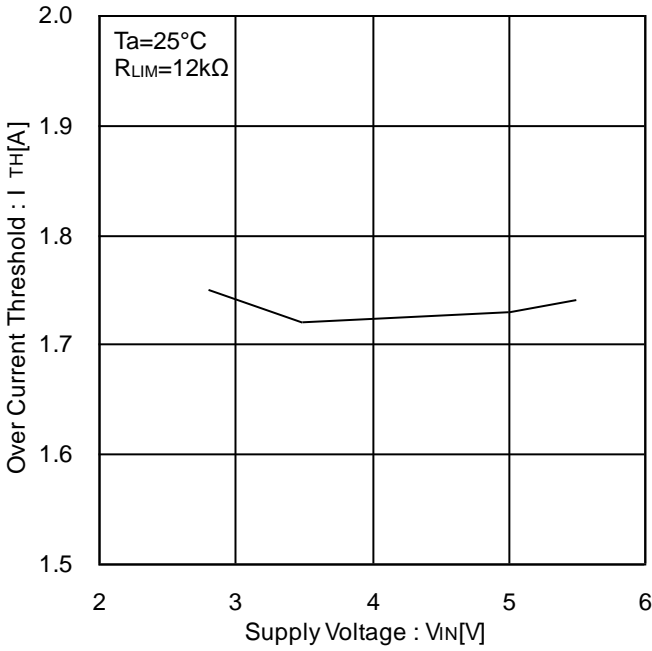


Figure 18. Over Current Threshold 3 vs Supply Voltage

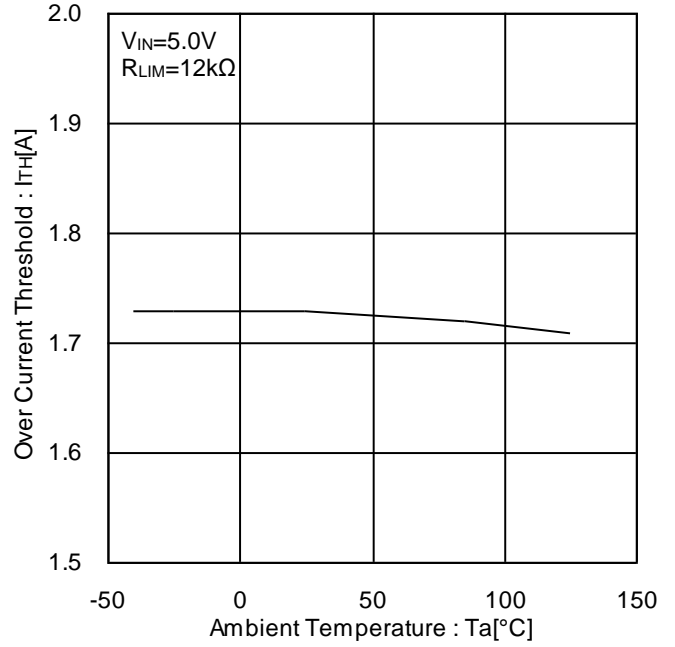


Figure 19. Over Current Threshold 3 vs Ambient Temperature

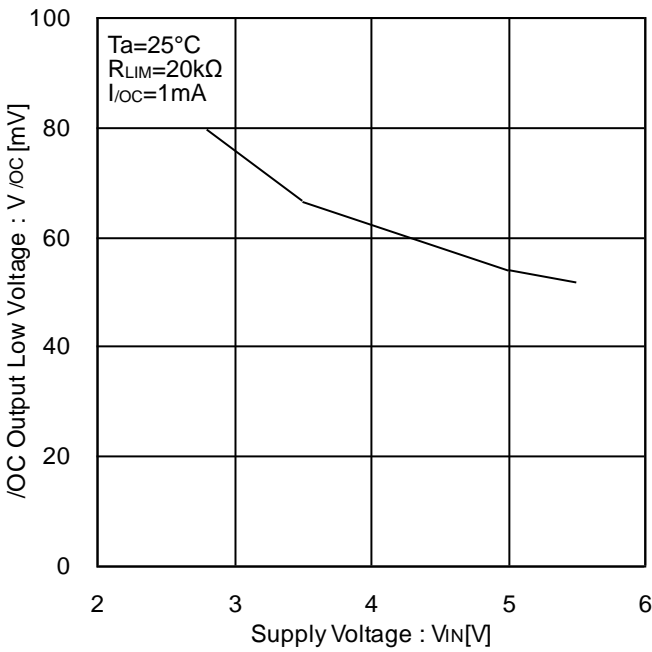


Figure 20. /OC Output Low Voltage vs Supply Voltage

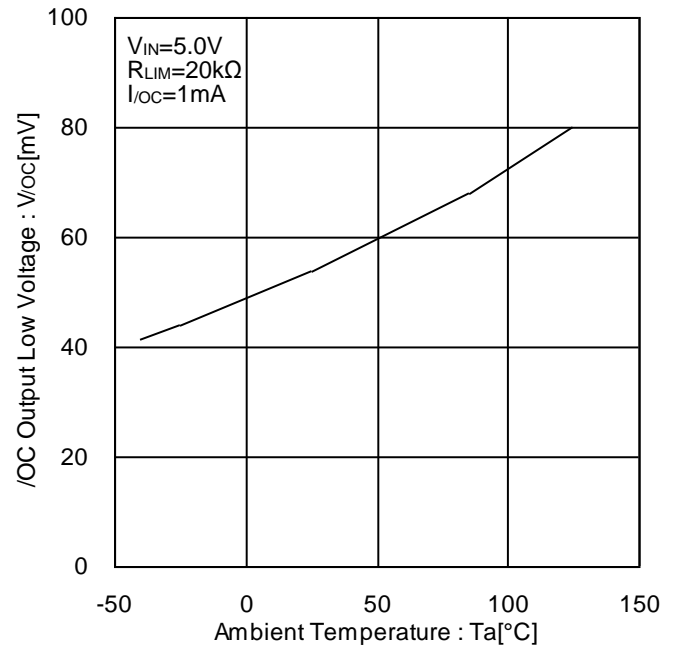


Figure 21. /OC Output Low Voltage vs Ambient Temperature

Typical Performance Curves - continued

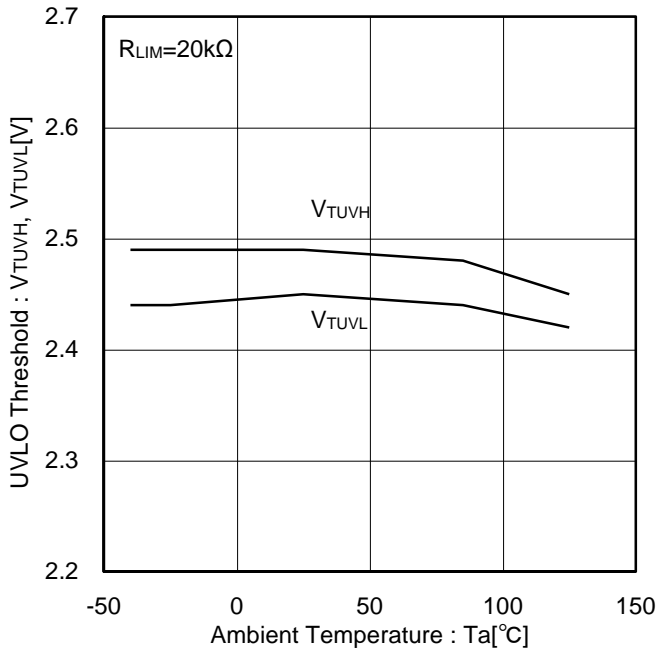


Figure 22. UVLO Threshold vs Ambient Temperature

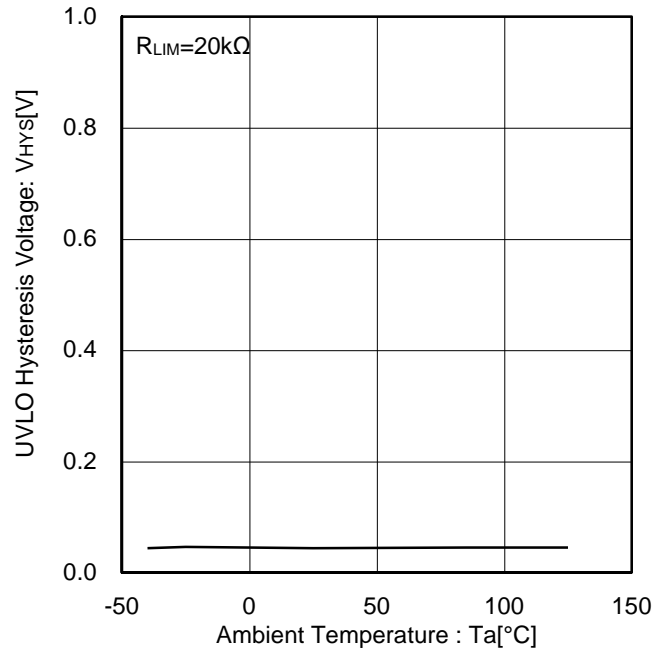


Figure 23. UVLO Hysteresis Voltage vs Ambient Temperature

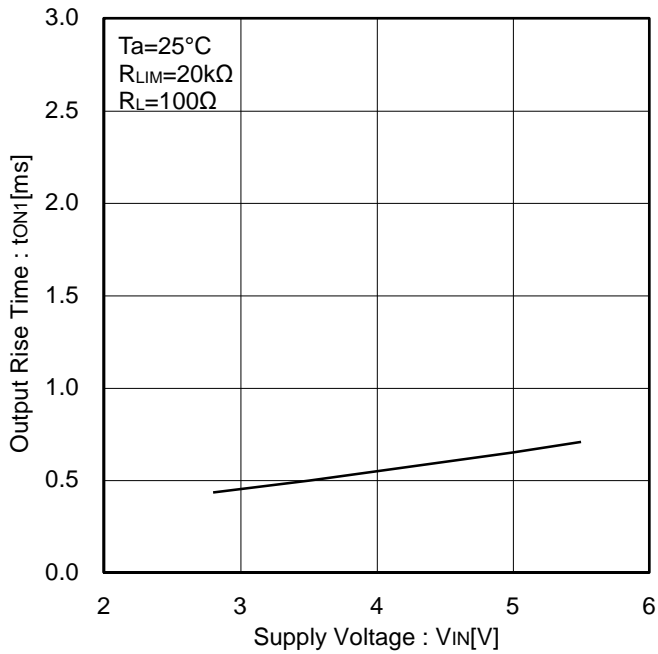


Figure 24. Output Rise Time vs Supply Voltage

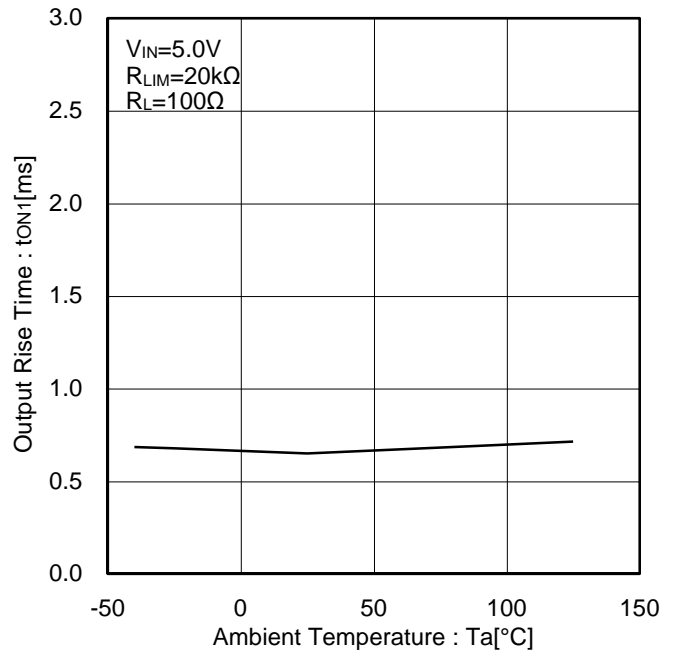


Figure 25. Output Rise Time vs Ambient Temperature

Typical Performance Curves - continued

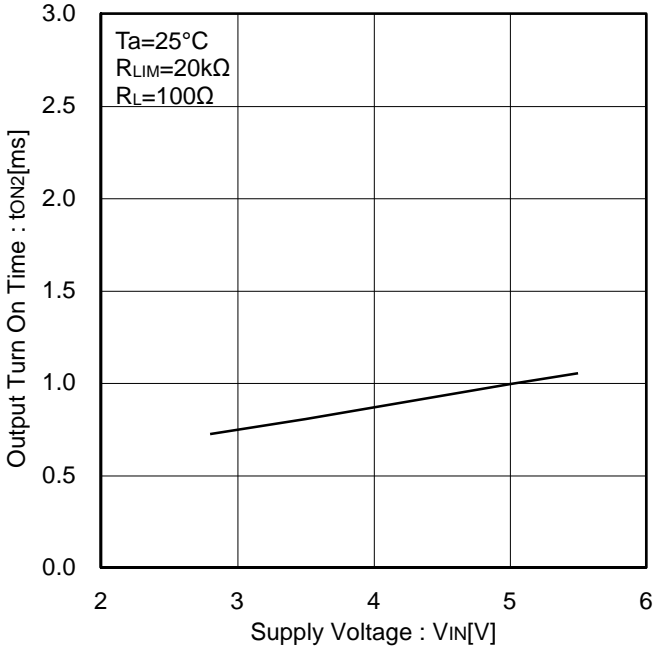


Figure 26. Output Turn On Time vs Supply Voltage

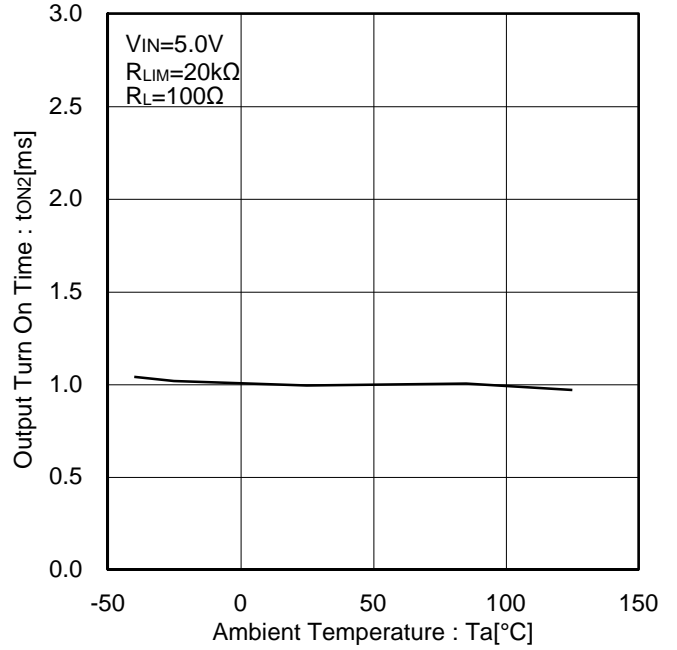


Figure 27. Output Turn On Time vs Ambient Temperature

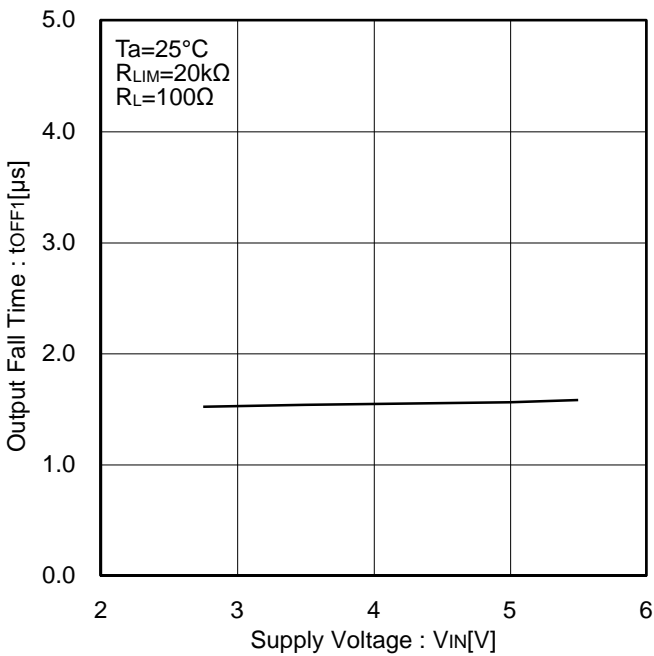


Figure 28. Output Fall Time vs Supply Voltage

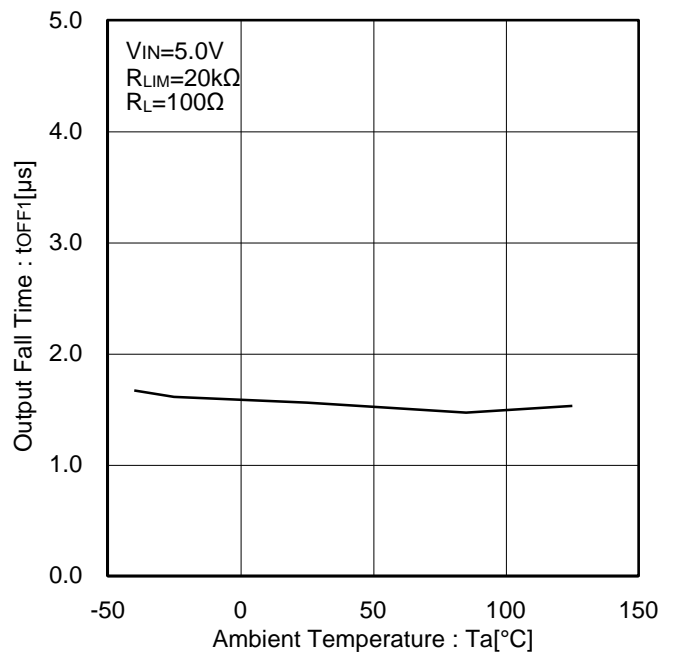


Figure 29. Output Fall Time vs Ambient Temperature

Typical Performance Curves - continued

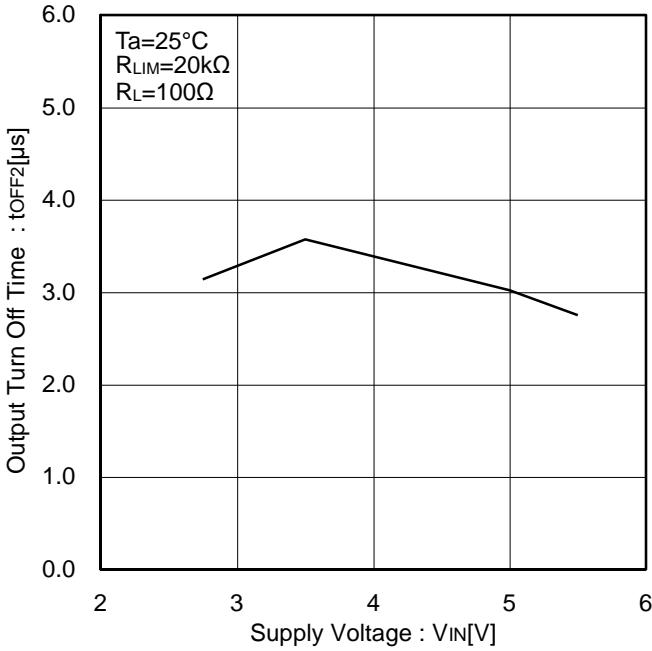


Figure 30. Output Turn Off Time vs Supply Voltage

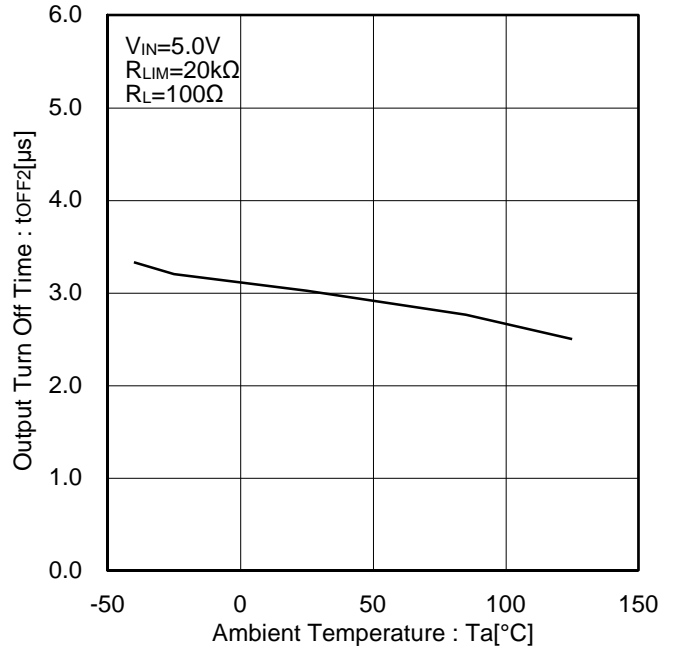


Figure 31. Output Turn Off Time vs Ambient Temperature

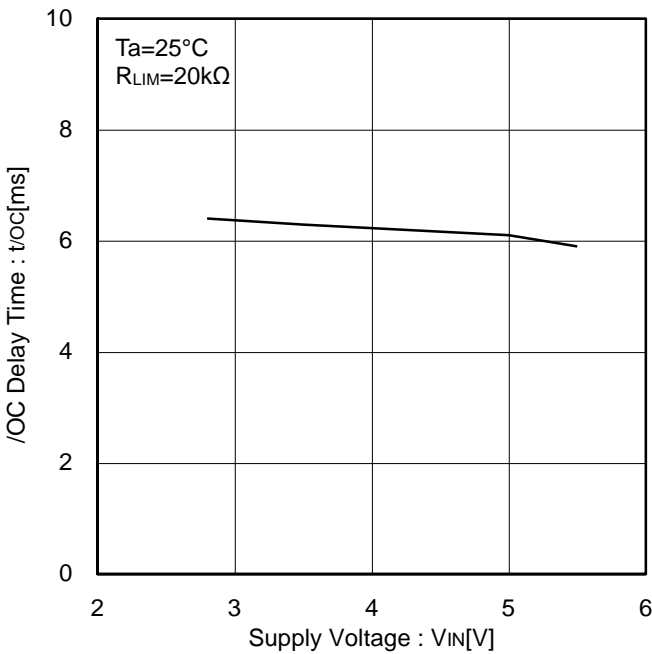


Figure 32. /OC Delay Time vs Supply Voltage

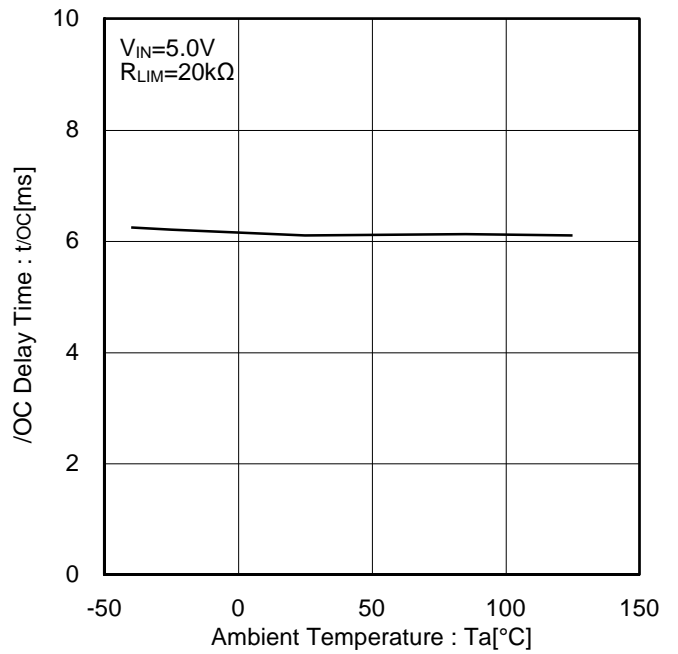


Figure 33. /OC Delay Time vs Ambient Temperature

Typical Performance Curves - continued

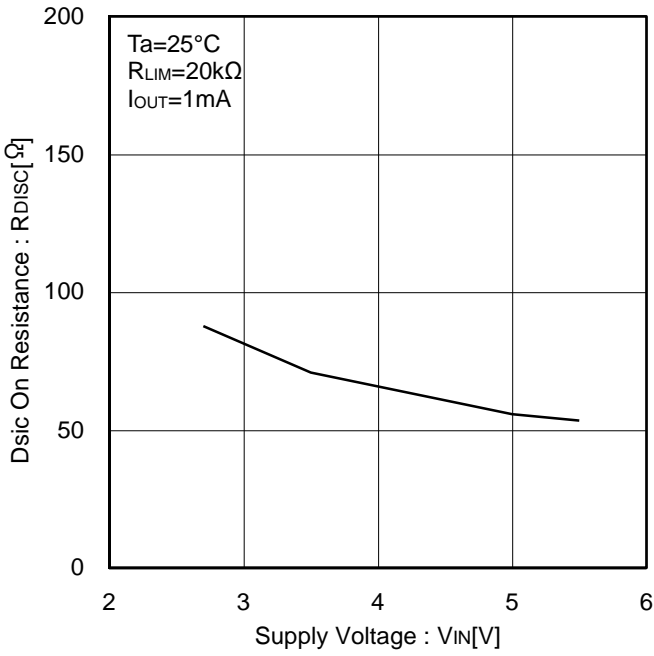


Figure 34. Discharge On Resistance vs Supply Voltage

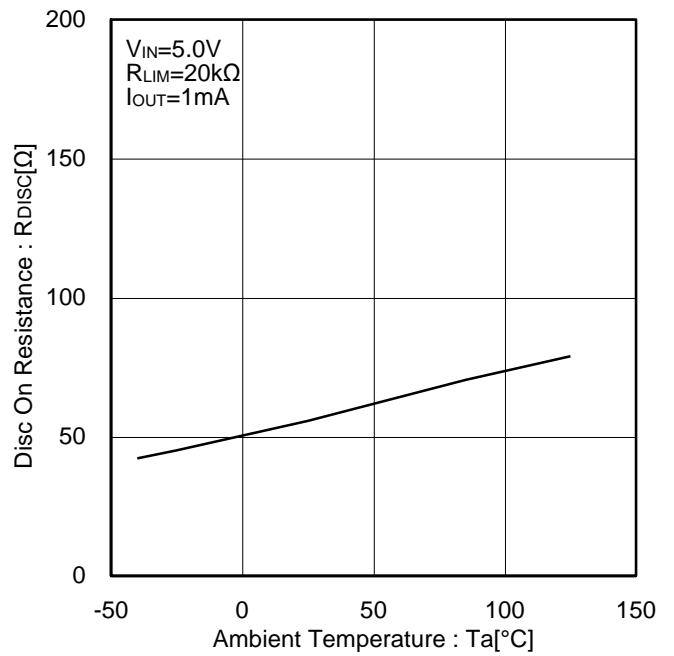
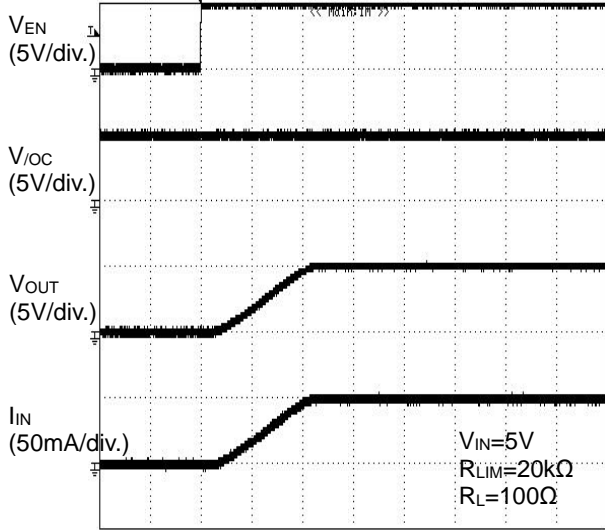
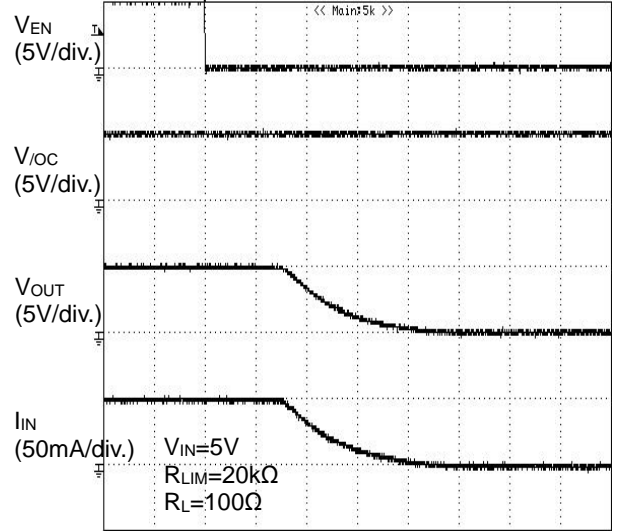


Figure 35. Discharge On Resistance vs Ambient Temperature

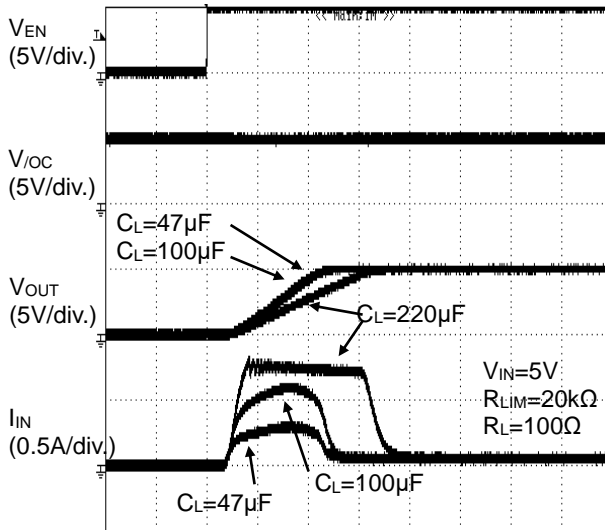
Typical Wave Forms



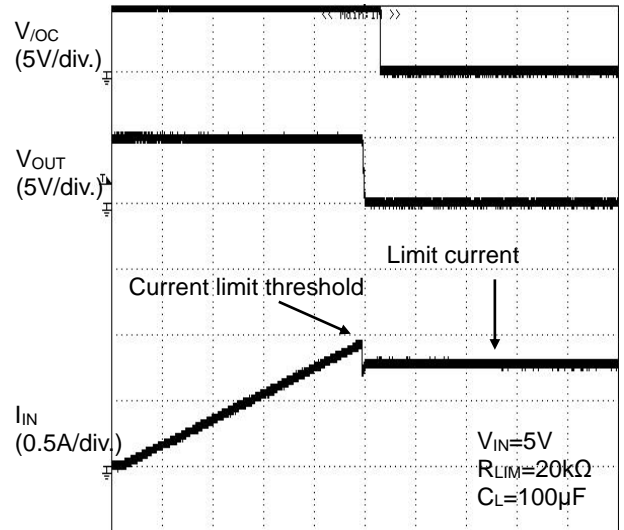
TIME (0.5ms/div.)
Figure 36. Output Rise Characteristic



TIME (1μs/div.)
Figure 37. Output Fall Characteristic

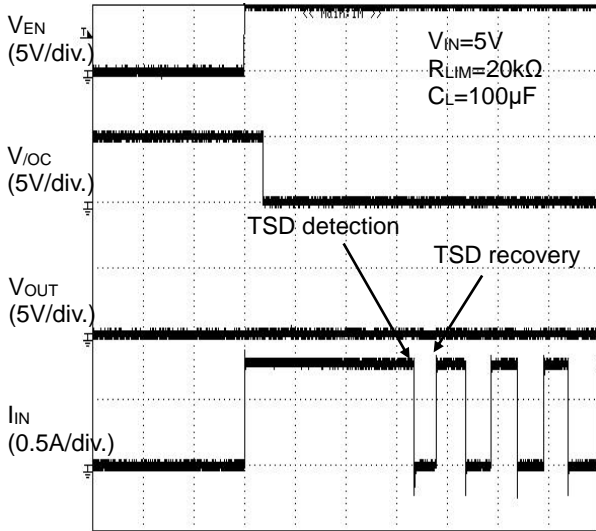


TIME (0.5ms/div.)
Figure 38. Inrush Current Response

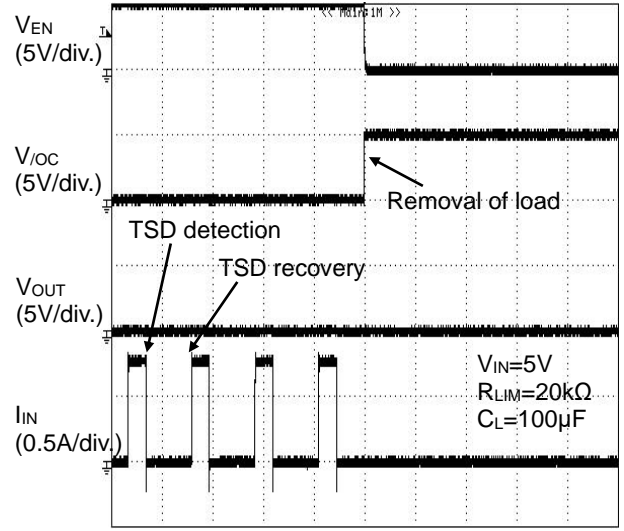


TIME (20ms/div.)
Figure 39. Over Current Response Ramped Load

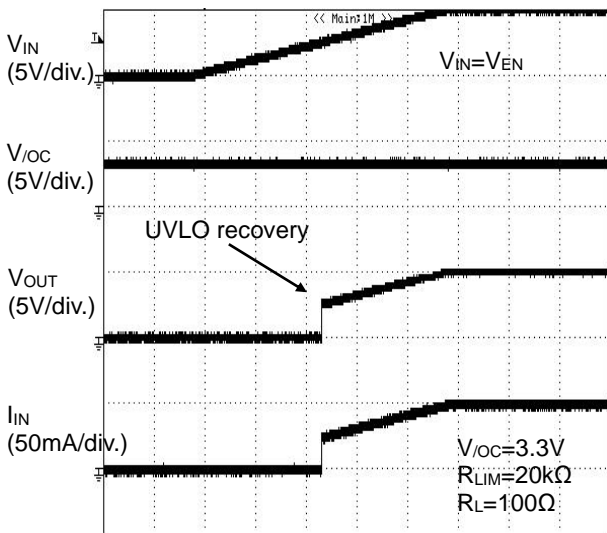
Typical Wave Forms - continued



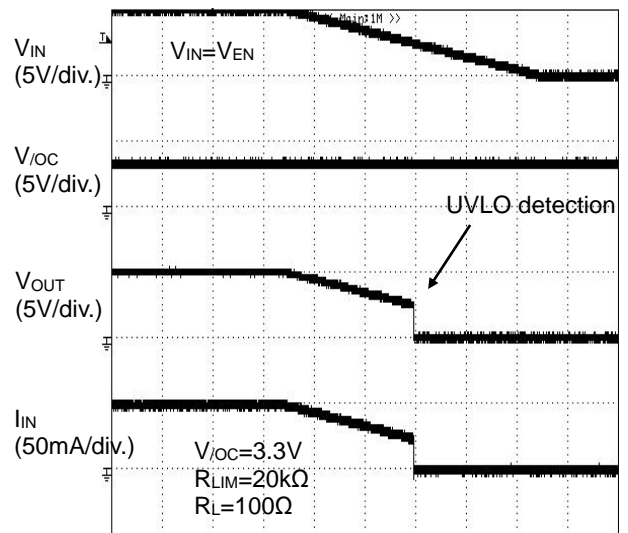
TIME (20ms/div.)
Figure 40. Over Current Response Enable Into Short Circuit



TIME (20ms/div.)
Figure 41. Over Current Response Disable From Short Circuit



TIME (1s/div.)
Figure 42. UVLO Response Increasing V_{IN}



TIME (1s/div.)
Figure 43. UVLO Response Decreasing V_{IN}

Typical Wave Forms – continued

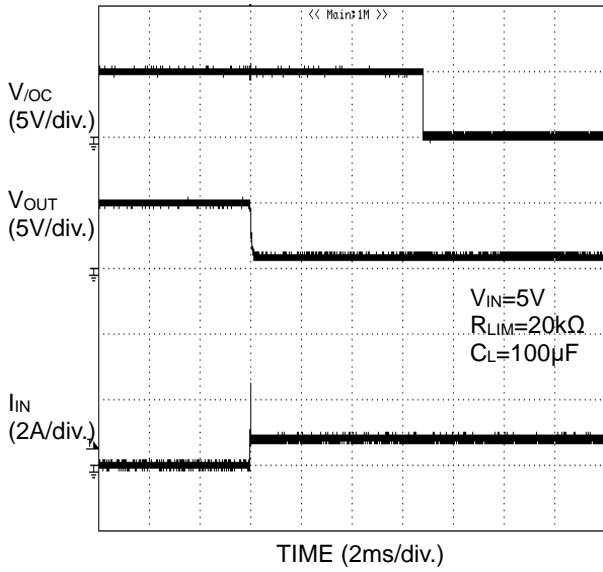


Figure 44. Over Current Response
1Ω Load Connected At Enable

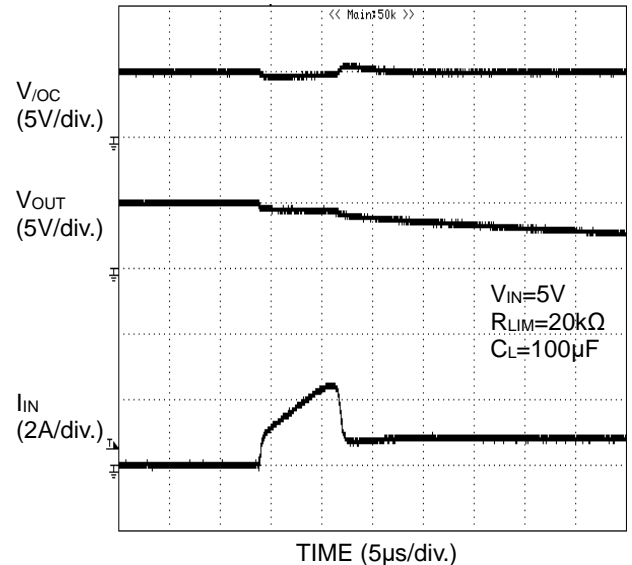


Figure 45. Over Current Response
1Ω Load Connected At Enable

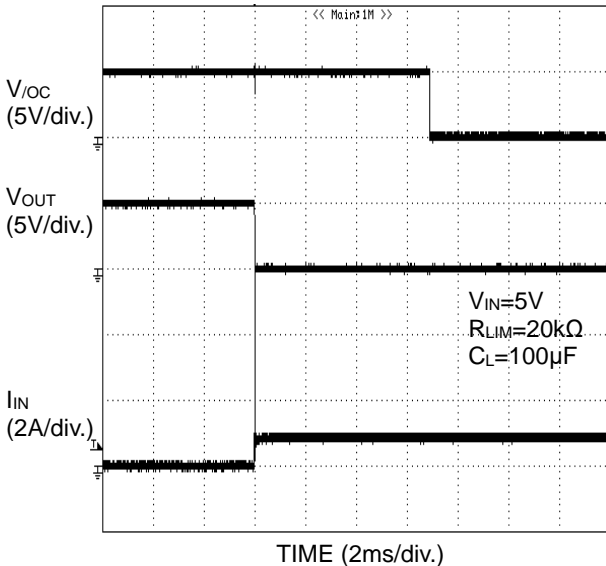


Figure 46. Over Current Response
0Ω Load Connected At Enable

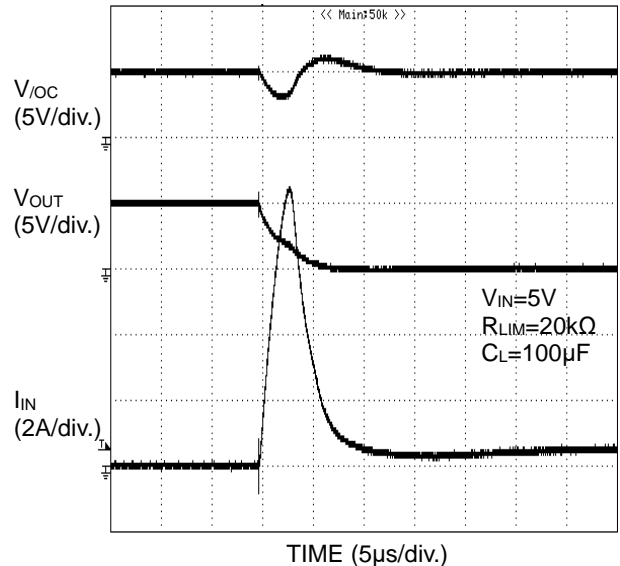


Figure 47. Over Current Response
0Ω Load Connected At Enable

Application Circuit Example

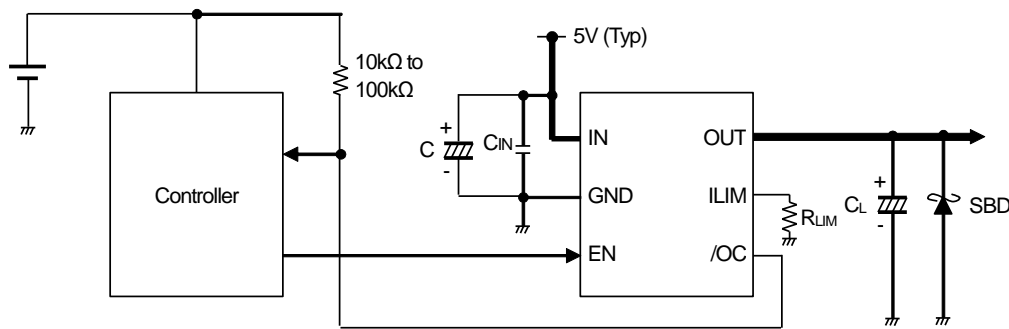


Figure 48. Application Circuit Example

Application Information

Ringing may cause bad influences on IC operations. In order to avoid this case, connect a low ESR bypass capacitor across IN terminal and GND terminal of IC. 1 μ F or higher is recommended. When excessive current flows due to output short-circuit or so, ringing occurs because of inductance between power source line to IC may exert a bad influence upon IC. In order to decrease voltage fluctuations from power source line to IC, connect a low ESR capacitor in parallel with C_{IN}. 10 μ F to 100 μ F or higher is effective.

When OUT terminal voltage is less than the absolute voltage (-0.3V), there is possibility that this IC suffers physical damage by parasitic diode. Recommended Voltage is over -0.3V. When OUT terminal and GND terminal short-circuit, undershoot occurs. To reduce undershoot level, recommendation is to put C_L and SBD near the OUT terminal. As pattern-layout and Application affect the undershoot level, make sure to leave an adequate margin.

Pull up /OC output via resistance value of 10k Ω to 100k Ω .

When using the circuit with changes to the external circuit constants, make sure to leave an adequate margin for external components including AC/DC characteristics as well as the dispersion of the IC.

Functional Description

1. Switch Operation

IN terminal and OUT terminal are connected to the drain and the source of switch MOSFET respectively. The IN terminal is also used as power source input to internal control circuit.

When the switch is turned on from EN control input, the IN and OUT terminals are connected by a 100m Ω (Typ) switch. In ON status, the switch is bidirectional. Therefore, when the potential of OUT terminal is higher than that of the IN terminal, current flows from OUT terminal to IN terminal.

Since a parasitic diode between the drain and the source of switch MOSFET is canceled, current flow from OUT to IN is prevented during off state.

2. Thermal Shutdown Circuit (TSD)

If over-current limit would continue, the temperature of the IC would increase drastically. If the junction temperature goes beyond 120 $^{\circ}$ C (Typ) in the condition of over-current detection, thermal shutdown circuit operates and turns power switch off, causing the IC to output a fault flag (/OC). Then, when the junction temperature decreases lower than 110 $^{\circ}$ C(Typ), the power switch is turned on and fault flag (/OC) is cancelled. Also, regardless of over-current condition, if the junction temperature were beyond 160 $^{\circ}$ C (Typ), thermal shutdown circuit makes power switch turn off and outputs fault flag (/OC). When junction temperature decreases lower than 140 $^{\circ}$ C (Typ), power switch is turned on and fault flag (/OC) is cancelled. This operation repeats, unless the increase of chip's temperature is removed or the output of power switch is turned OFF. Fault flag (/OC) is output without delay time at thermal shutdown.

The thermal shutdown circuit operates when the switch is ON (EN signal is active).

3. Over-Current Detection (OCD)

The over-current detection circuit limits current (I_{sc}) and outputs error flag (/OC) when current flowing in each switch MOSFET exceeds a specified value. The over-current detection circuit works when the switch is on (EN signal is active). There are three types of response against over-current.

(1) When the switch is turned on while the output is in short circuit status, the switch gets into current limit status immediately. (See figure 40.)

(2) When the output short-circuits or high capacity load is connected while the switch is on, very large current flows until the over-current limit circuit reacts. When the over-current detection and limit circuit operates, current limitation is carried out.(See figure 46,47.)

(3) When the output current increases gradually, current limitation would not operate unless the output current exceeds the over-current detection value. When it exceeds the over-current detection value, current limitation is carried out. (See Figure 39.)

4. Under-Voltage Lockout (UVLO)

UVLO circuit prevents the switch from turning on until the V_{IN} exceeds 2.55V(Typ). If the V_{IN} drops below 2.5V(Typ) while the switch turns on, then UVLO shuts off the power switch. UVLO has hysteresis of 50mV(Typ). Under-voltage lockout circuit operates when the switch is on (EN signal is active). (see Figure 42,43.)

5. Fault Flag (/OC) Output

Fault flag output is an N-MOS open drain output. At detection of over-current or thermal shutdown, output is low-level. Over-current detection has delay filter. This delay filter prevents instantaneous current detection such as inrush current at switch on, hot plug from being informed to outside, but if charge up time for output capacitance is longer than delay time, fault flag output asserts low level. When output current is close to Current Limit Threshold value, fault flag output (/OC) might be low level before turning to over-current condition because it is affected by current swinging or noise. If fault flag(/OC) output is unused, /OC pin should be connected to open or ground line.

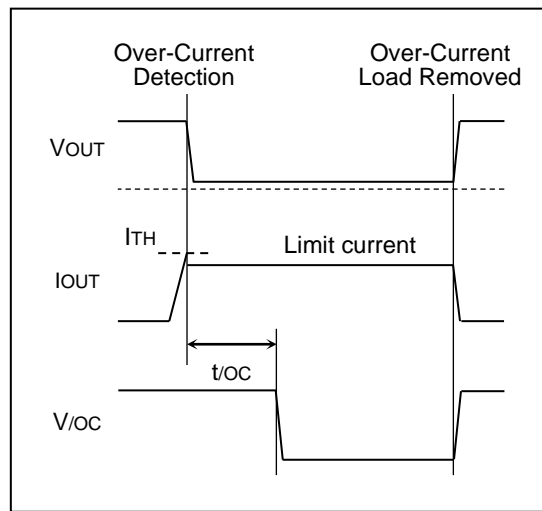


Figure 49. Over-Current Detection

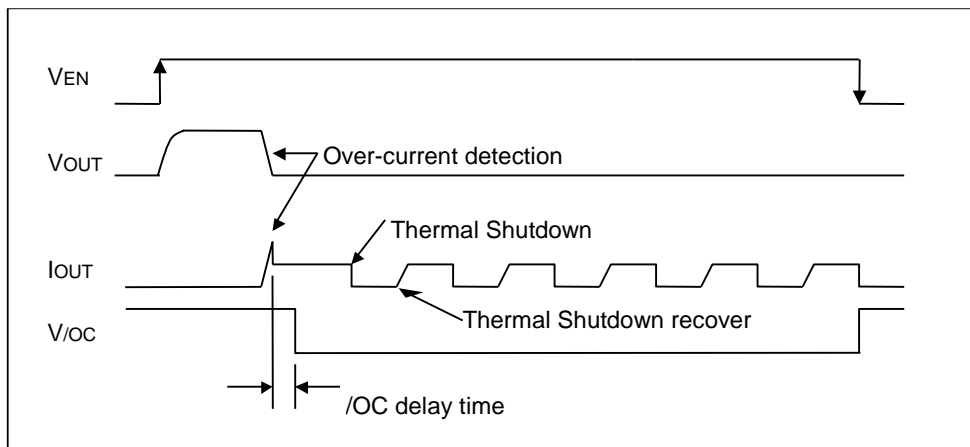


Figure 50. Over-Current Detection, Thermal Shutdown Timing

6. Adjustable Current Limit Threshold

BD22441G-C is able to change over-current detection value from 0.2A(Typ) to 1.7A(Typ) by connecting resistance (R_{LIM}) between ILIM pin and GND pin. The resistance value from 11.97k Ω to 106.3k Ω is recommended for R_{LIM} . The relational expression and the table for resistance value and over-current detection value are described below. Allocate R_{LIM} close to IC as possible. Be careful not to be affected by parasitic resistance of board pattern because over-current detection value is depended on the resistance value between ILIM pin and GND pin. ILIM pin cannot be used as open and short to GND pin. The R_{LIM} resistance tolerance directly affects the current limit threshold accuracy. Recommended to use low tolerance resistance.

Over Current Threshold Equation,

$$I_{TH}(Typ)[mA] = 19364 \times R_{LIM}[k\Omega]^{-0.98}$$

$$I_{TH}(Min)[mA] = 17500 \times R_{LIM}[k\Omega]^{-1} - 53$$

$$I_{TH}(Max)[mA] = 22600 \times R_{LIM}[k\Omega]^{-1} + 104$$

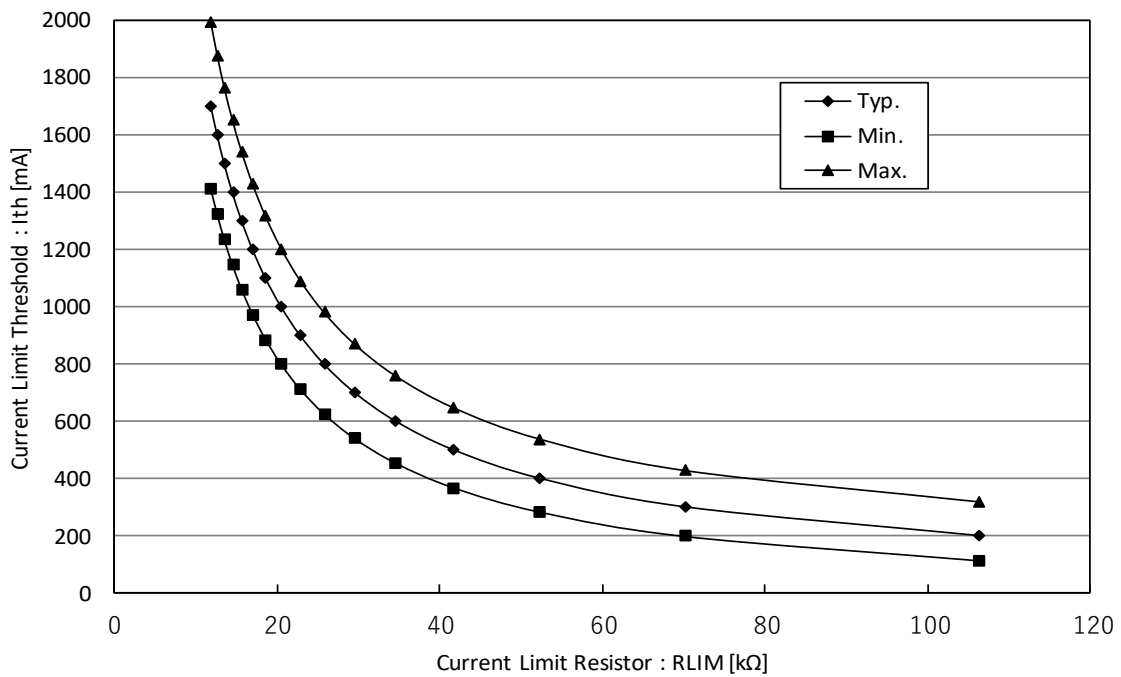


Figure 51. I_{TH} vs. R_{LIM}

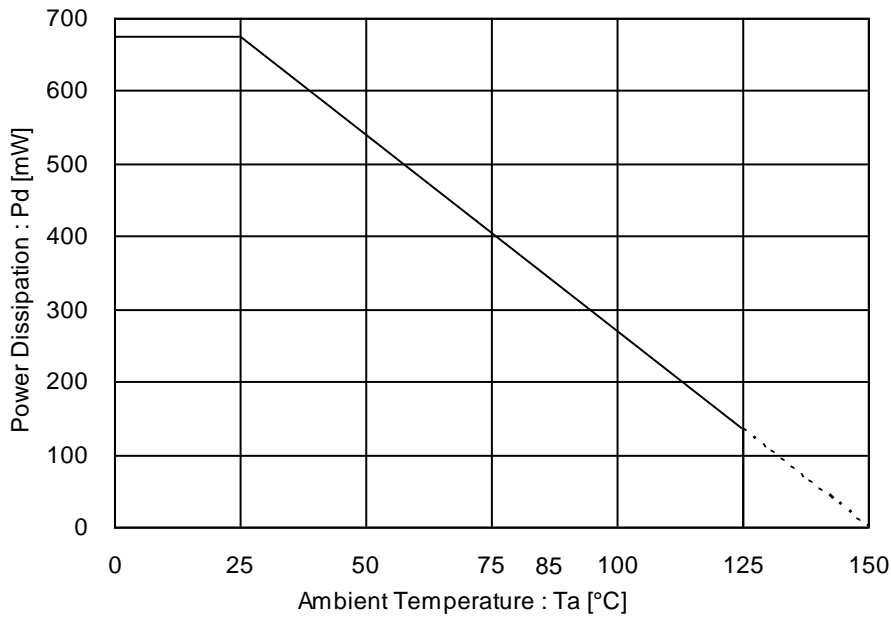
R _{LIM} (kΩ)	Current Limit Threshold (mA)		
	MIN	TYP	MAX
106.30	111.7	200	316.6
70.28	196.0	300	425.5
52.40	281.0	400	535.2
41.73	366.4	500	645.5
34.65	452.1	600	756.2
29.60	538.2	700	867.4
25.83	624.5	800	978.8
22.91	711.0	900	1090.5
20.57	797.7	1000	1202.5
18.67	884.6	1100	1314.7
17.08	971.6	1200	1427.1
15.74	1058.8	1300	1539.8
14.59	1146.2	1400	1652.5
13.60	1233.6	1500	1765.5
12.73	1321.2	1600	1878.6
11.97	1408.9	1700	1991.9

Table 1. I_{TH} Tolerance vs. R_{LIM}

7. Output Discharge Function

When the switch is turned off from disable control input or UVLO function, the 60Ω(Typ) output discharge circuit between OUT and GND turns on. By turning on this switch, electric charge at capacitive load is discharged. But when the voltage of IN declines extremely, then the OUT pin becomes high impedance without UVLO function.

Power Dissipation
(SSOP6 package)



* 70mm x 70mm x 1.6mm Glass Epoxy Board
Figure 52. Power Dissipation Curve (Pd-Ta Curve)

I/O Equivalence Circuit

Symbol	Pin No.	Equivalent Circuit
EN	3	
/OC	4	
ILIM	5	
OUT	6	

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin A$ and $GND > Pin B$, the P-N junction operates as a parasitic diode.

When $GND > Pin B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

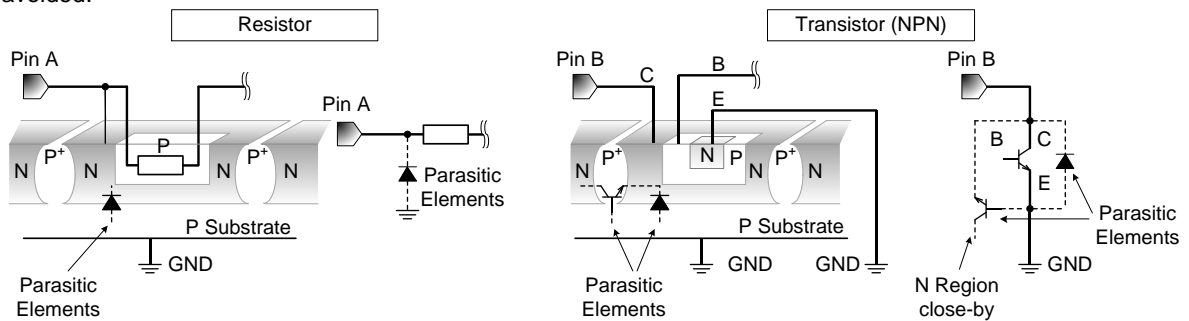


Figure 52. Example of monolithic IC structure

13. Ceramic Capacitor

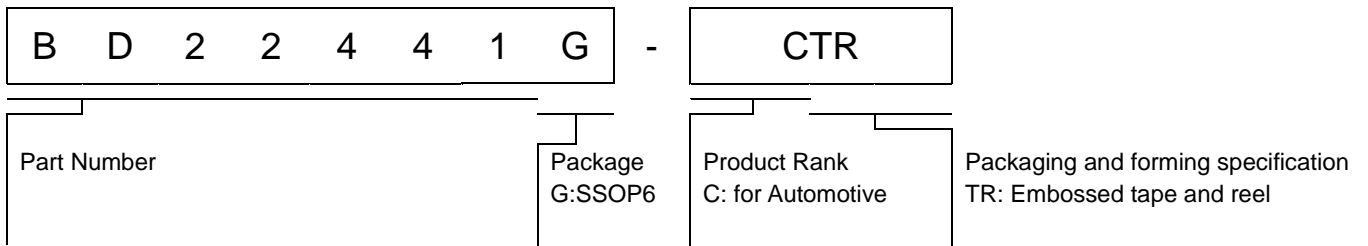
When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Thermal Shutdown Circuit(TSD)

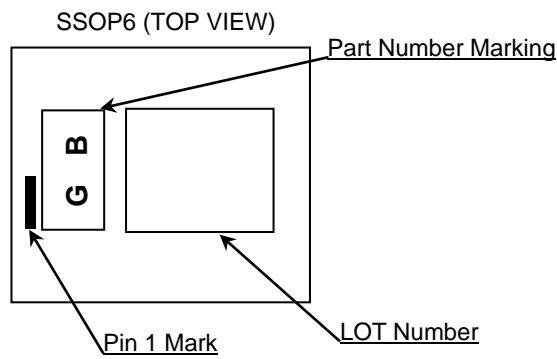
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF power output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

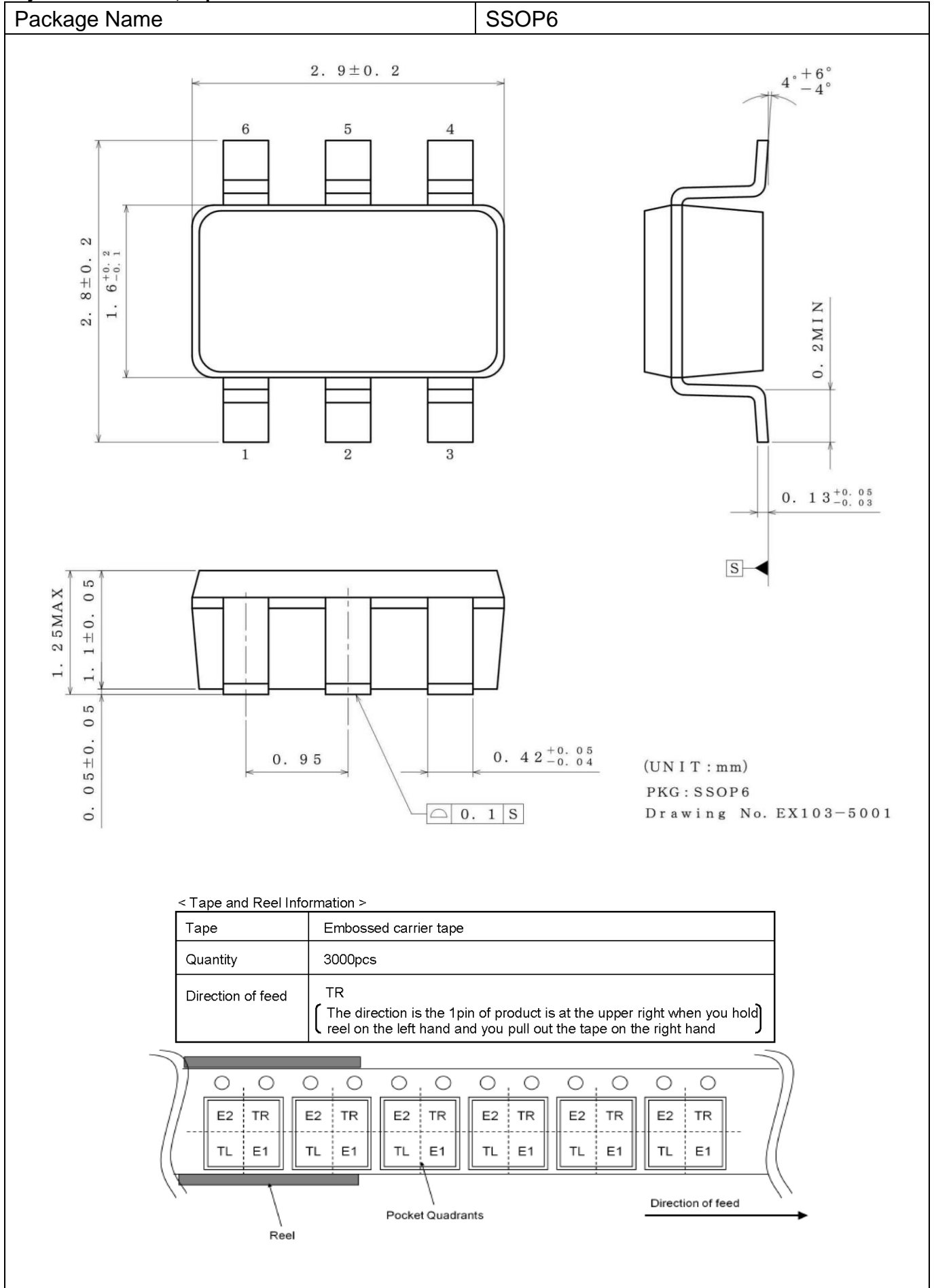
Ordering Information



Marking Diagram



Physical Dimension, Tape and Reel Information



Revision History

Date	Revision	Changes
26.Jun.2020	001	New Release
26.Oct.2020	002	Change CGTR to CTR at Page 23 Packaging and forming specification.
21.Jun.2021	003	Change Max limit for Output Turn-On Time 10ms to 3ms at Page 3.
11.Apr.2022	004	Change Max limit for Output Rise Time 6ms to 1.8ms at Page 3.
02.Apr.2024	005	Change Min limit for EN Input Voltage 2.7V to 2.3V at Page 3.

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - [f] Sealing or coating our Products with resin or other coating materials
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 - [h] Use of the Products in places subject to dew condensation
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8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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 - [d] the Products are exposed to high Electrostatic
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3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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