

1.5A STEP DOWN SWITCHING REGULATOR

1 FEATURES

- UP TO 1.5A STEP DOWN CONVERTER
- OPERATING INPUT VOLTAGE FROM 8V TO 55V
- PRECISE 3.3V ($\pm 1\%$) INTERNAL REFERENCE VOLTAGE
- OUTPUT VOLTAGE ADJUSTABLE FROM 3.3V TO 50V
- SWITCHING FREQUENCY ADJUSTABLE UP TO 300KHz
- VOLTAGE FEEDFORWARD
- ZERO LOAD CURRENT OPERATION
- INTERNAL CURRENT LIMITING (PULSE-BYPULSE AND HICCUP MODE)
- INHIBIT FOR ZERO CURRENT CONSUMPTION
- PROTECTION AGAINST FEEDBACK DISCONNECTION
- THERMAL SHUTDOWN
- SOFT START FUNCTION

2 DESCRIPTION

The L4971 is a step down monolithic power switching regulator delivering 1.5A at a voltage between 3.3V and 50V (selected by a simple external divider). Realized in BCD mixed technology, the device uses an internal power D-MOS transistor (with a typical R_{dson} of 0.25Ω) to obtain very high efficiency and high switching speed.

Figure 1. Package



Table 1. Order Codes

Part Number	Package
L4971	DIP8
L4971D	SO16W
L4971D013TR	SO16 in Tape & Reel

A switching frequency up to 300KHz is achievable (the maximum power dissipation of the packages must be observed).

A wide input voltage range between 8V to 55V and output voltages regulated from 3.3V to 50V cover the majority of today's applications.

Features of this new generations of DC-DC converter include pulse-by-pulse current limit, hiccup mode for short circuit protection, voltage feedforward regulation, soft-start, protection against feedback loop disconnection, inhibit for zero current consumption and thermal shutdown.

The device is available in plastic dual in line, DIP8 for standard assembly, and SO16W for SMD assembly.

Figure 1. Block Diagram

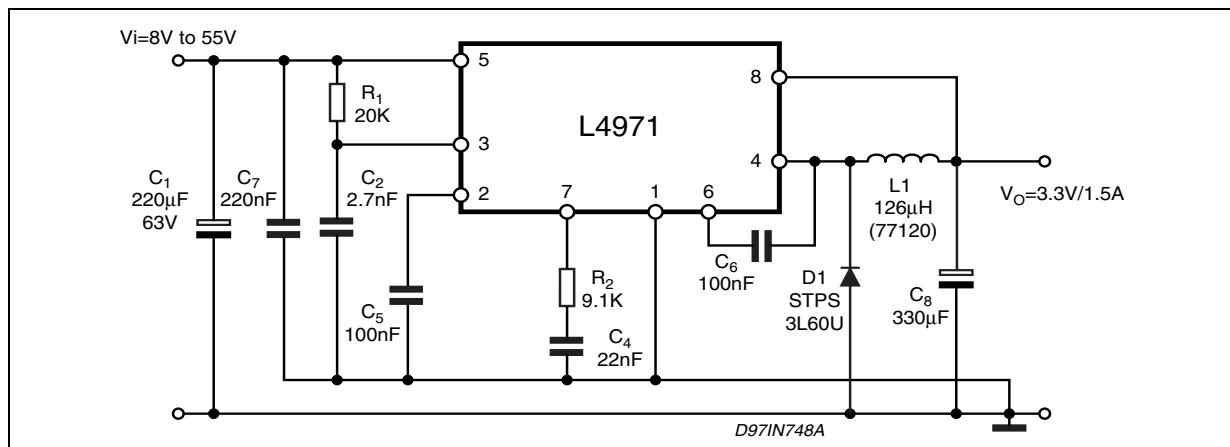


Table 3. Absolute Maximum Ratings

Symbol		Parameter	Value	Unit	
Minidip	S016				
V ₅	V ₁₁	Input voltage	58	V	
V ₄	V ₅ , V ₆	Output DC voltage	-1	V	
		Output peak voltage at t = 0.1 μs f=200KHz	-5	V	
I ₄	I ₅ , I ₆	Maximum output current	int. limit.		
V ₆ -V ₅	V ₁₂ -V ₁₁		14	V	
V ₆	V ₁₂	Bootstrap voltage	70	V	
V ₇	V ₁₃	Analog input voltage (V _{CC} = 24V)	12	V	
V ₂	V ₃	Analog input voltage (V _{CC} = 24V)	13	V	
V ₈	V ₁₄	(V _{CC} = 20V)	6	V	
			-0.3	V	
P _{tot}		Power dissipation a Tamb ≤60°C	DIP8	1	W
			SO16	0.8	W
T _j , T _{stg}		Junction and storage temperature	-40 to 150	°C	

Table 4. Thermal Data

Symbol	Parameter		DIP8	SO16	Unit
R _{th(j-amb)}	Thermal Resistance Junction to ambient	Max.	90 (*)	110 (*)	°C/W

(*) Package mounted on board.

3 ELECTRICAL CHARACTERISTICS

Table 5. (T_j = 25°C, C_{osc} = 2.7nF, R_{osc} = 20kΩ, V_{CC} = 24V, unless otherwise specified.)* Specification Referred to T_j from 0 to 125°C

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTIC							
V _i	Operating input voltage range	V _o = 3.3 to 50V; I _o = 1.5A	*	8		55	V
V _o	Output voltage	I _o = 0.5A		3.33	3.36	3.39	V
		I _o = 0.2 to 1.5A		3.292	3.36	3.427	V
		V _{CC} = 8 to 55V	*	3.22	3.36	3.5	V
V _d	Dropout voltage	V _{CC} = 10V; I _o = 1.5A			0.44	0.55	V
			*			0.88	V
I _l	Maximum limiting current Efficiency	V _{CC} = 8 to 55V	*	2	2.5	3	A
		V _o = 3.3V; I _o = 1.5A			85		%
f _s	Switching frequency		*	90	100	110	KHz
SVRR	Supply voltage ripple rejection	V _i = V _{CC} +2V _{RMS} ; V _o = V _{ref} ; I _o = 1.5A; f _{ripple} = 100Hz		60			dB
	Voltage stability of switching frequency	V _{CC} = 8 to 55V			3	6	%
	Temp. stability of switching frequency	T _j = 0 to 125°C			4		%

Table 5. ($T_j = 25^\circ\text{C}$, $C_{osc} = 2.7\text{nF}$, $R_{osc} = 20\text{k}\Omega$, $V_{CC} = 24\text{V}$, unless otherwise specified.)* Specification Referred to T_j from 0 to 125°C

Soft Start							
	Soft start charge current			30	40	50	μA
	Soft start discharge current			6	10	14	μA
Inhibit							
V_{LL}	Low level voltage		*			0.9	V
I_{sLL}	Isorce Low level		*		5	15	μA
DC Characteristics							
I_{qop}	Total operating quiescent current				4	6	mA
I_q	Quiescent current	Duty Cycle = 0; $V_{FB} = 3.8\text{V}$			2.5	3.5	mA
I_{qst-by}	Total stand-by quiescent current	$V_{inh} < 0.9\text{V}$			100	200	μA
		$V_{cc} = 55\text{V}; V_{inh} < 0.9\text{V}$			150	300	μA
Error Amplifier							
V_{FB}	Voltage Feedback Input			3.33	3.36	3.39	V
R_L	Line regulation	$V_{cc} = 8$ to 55V			5	10	mV
	Ref. voltage stability vs temperature		*		0.4		mV/ $^\circ\text{C}$
V_{oH}	High level output voltage	$V_{FB} = 2.5\text{V}$		10.3			V
V_{oL}	Low level output voltage	$V_{FB} = 3.8\text{V}$				0.65	V
$I_{o\ source}$	Source output current	$V_{comp} = 6\text{V}; V_{FB} = 2.5\text{V}$		200	300		μA
$I_{o\ sink}$	Sink output current	$V_{comp} = 6\text{V}; V_{FB} = 3.8\text{V}$		200	300		μA
I_b	Source bias current				2	3	μA
SVRR E/A	Supply voltage ripple rejection	$V_{comp} = V_{fb}; V_{cc} = 8$ to 55V		60	80		dB
	DC open loop gain	$R_L = \infty$		50	57		dB
gm	Transconductance	$I_{comp} = -0.1$ to 0.1mA $V_{comp} = 6\text{V}$			2.5		ms
Oscillator Section							
	Ramp Valley			0.78	0.85	0.92	V
	Ramp peak	$V_{cc} = 8\text{V}$		2	2.15	2.3	V
		$V_{cc} = 55\text{V}$		9	9.6	10.2	V
	Maximum duty cycle			95	97		%
	Maximum Frequency	Duty Cycle = 0% ; $R_{osc} = 13\text{k}\Omega, C_{osc} = 820\text{pF}$				300	kHz

Table 6. Typical Performance (Using Evaluation Board) fsw = 100kHz

Output Voltage	Output Ripple	Efficiency $V_{CC}=35V$ $I_O = 1.5A$	Line Regulation $I_o = 1.5A$ $V_{CC} = 8$ to $55V$	Load Regulation $V_{CC}=35V$ $I_O = 0.5$ to $1.5A$
3.3V	10mV	84 (%)	3mV	6mV
5.1V	10mV	86 (%)	3mV	6mV
12V	12mV	93 (%)	3mV ($V_{CC} = 15$ to $55V$)	4mV

Figure 4. Test and valuation board circuit.

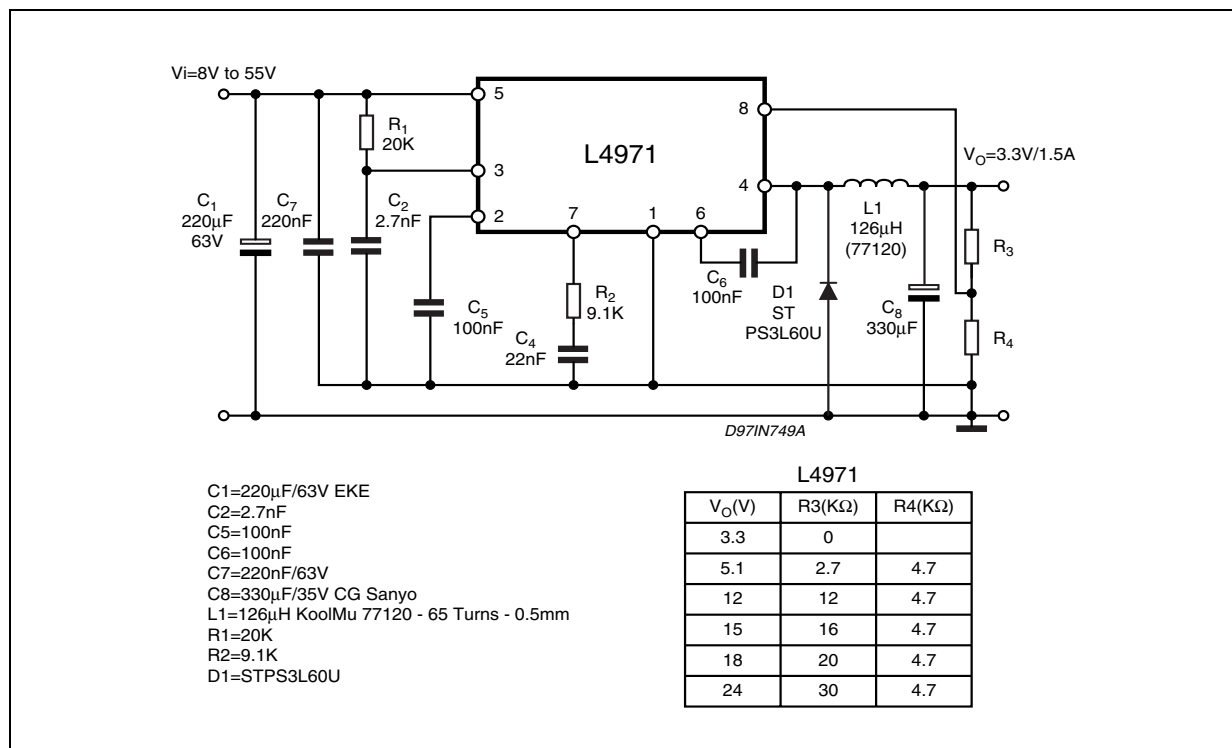


Figure 5. PCB and component layout of the figure 4.

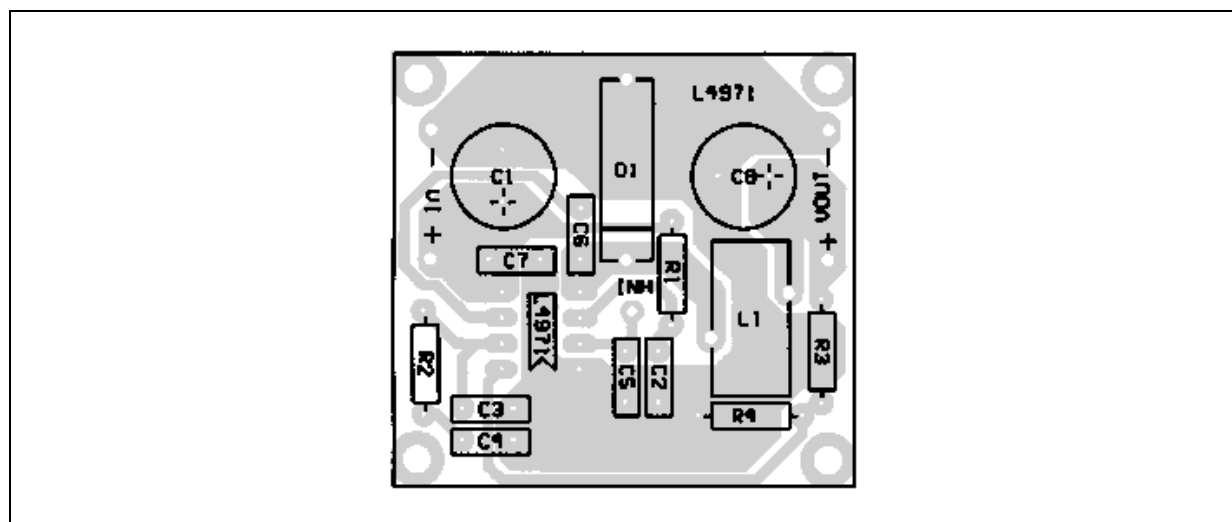


Figure 6. Quiescent drain current vs. input voltage.

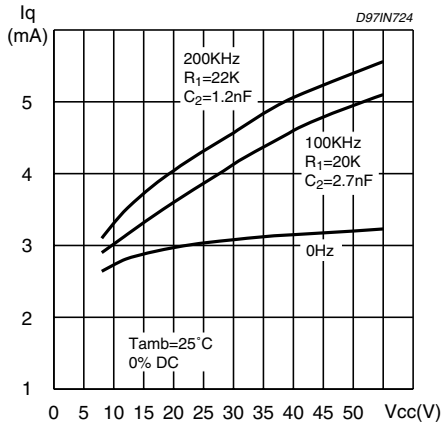


Figure 9. Line Regulation

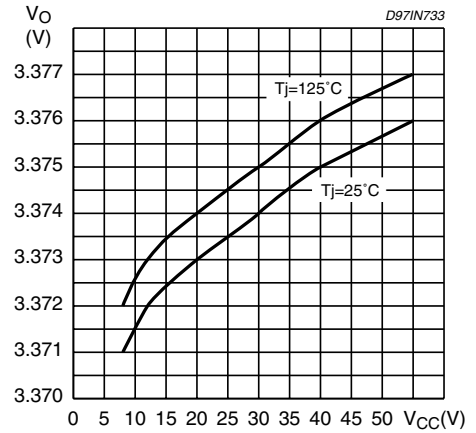


Figure 7. Quiescent current vs. junction temperature

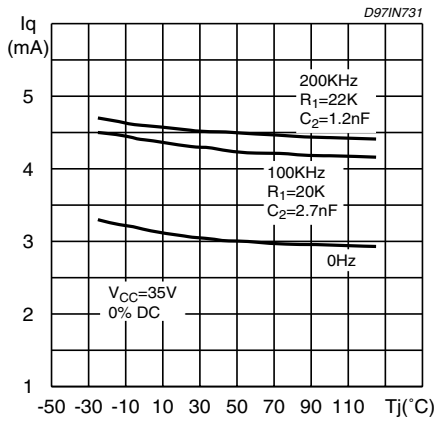


Figure 10. Line Regulation

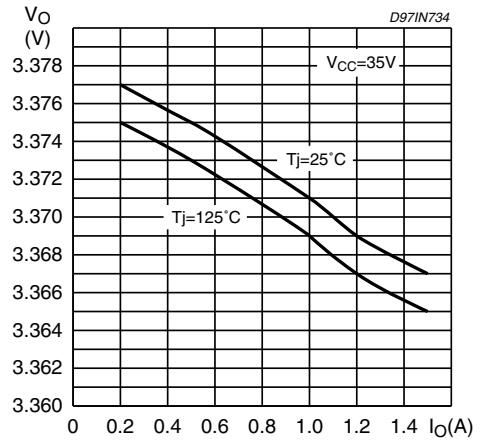


Figure 8. Stand-by drain current vs. input voltage

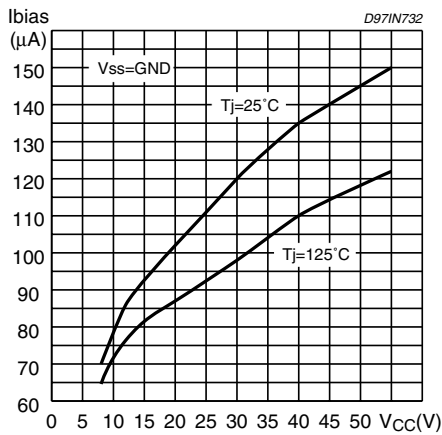


Figure 11. Switching frequency vs. R1 and C2

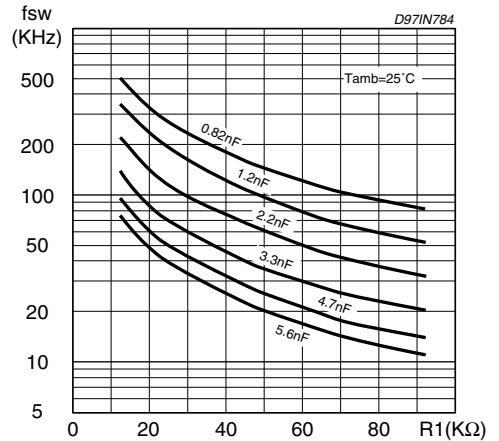


Figure 12. Switching Frequency vs. input voltage.

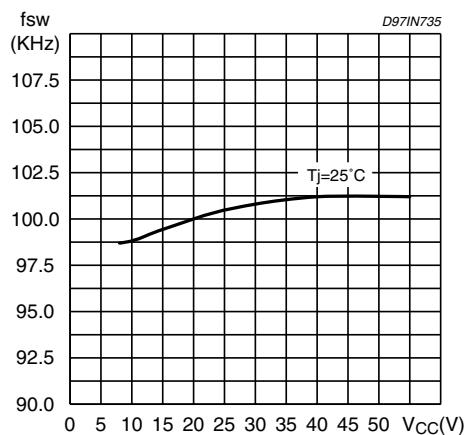


Figure 15. Efficiency vs output voltage.

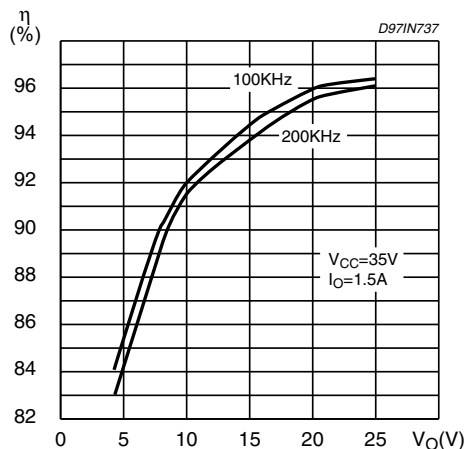


Figure 13. Switching frequency vs. junction temperature.

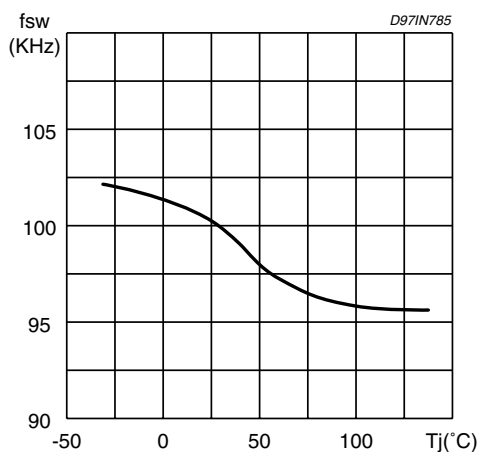


Figure 16. Efficiency vs. output current.

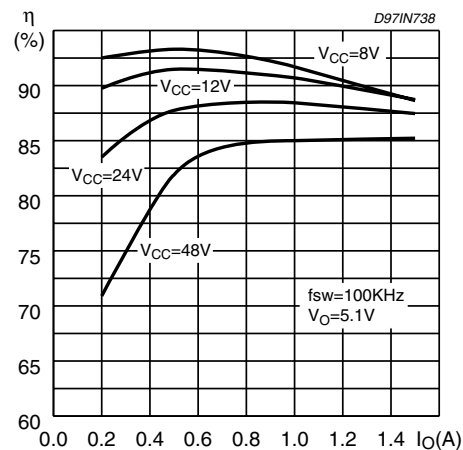


Figure 14. Dropout voltage between pin 5 and 4

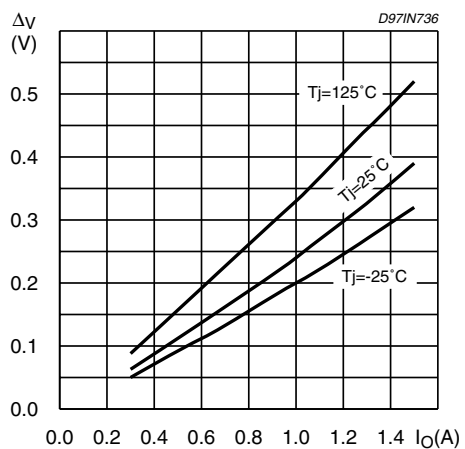


Figure 17. Efficiency vs. output current.

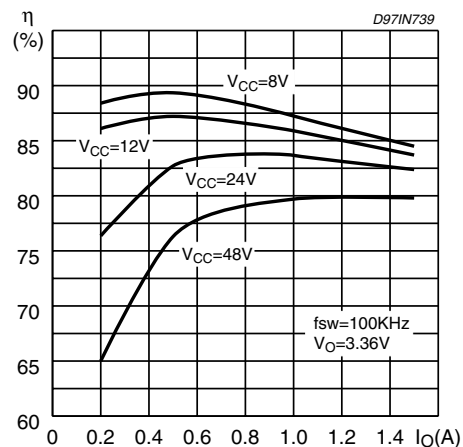


Figure 18. Efficiency vs. output current.

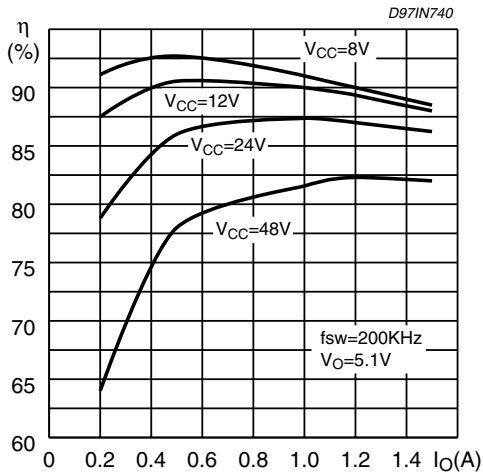


Figure 21. Power dissipation vs. V_{CC}.

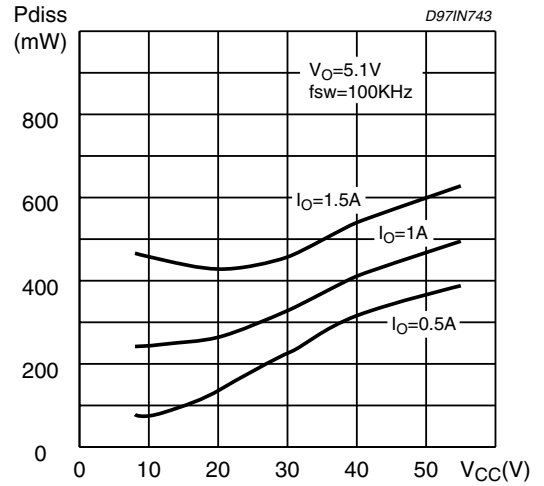


Figure 19. Efficiency vs. output current.

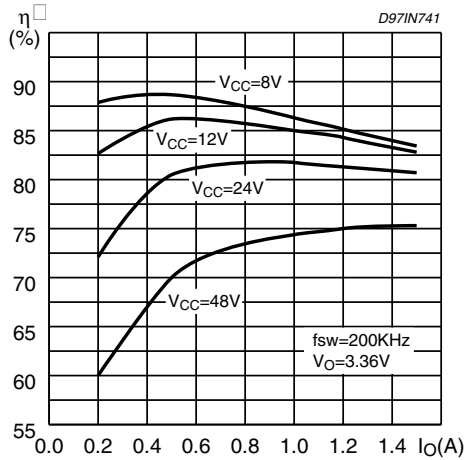


Figure 22. Efficiency vs. V_O

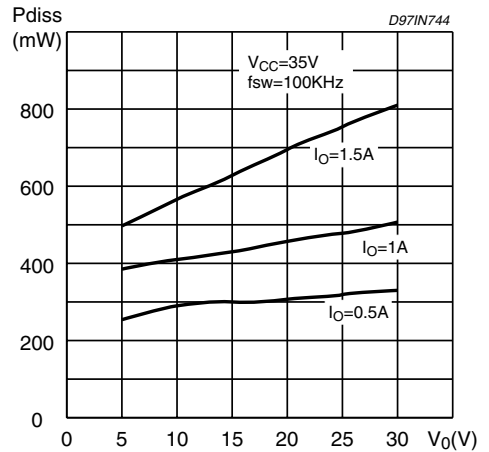


Figure 20. Efficiency vs. V_{CC}.

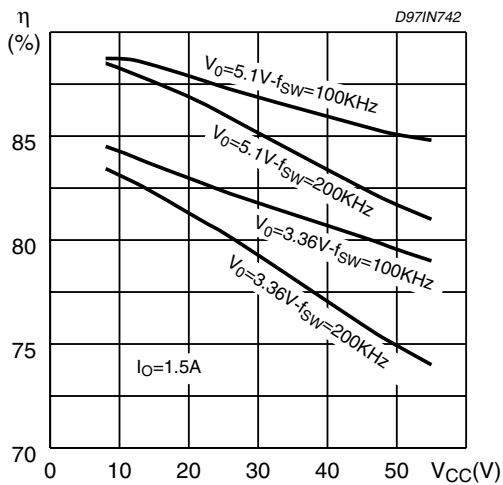


Figure 23. Pulse by pulse limiting current vs. junction temperature.

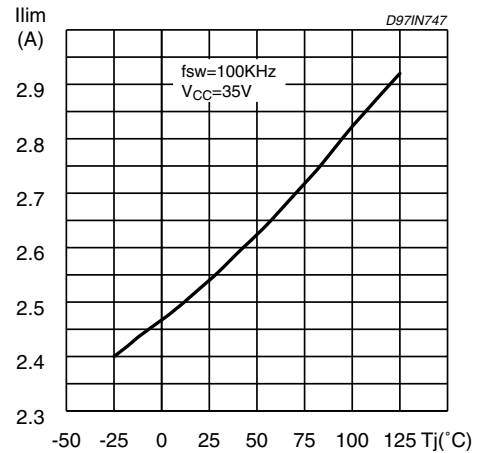


Figure 24. Load transient.

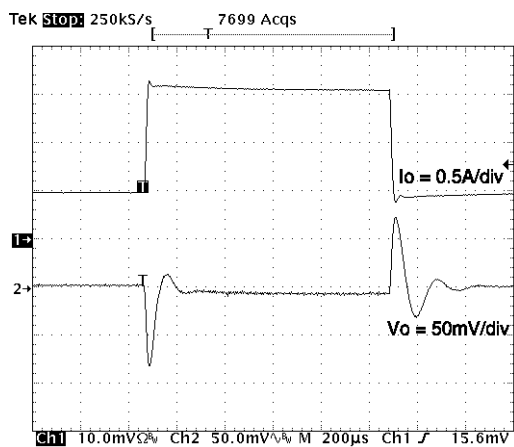


Figure 27. Soft start capacitor selection vs. Inductor and Vccmax

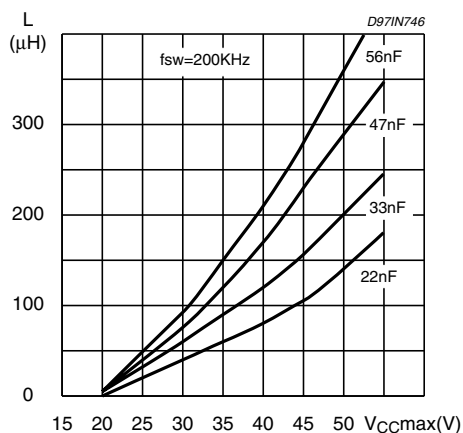


Figure 25. Line transient.

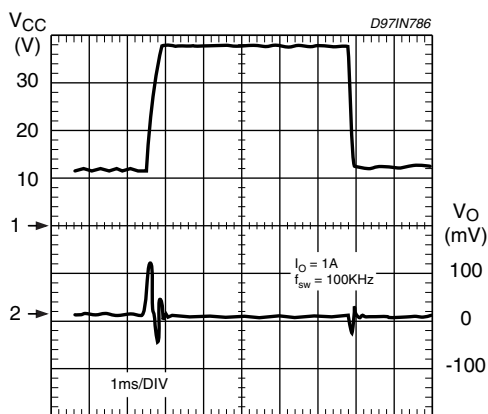


Figure 28. Open loop frequency and phase of error amplifier

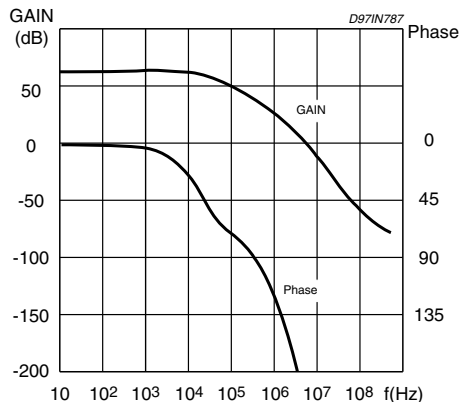


Figure 26. Soft start capacitor selection Vs inductor and Vccmax.

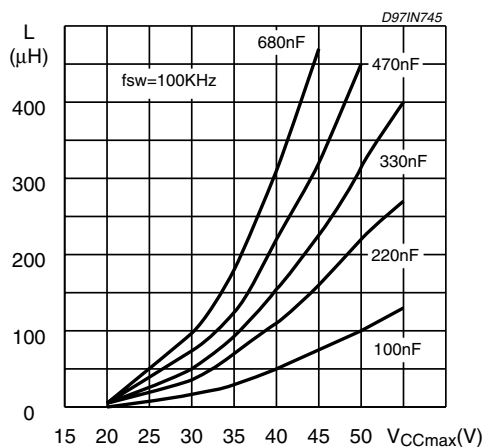
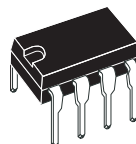


Figure 29. DIP8 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

OUTLINE AND MECHANICAL DATA



DIP-8

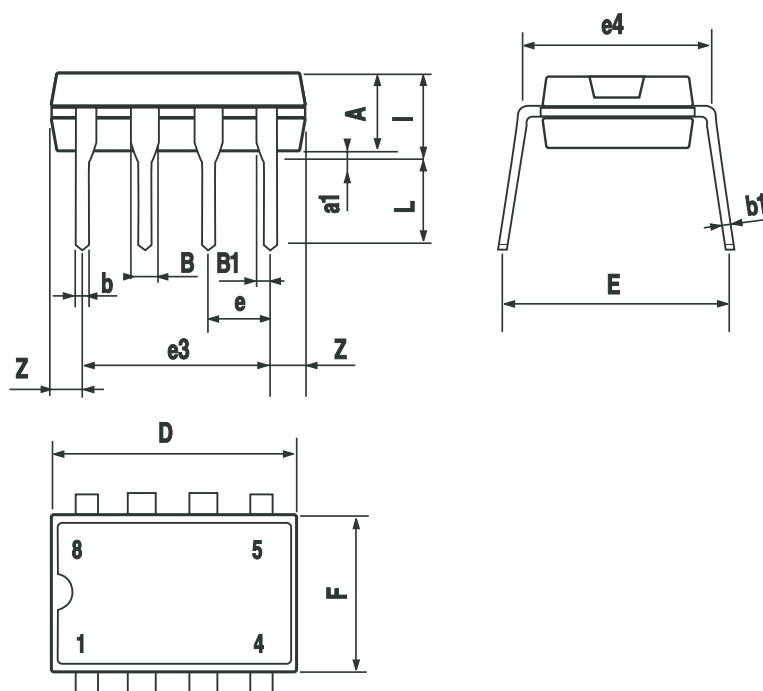
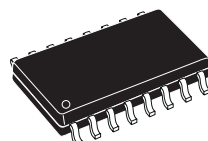


Figure 30. SO16 Mechanical Data & Package Dimensions

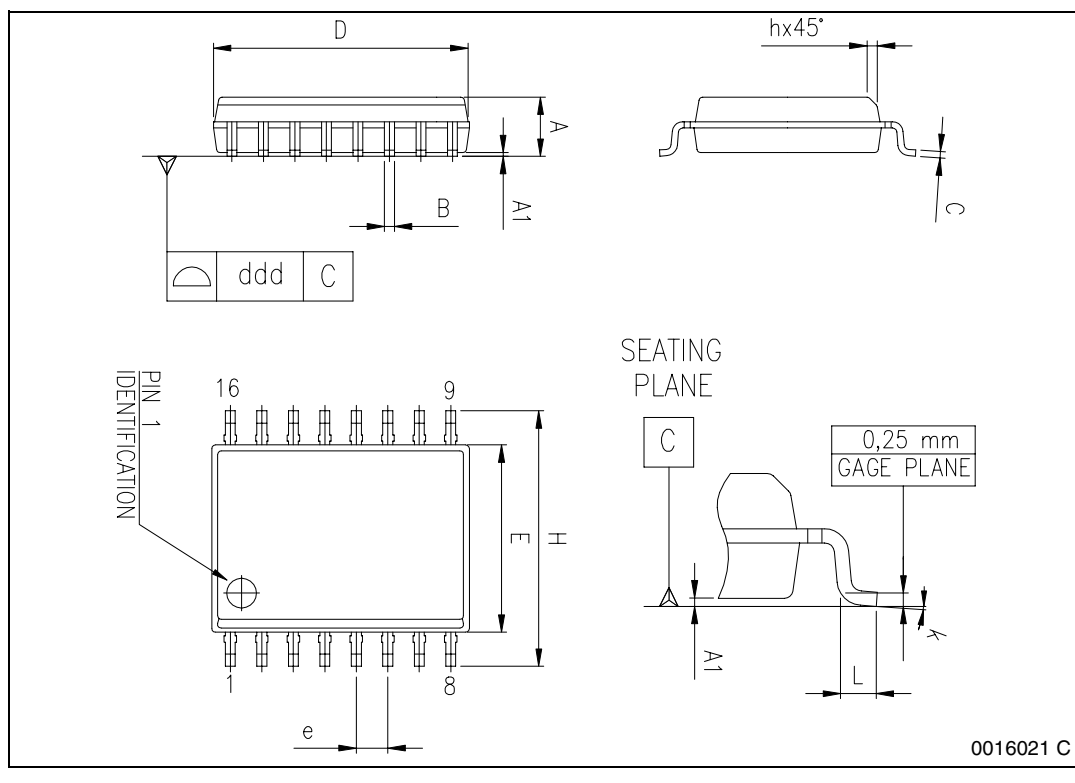
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D ⁽¹⁾	10.10		10.50	0.398		0.413
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA



SO16 (Wide)



4 REVISION HISTORY

Table 7. Revision History

Date	Revision	Description of Changes
October 2004	10	First Issue in EDOCS
May 2005	11	Updated the Layout look & feel. Changed name of the D1 on the figs. 1 and 4.

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