

74LVC1G07

Buffer with open-drain output

Rev. 16 — 3 February 2022

Product data sheet

1. General description

The 74LVC1G07 is a single buffer with open-drain output. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments. Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times. This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- CMOS low power consumption
- I_{OFF} circuitry provides partial Power-down mode operation
- -24 mA output drive ($V_{CC} = 3.0$ V)
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Complies with JEDEC standard:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8C (2.7 V to 3.6 V)
 - JESD36 (4.5 V to 5.5 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2000 V
 - MM: JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC1G07GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74LVC1G07GV	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753
74LVC1G07GM	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
74LVC1G07GN	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 0.9 × 1.0 × 0.35 mm	SOT1115
74LVC1G07GS	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm	SOT1202
74LVC1G07GX	-40 °C to +125 °C	X2SON5	plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 × 0.8 × 0.32 mm	SOT1226-3
74LVC1G07GX4	-40 °C to +125 °C	X2SON4	plastic thermal enhanced extremely thin small outline package; no leads; 4 terminals; body 0.6 × 0.6 × 0.32 mm	SOT1269-2

4. Marking

Table 2. Marking

Type number	Marking code ^[1]
74LVC1G07GW	VS
74LVC1G07GV	V07
74LVC1G07GM	VS
74LVC1G07GN	VS
74LVC1G07GS	VS
74LVC1G07GX	VS
74LVC1G07GX4	VS

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

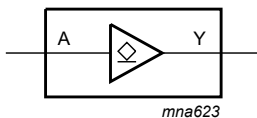


Fig. 1. Logic symbol



Fig. 2. IEC logic symbol

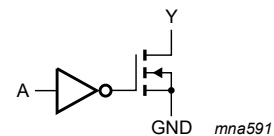


Fig. 3. Logic diagram

6. Pinning information

6.1. Pinning

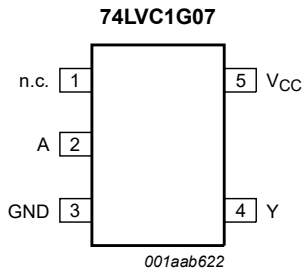


Fig. 4. Pin configuration SOT353-1 (TSSOP5) and SOT753 (SC-74A)

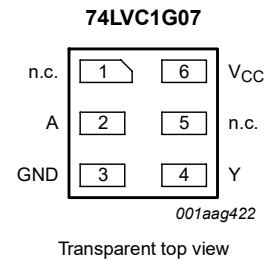


Fig. 5. Pin configuration SOT886, SOT1115 and SOT1202 (XSON6)

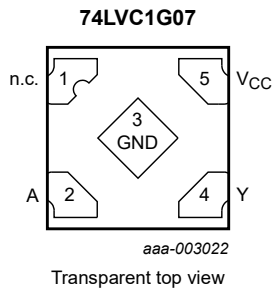


Fig. 6. Pin configuration SOT1226-3 (X2SON5)

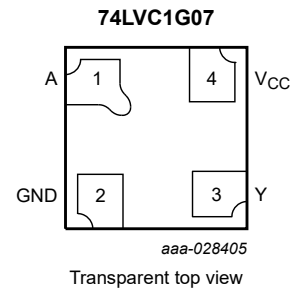


Fig. 7. Pin configuration SOT1269-2 (X2SON4)

6.2. Pin description

Table 3. Pin description

Symbol	Pin			Description
	TSSOP5, SC-74A and X2SON5	XSON6	X2SON4	
n.c.	1	1, 5	-	not connected
A	2	2	1	data input
GND	3	3	2	ground (0 V)
Y	4	4	3	data output
V _{CC}	5	6	4	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input A	Output Y
L	L
H	Z

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage		[1] -0.5	+6.5	V
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
V_O	output voltage	Active mode	[1] -0.5	+6.5	V
		Power-down mode; $V_{CC} = 0$ V	[1] -0.5	+6.5	V
I_O	output current	$V_O = 0$ V to 6.5 V	-	50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C			
		TSSOP5, SC-74A, XSON6 and X2SON5 package	[2] -	250	mW
		X2SON4 package	[3] -	150	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT353-1 (TSSOP5) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.

For SOT753 (SC-74A) package: P_{tot} derates linearly with 3.8 mW/K above 85 °C.

For SOT886 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.

For SOT1115 (XSON6) package: P_{tot} derates linearly with 3.2 mW/K above 71 °C.

For SOT1202 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.

For SOT1226-3 (X2SON5) package: P_{tot} derates linearly with 3.0 mW/K above 67 °C.

[3] For SOT1269-2 (X2SON4) package: P_{tot} derates linearly with 1.7 mW/K above 57 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	Active mode	0	-	5.5	V
		Power-down mode; $V_{CC} = 0$ V	0	-	5.5	V
T_{amb}	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	-	-	20	ns/V
		$V_{CC} = 2.7$ V to 5.5 V	-	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65V _{CC}	-	-	0.65V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7V _{CC}	-	-	0.7V _{CC}	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35V _{CC}	-	0.35V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3V _{CC}	-	0.3V _{CC}	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 µA; V _{CC} = 1.65 V to 5.5 V	-	-	0.10	-	0.10	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.70	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.30	-	0.45	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.40	-	0.60	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.80	V
		I _O = 32 mA; V _{CC} = 4.5 V	-	-	0.55	-	0.80	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V [2]	-	±0.1	±1	-	±1	µA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 5.5 V	-	±0.1	±2	-	±2	µA
I _{OFF}	power-off leakage current	V _I or V _O = 5.5 V; V _{CC} = 0 V	-	±0.1	±2	-	±2	µA
I _{CC}	supply current	V _I = 5.5 V or GND; I _O = 0 A; V _{CC} = 1.65 V to 5.5 V	-	0.1	4	-	4	µA
ΔI _{CC}	additional supply current	per pin; V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 2.3 V to 5.5 V [2]	-	5	500	-	500	µA
C _I	input capacitance	V _{CC} = 3.3 V; V _I = GND to V _{CC}	-	5.0	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

[2] These typical values are measured at V_{CC} = 3.3 V.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 9.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t _{pd}	propagation delay	A to Y; see Fig. 8 [2]						
		V _{CC} = 1.65 V to 1.95 V	1.0	2.6	6.7	1.0	8.4	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	1.7	5.5	0.5	7.0	ns
		V _{CC} = 2.7 V	0.5	2.3	4.7	0.5	6.0	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	2.2	4.2	0.5	5.5	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	1.6	3.5	0.5	4.5	ns
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} ; V _{CC} = 3.3 V [3]	-	7.0	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2] t_{pd} is the same as t_{PLZ} and t_{PZL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

∑(C_L × V_{CC}² × f_o) = sum of outputs.

11.1. Waveforms and test circuit

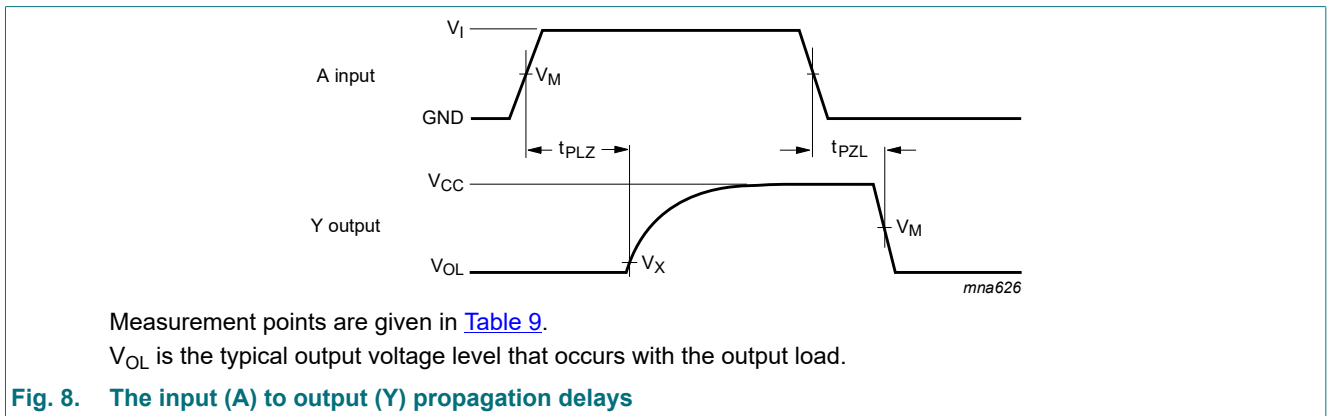
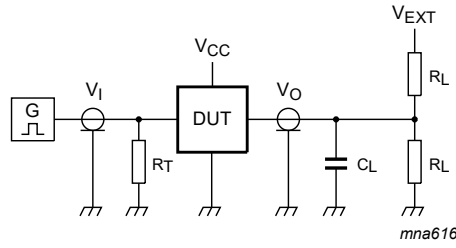


Fig. 8. The input (A) to output (Y) propagation delays

Table 9. Measurement points

Supply voltage	Input	Output	
V _{CC}	V _M	V _M	V _X
1.65 V to 1.95 V	0.5V _{CC}	0.5V _{CC}	V _{OL} + 0.15 V
2.3 V to 2.7 V	0.5V _{CC}	0.5V _{CC}	V _{OL} + 0.15 V
2.7 V	1.5 V	1.5 V	V _{OL} + 0.3 V
3.0 V to 3.6 V	1.5 V	1.5 V	V _{OL} + 0.3 V
4.5 V to 5.5 V	0.5V _{CC}	0.5V _{CC}	V _{OL} + 0.3 V



Test data is given in [Table 10](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 9. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PZL}, t_{PLZ}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 k Ω	$2V_{CC}$
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	$2V_{CC}$
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	6 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	6 V
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	$2V_{CC}$

12. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1



Fig. 10. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads

SOT753

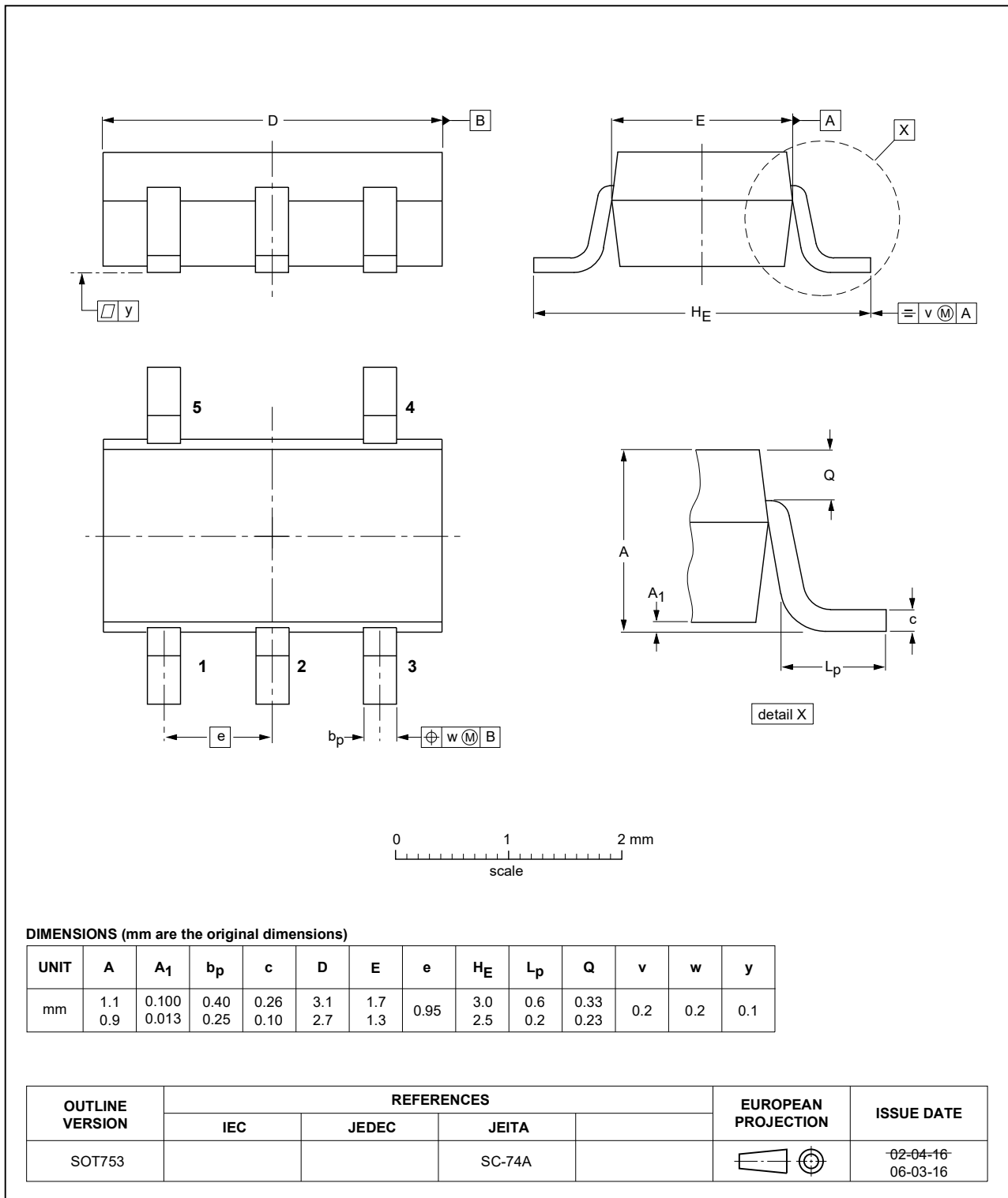


Fig. 11. Package outline SOT753 (SC-74A)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886



Fig. 12. Package outline SOT886 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 0.9 x 1.0 x 0.35 mm

SOT1115



Fig. 13. Package outline SOT1115 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 1.0 x 1.0 x 0.35 mm

SOT1202



Fig. 14. Package outline SOT1202 (XSON6)

X2SON5: plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 x 0.8 x 0.32 mm

SOT1226-3



Fig. 15. Package outline SOT1226-3 (X2SON5)

X2SON4: plastic thermal enhanced extremely thin small outline package; no leads; 4 terminals; body 0.6 x 0.6 x 0.32 mm

SOT1269-2

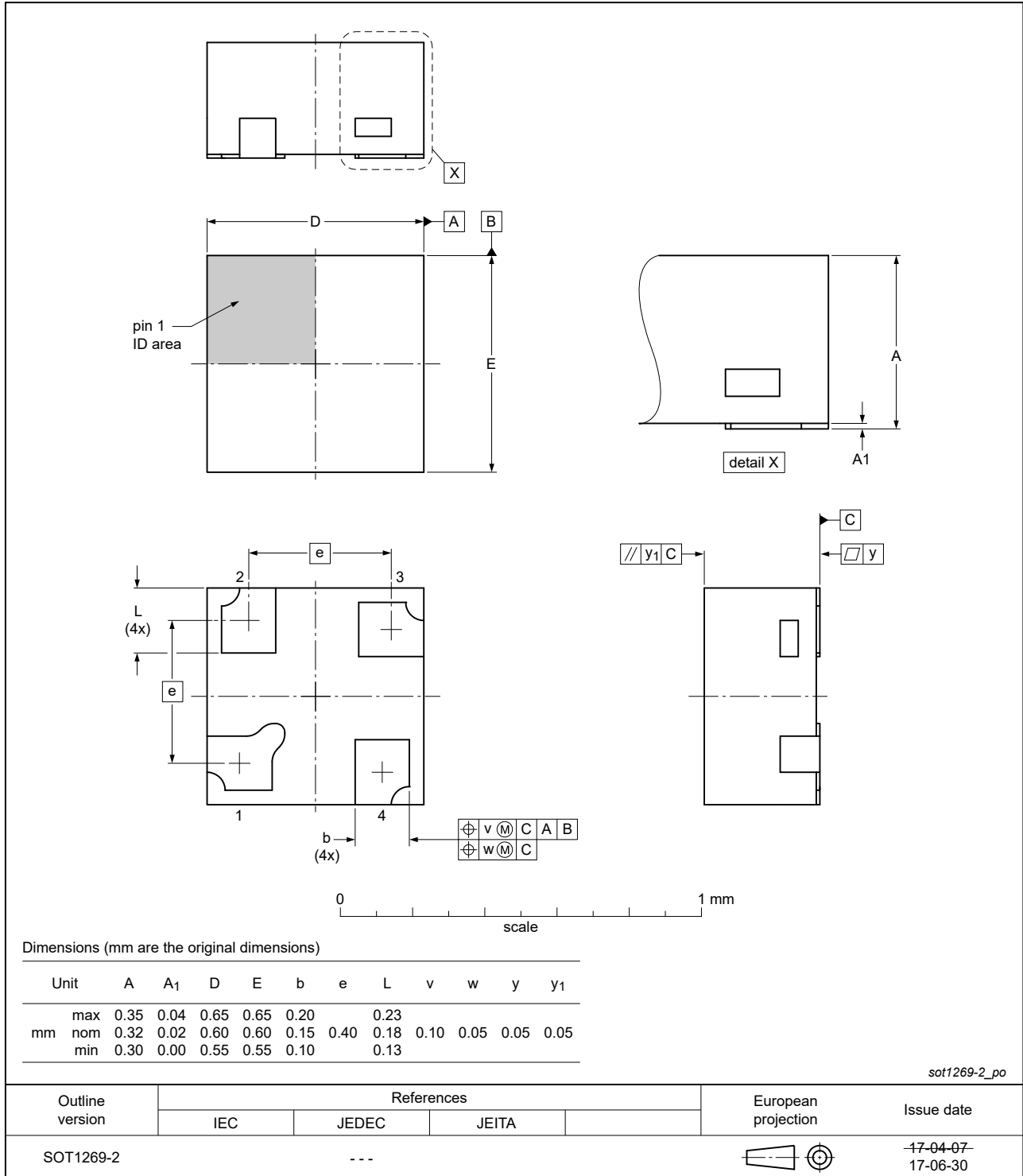


Fig. 16. Package outline SOT1269-2 (X2SON4)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G07 v.16	20220203	Product data sheet	-	74LVC1G07 v.15
Modifications:	<ul style="list-style-type: none"> Fig. 10: Package outline drawing for SOT353-1 (TSSOP5) has changed. 			
74LVC1G07 v.15	20210803	Product data sheet	-	74LVC1G07 v.14
Modifications:	<ul style="list-style-type: none"> Type number 74LVC1G07GF (SOT891/XSON6) removed. SOT1226 (X2SON5) package changed to SOT1226-3 (X2SON5) package. Section 1 and Section 2 updated. Table 5: Derating values for P_{tot} total power dissipation updated. 			
74LVC1G07 v.14	20180608	Product data sheet	-	74LVC1G07 v.13
Modifications:	<ul style="list-style-type: none"> Added type number 74LVC1G07GX4 (SOT1269-2) 			
74LVC1G07 v.13	20170511	Product data sheet	-	74LVC1G07 v.12
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 			
74LVC1G07 v.12	20161128	Product data sheet	-	74LVC1G07 v.11
Modifications:	<ul style="list-style-type: none"> Table 7: The maximum limits for leakage current and supply current have changed. 			
74LVC1G07 v.11	20120629	Product data sheet	-	74LVC1G07 v.10
Modifications:	<ul style="list-style-type: none"> Added type number 74LVC1G07GX (SOT1226) Package outline drawing of SOT886 (Fig. 12) modified. 			
74LVC1G07 v.10	20111207	Product data sheet	-	74LVC1G07 v.9
Modifications:	<ul style="list-style-type: none"> Legal pages updated. 			
74LVC1G07 v.9	20100824	Product data sheet	-	74LVC1G07 v.8
74LVC1G07 v.8	20070717	Product data sheet	-	74LVC1G07 v.7
74LVC1G07 v.7	20070515	Product data sheet	-	74LVC1G07 v.6
74LVC1G07 v.6	20040907	Product specification	-	74LVC1G07 v.5
74LVC1G07 v.5	20030307	Product specification	-	74LVC1G07 v.4
74LVC1G07 v.4	20021002	Product specification	-	74LVC1G07 v.3
74LVC1G07 v.3	20020528	Product specification	-	74LVC1G07 v.2
74LVC1G07 v.2	20010406	Product specification	-	74LVC1G07 v.1
74LVC1G07 v.1	20001122	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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Contents

1. General description	1
2. Features and benefits	1
3. Ordering information	2
4. Marking	2
5. Functional diagram	2
6. Pinning information	3
6.1. Pinning.....	3
6.2. Pin description.....	3
7. Functional description	3
8. Limiting values	4
9. Recommended operating conditions	4
10. Static characteristics	5
11. Dynamic characteristics	6
11.1. Waveforms and test circuit.....	6
12. Package outline	8
13. Abbreviations	15
14. Revision history	15
15. Legal information	16

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