Product Change Notification - SYST-22TQTN001

Date:

23 Apr 2020

Product Category:

8-bit Microcontrollers

Affected CPNs:

Notification subject:

ERRATA - AVR128DA28/32/48/64 Silicon Errata and Data Sheet Clarification Errata Document Revision

Notification text:

SYST-22TQTN001

Microchip has released a new Product Documents for the AVR128DA28/32/48/64 Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at AVR128DA28/32/48/64 Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change: Initial document release

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 23 Apr 2020

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

AVR128DA28/32/48/64 Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

AVR128DA28-I/SO
AVR128DA28-I/SP
AVR128DA28-I/SS
AVR128DA28T-I/SO
AVR128DA28T-I/SS
AVR128DA32-I/PT
AVR128DA32-I/RXB
AVR128DA32T-I/PT
AVR128DA32T-I/RXB
AVR128DA48-I/6LX
AVR128DA48-I/PT
AVR128DA48T-I/6LX
AVR128DA48T-I/PT
AVR128DA64-I/MR
AVR128DA64-I/PT
AVR128DA64T-I/MR
AVR128DA64T-I/PT

AVR128DA28/32/48/64

Silicon Errata and Data Sheet Clarification

The AVR128DA28/32/48/64 devices you have received conform functionally to the current device data sheet (http://microchip.com/DS40002183), except for the anomalies described in this document. The erratas described in this document will likely be addressed in future revisions of the AVR128DA28/32/48/64 devices.

Note:

- This document summarizes all the silicon errata issues from all revisions of silicon, previous as well as current.
- Refer to the Device/Revision ID section in the current device data sheet (http://microchip.com/DS40002183) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance.

Table of Contents

1. Silicon Issue Summary

Legend

-	Erratum is not applicable.
X	Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision	
		Rev. A6(*)	Rev. A7
EVSYS	2.2.1 The PB[7:6] and PE[7:4] Pins are Not Connected to the Event System	X	X
PORT	2.3.1 Digital Input on Pin Automatically Disabled When Pin Selected for Analog Input	X	X
NVMCTRL	2.4.1 Flash Mapping into Data Space Not Working Properly	X	X
SPI	2.5.1 SSD Bit Must Be Set When SPIROUTE Value = NONE	X	X
TCA	2.6.1 TCA1 Pinout Alternative 2 and 3 Not Functional	X	X
TWI	2.7.1 The Output Pin Override Does Not Function as Expected	X	X
	2.7.2 The 50 nS and 300 nS SDA Hold Time Selection Bits are Swapped.	X	X
USART	2.8.1 Open-Drain Mode Does Not Work When TXD is Configured as Output	X	X

Note:
(*) This revision is the initial release of the silicon.

2. Silicon Errata Issues

2.1 Errata Details

-	Erratum is not applicable.
X	Erratum is applicable.

2.2 EVSYS - Event System

2.2.1 The PB[7:6] and PE[7:4] Pins are Not Connected to the Event System

The PB[7:6] and PE[7:4] pins are not connected to the Event System. This is true for both input and output signals into the Event System on these pins.

Work around
None.

Affected Silicon Revisions

Rev. A6	Rev. A7
X	X

2.3 PORT - I/O Pin Configuration

2.3.1 Digital Input on Pin Automatically Disabled When Pin Selected for Analog Input

If an input pin is selected to be analog input, the digital input function for those pins is automatically disabled.

Work around
None.

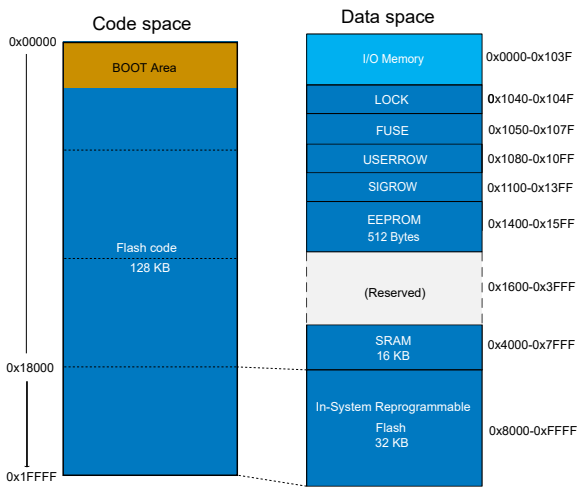
Affected Silicon Revisions

Rev. A6	Rev. A7
X	X

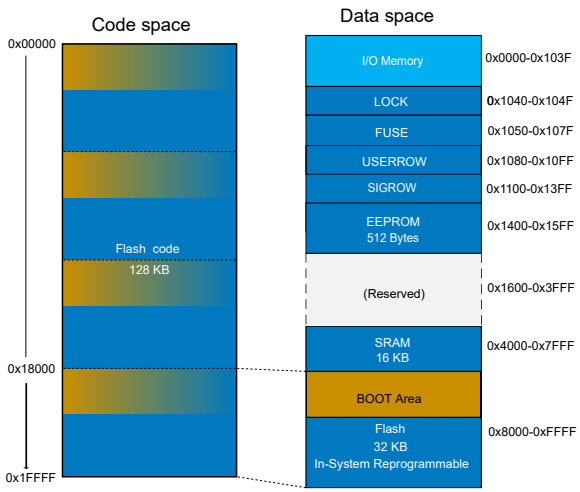
2.4 NVMCTRL - Nonvolatile Memory Controller

2.4.1 Flash Mapping into Data Space Not Working Properly

The inter-section Flash protection mechanism does not take into account the FLMAP bit field in the NVMCTRL.CTRLB register when checking if the address is in BOOT, APPCODE or APPDATA sections. It uses for comparison only the address offset between Flash start address in data space (`0x8000`) and the accessed address. This will cause the mirroring of the BOOT section in each Flash section selected by FLMAP (in blocks of 32 KB). See image below:



BOOT area for devices without issue



BOOT area for devices with issue

For read operations, the FLMAP bit field works as documented when the Boot Read Protect (BOOTRP) bit is not enabled.

For write operations, the inter-section Flash protection works properly only when FLMAP is set to `0x00`.

Work around
Use only store program memory `(SPM)` instructions to write and load program memory `(LPM)` instructions to read Flash memory.

Affected Silicon Revisions

Rev. A6	Rev. A7
X	X

2.5 SPI - Serial Peripheral Interface

2.5.1 SSD Bit Must Be Set When SPIROUTE Value = NONE

When operating either SPIn module, when the PORTMUX.SPIROUTE selection is NONE, the $\overline{SS}$ pin must be disabled (CTRLB.SSD = `1`) to maintain Master mode operation.

Work around
None.

Affected Silicon Revisions

Rev. A6	Rev. A7
X	X

2.6 TCA - 16-bit Timer/Counter Type A

2.6.1 TCA1 Pinout Alternative 2 and 3 Not Functional

It is not possible to configure TCA1 in PORTMUX.TCAROUTEA to use pinout alternative 2 and 3.

Work around
Use TCA1 pinout alternative 0 or 1.

Affected Silicon Revisions

Rev. A6	Rev. A7
X	X

2.7 TWI - Two-Wire Interface

2.7.1 The Output Pin Override Does Not Function as Expected

When TWI is enabled it overrides the output pin driver, but not the output value. So when the value in the port out (PORTx.OUT) register is '1', for the pins corresponding to the SDA or SCL, the output on the line will always be high.

Work around
Ensure that the value in the PORTx.OUT register corresponding to the SCL and SDA pins are '0' before enabling the TWI.

Affected Silicon Revisions

Rev. A6	Rev. A7
X	X

2.7.2 The 50 nS and 300 nS SDA Hold Time Selection Bits are Swapped.

The bits corresponding to the SDA Hold Time (SDAHOLD) bit field in the TWIn.CTRLA register are swapped.

Work around
Use the 50 ns bit field selection for the 300 ns hold time and vice-versa.

Affected Silicon Revisions

Rev. A6	Rev. A7
X	X

2.8 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.8.1 Open-Drain Mode Does Not Work When TXD is Configured as Output

When the USART TXD pin is configured as an output, it can drive the pin high regardless of whether the Open-Drain mode is enabled or not.

Work around
Configure the TXD pin as an input by writing the corresponding bit in PORTx.DIR to '0' when using Open-Drain mode.

Affected Silicon Revisions

Rev. A6	Rev. A7
X	X

3. Data Sheet Clarifications

None.

4. Document Revision History

Note: The data sheet clarification document revision is independent of the die revision and the device variant (last letter of the ordering number).

4.1 Revision History

Doc Rev.	Date	Comments
A	04/2020	• Initial document release.

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