ROHM SEMICONDUCTOR

Datasheet

General-Purpose 4ch Electronic Volume with Built-in Advanced Switch

BD3464FV

General Description

BD3464FV is a 4ch electronic volume which has the best audio efficiency in the industry. It has a volume switching shock sound prevention technique called "Advanced Switch," supporting the construction of high quality car audio space by simple control.

Features

- Reduce switching noise of volume by using Advanced Switch circuit.
- Energy-saving design resulting in low-current consumption by utilizing the Bi-CMOS process. It has the advantage in quality over scaling down the power heat control of the internal regulators.
- Arranges all I/O terminals together for easier PCB layout and smaller PCB area.
- I^2C BUS can be controlled by 3.3V / 5V.

Applications

It is optimal for car audio. It can also be used for car navigation, audio equipment of mini Compo, micro Compo, DVD, TV, etc.

Key Specifications

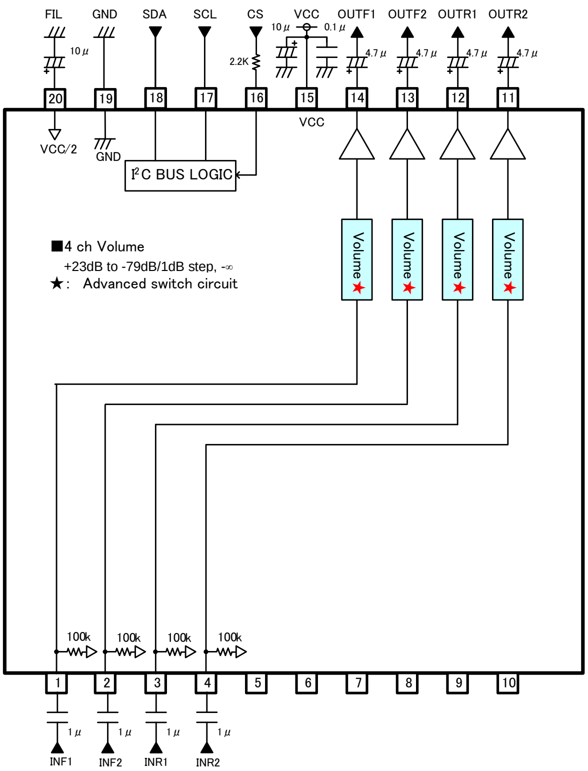
Power Supply Voltage Range:	7.0V to 9.5V
Circuit Current (no signal):	25mA (Typ)
Total Harmonic Distortion:	0.0004%(Typ)
Maximum Input Voltage:	2.35Vrms (Typ)
Cross-talk between Selectors:	-105dB (Typ)
Volume Control Range:	+23dB to -79dB
Output Noise Voltage:	1.9µVrms(Typ)
Residual Output Noise Voltage:	1.6µVrms (Typ)
Operating Temperature Range:	-40°C to +85°C

Package

W(Typ) x D(Typ) x H(Max)

SSOP-B20
6.50mm x 6.40mm x 1.45mm

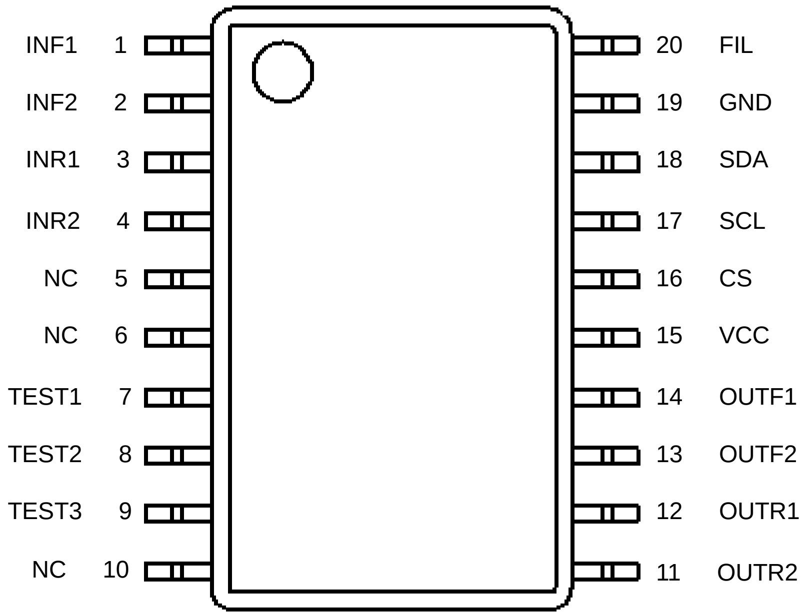
Typical Application Circuit



Unit
R : [Ω]
C : [F]

○Product structure：Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

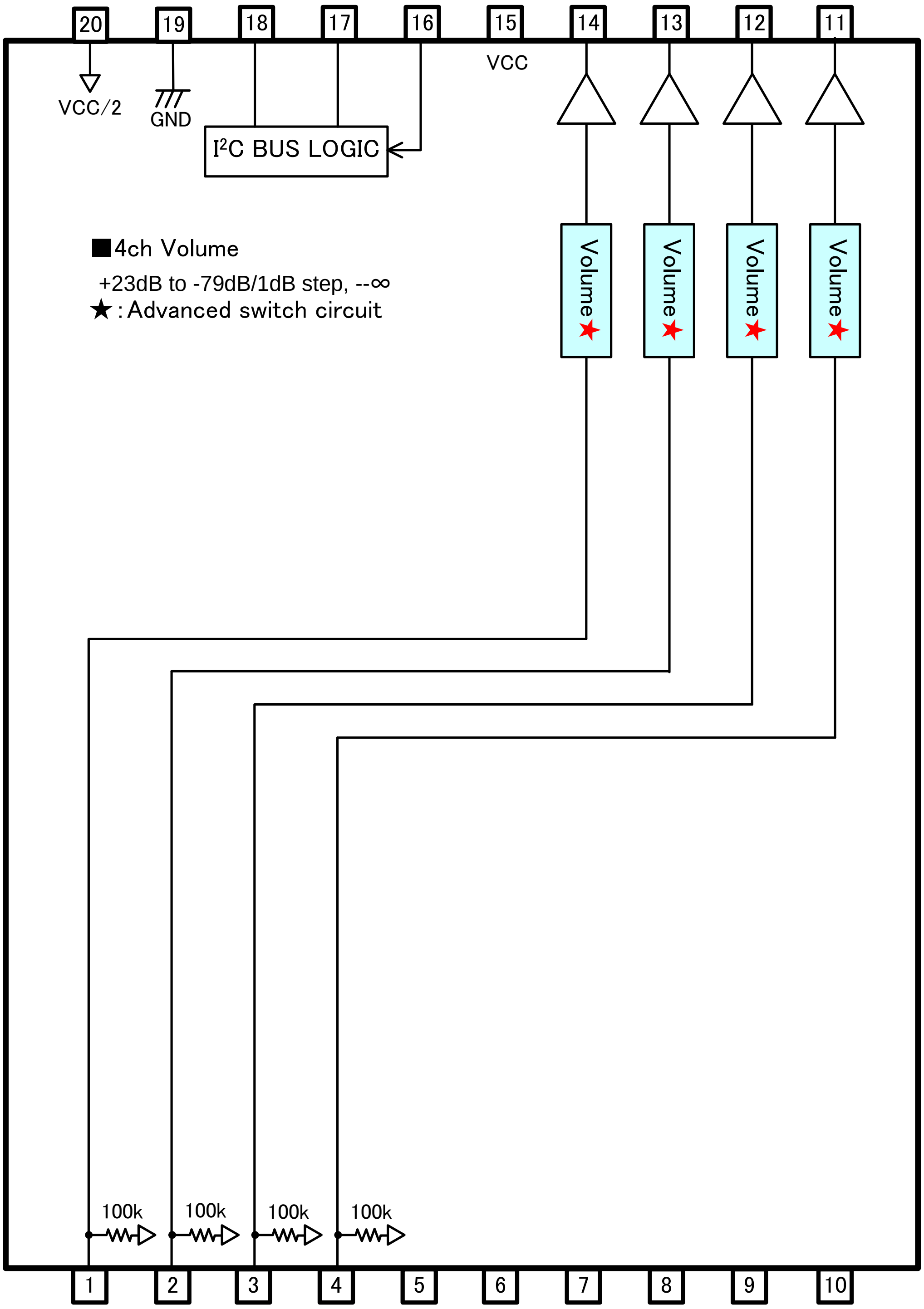
Pin Configuration



Pin Descriptions

Pin No.	Pin Name	Description	Pin No.	Pin Name	Description
1	INF1	1ch Front input terminal	11	OUTR2	2ch Rear output terminal
2	INF2	2ch Front input terminal	12	OUTR1	1ch Rear output terminal
3	INR1	1ch Rear input terminal	13	OUTF2	2ch Front output terminal
4	INR2	2ch Rear input terminal	14	OUTF1	1ch Front output terminal
5	NC		15	VCC	Power supply terminal
6	NC		16	CS	Chip select terminal
7	TEST1	Test Pin	17	SCL	I^2C Communication clock terminal
8	TEST2	Test Pin	18	SDA	I^2C Communication data terminal
9	TEST3	Test Pin	19	GND	GND terminal
10	NC		20	FIL	VCC/2 terminal

Block Diagram



Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	10.0V	V
Input Voltage	V_{IN}	V_{CC}+0.3 to GND-0.3	V
Power Dissipation	Pd	0.81 (Note 1)	W
Storage Temperature	Tastg	-55 to +150	°C

(Note 1) This value decreases 6.5mW/°C for Ta=25°C or more when mounted on ROHM standard board. Thermal resistance θja=153.8 (°C/W)
ROHM Standard board Size : 70 x 70 x 1.6(mm^3)
Material : FR4 grass epoxy board(3% or less of copper foil area)

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	7.0	-	9.5	V
Temperature	Topr	-40	-	+85	°C

Electrical Characteristics

(Unless specified, Ta=25°C, V_{CC}=8.5V, f=1kHz, V_{IN}=1Vrms, Rg=600Ω, R_L=10kΩ, INF1 input, Volume 0dB)

BLOCK	Parameter	Symbol	Limit			Unit	Conditions
			Min	Typ	Max		
GENERAL	Circuit Current (No Signal)	I_Q	-	25	40	mA	No signal
	Voltage Gain	G_V	-1.5	0	+1.5	dB	G_V=20log(V_{OUT}/V_{IN})
	Channel Balance	CB	-1.5	0	+1.5	dB	CB=G_{V1}-G_{V2}
	Total Harmonic Distortion	THD	-	0.0004	0.05	%	V_{OUT}=1Vrms BW=400Hz-30KHz
	Output Noise Voltage *	V_{NO}	-	1.9	10	μVrms	Rg=0Ω BW=IHF-A
	Residual Output Noise Voltage *	V_{NOR}	-	1.6	10	μVrms	Volume=-∞dB Rg=0Ω BW=IHF-A
	Cross-talk Between Channels *	CTC	-	-105	-90	dB	Rg=0Ω CTC=20log(V_{OUT}/V_{IN}) BW=IHF-A
	Ripple Rejection	RR	-	-80	-40	THD	f=100Hz V_{RR}=100mVrms RR=20log(V_{OUT}/V_{CC}IN)

Electrical Characteristics – continued

(Unless specified, Ta=25°C, V_{CC}=8.5V, f=1kHz, V_{IN}=1Vrms, Rg=600Ω, R_L=10kΩ, INF1 input, Volume 0dB)

BLOCK	Parameter	Symbol	Limit Min	Limit Typ	Limit Max	Unit	Conditions
VOLUME	Input Impedance	R_{IN_V}	70	100	130	kΩ	
	Maximum Input Voltage	V_{IM}	2	2.35	-	Vrms	V_{IM} AT THD+N(V_{OUT})=1% BW=400Hz-30KHz
	Maximum Gain	G_{V_BST}	21	23	25	dB	GAIN=23DB V_{IN}=100mVrms G_V=20log(V_{OUT}/V_{IN})
	Maximum Attenuation *	G_{V_MIN}	-	-109	-90	dB	Volume=-∞dB G_V=20log(V_{OUT}/V_{IN}) BW=IHF-A
	Step Resolution	G_{V_STEP}	-	1	-	dB	GAIN&ATT=+23dB to -79dB
	Gain Set Error	G_{V_ERR}	-2	0	+2	dB	GAIN=+1dB to +23dB
	Attenuation Set Error 1	G_{V_ERR1}	-2	0	+2	dB	ATT=-1dB to -15dB
	Attenuation Set Error 2	G_{V_ERR2}	-3	0	+3	dB	ATT=-16dB to -47dB
	Attenuation Set Error 3	G_{V_ERR3}	-4	0	+4	dB	ATT=-48dB to -79dB
	Output Impedance	R_{OUT}	-	-	50	Ω	V_{IN} =100mVrms
	Maximum Output Voltage	V_{OM}	2	2.35	-	Vrms	THD+N=1% BW=400Hz-30kHz

VP-9690A (Average value detection, effective value display) filter by Matsushita Communication is used for * measurement.
Phase between input / output is same.

Typical Performance Curves

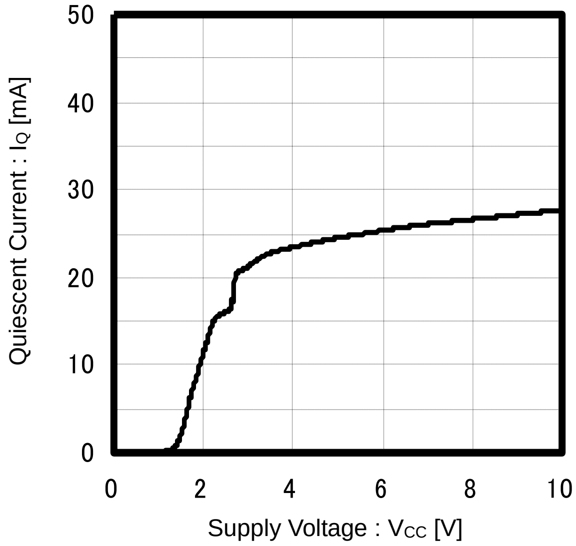


Figure 1. Quiescent Current vs Supply Voltage

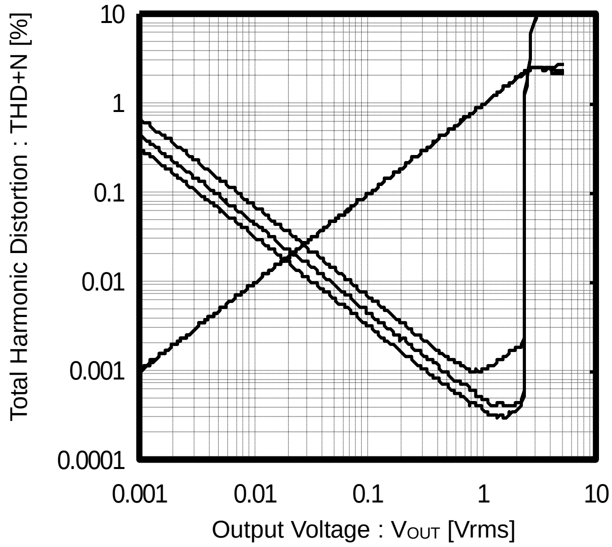


Figure 2. Total Harmonic Distortion vs Output Voltage

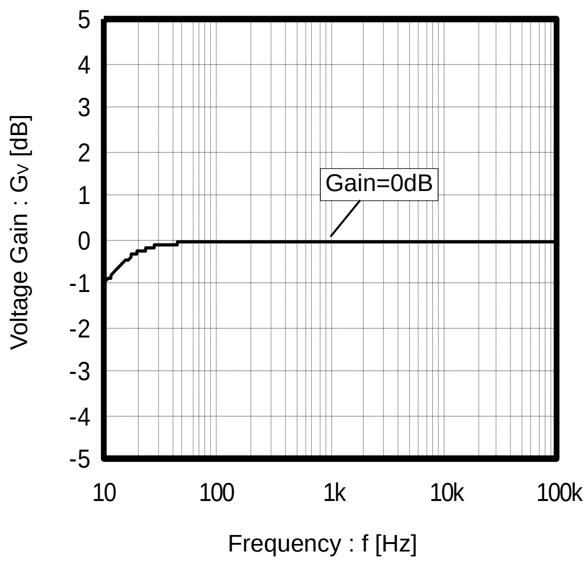


Figure 3. Voltage Gain vs Frequency

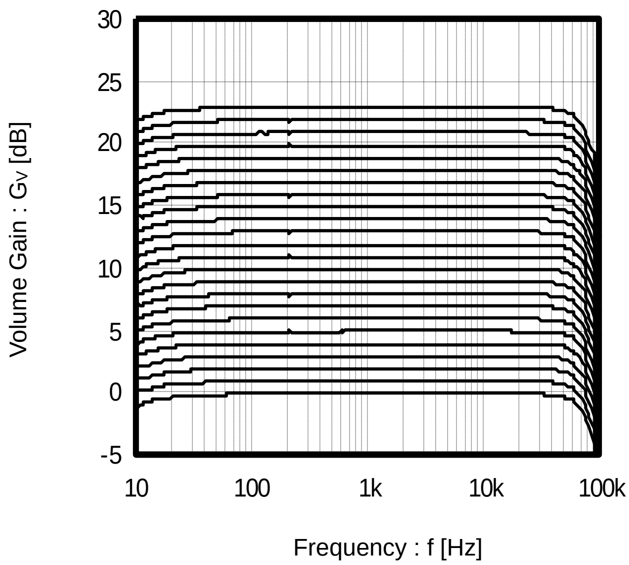


Figure 4. Volume Gain vs Frequency (0dB to +23dB)

Typical Performance Curves – continued

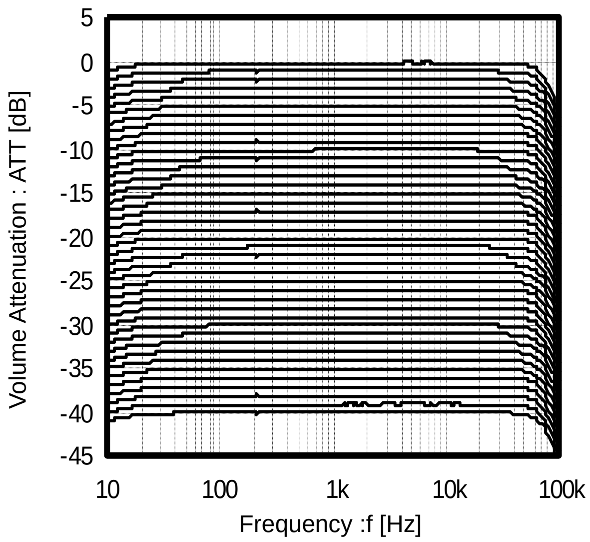


Figure 5. Volume Gain vs Frequency 1
(0dB to -40dB)

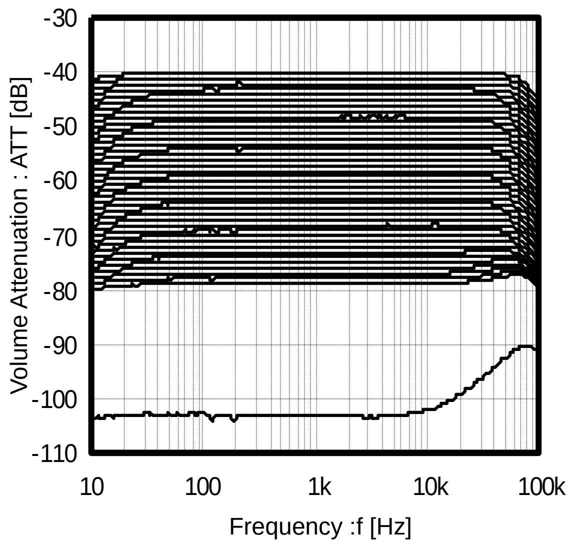


Figure 6. Volume Gain vs Frequency 2
(-41dB to -79dB)

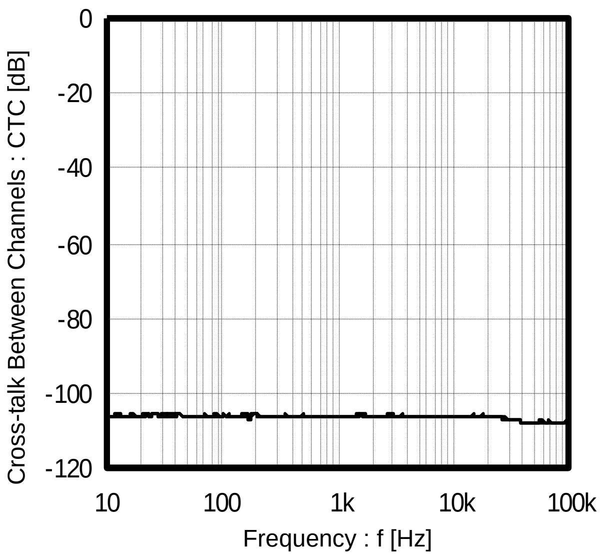


Figure 7. Cross-Talk Between Channels vs Frequency

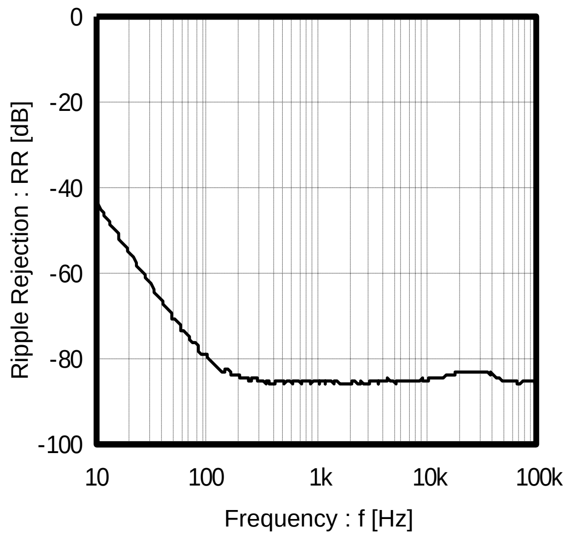


Figure 8. Ripple Rejection Ratio vs Frequency

Typical Performance Curves – continued

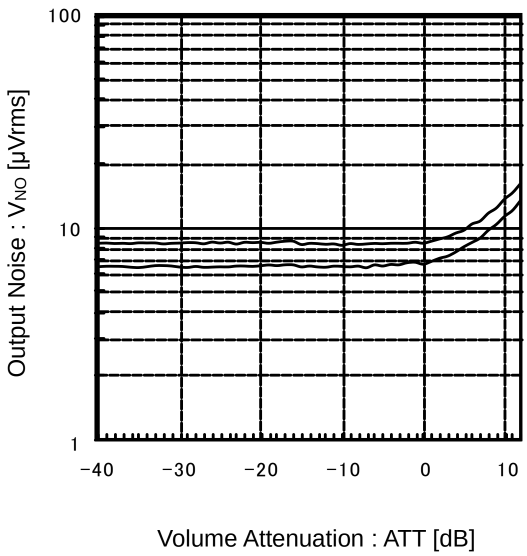


Figure 9. Output Noise vs Volume Attenuation

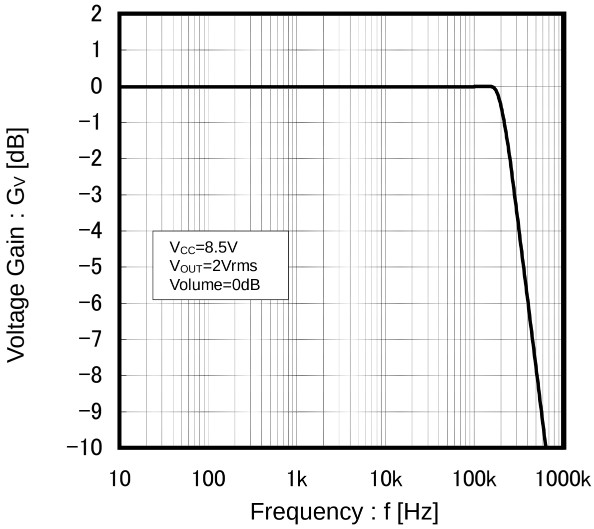


Figure 10. Volume Gain of Large Output Level vs Frequency

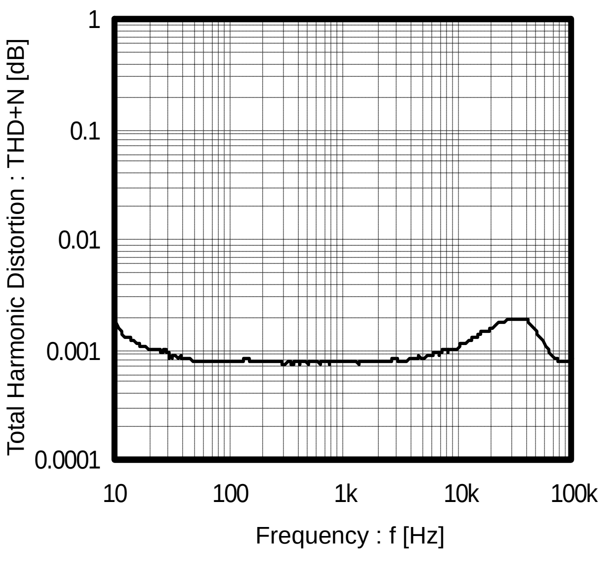


Figure 11. Total Harmonic Distortion vs Frequency

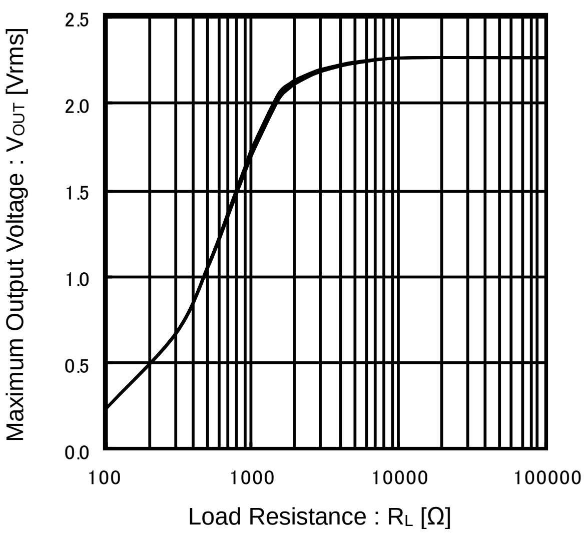


Figure 12. Maximum Output Voltage vs Load Resistance

Typical Performance Curves – continued

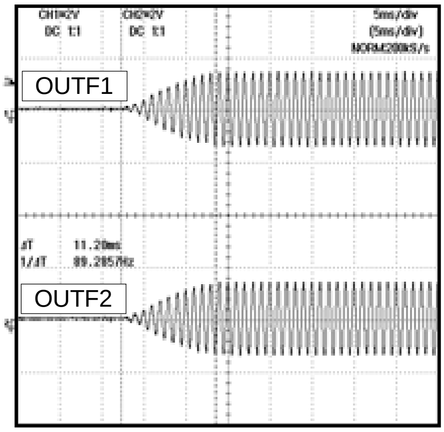


Figure 13. Advanced Switch 1

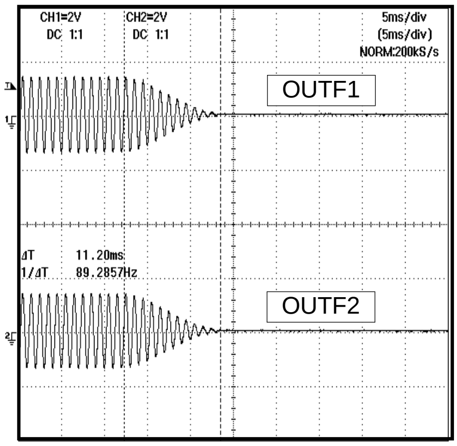


Figure 14. Advanced Switch 2

Timing Chart

Control Signal Specifications

(1) Electrical Specifications and Timing for Bus Lines and I/O Stages

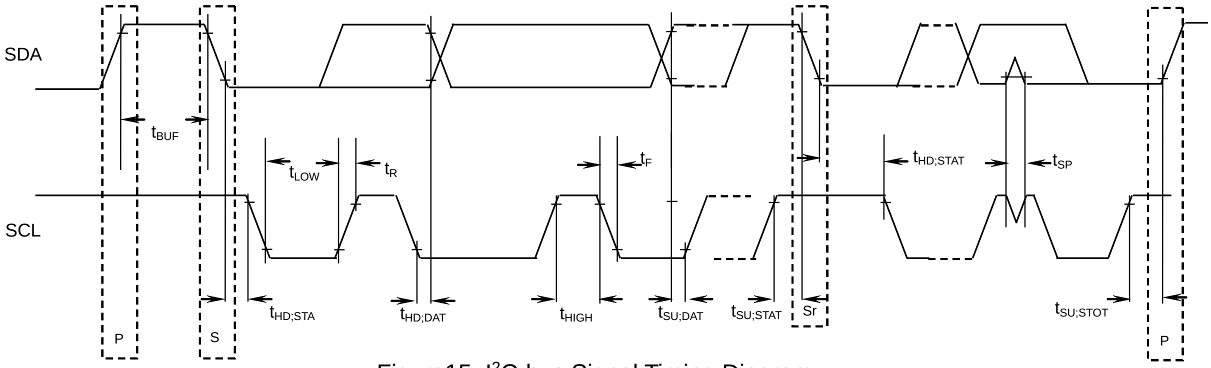


Figure15. I^2C-bus Signal Timing Diagram

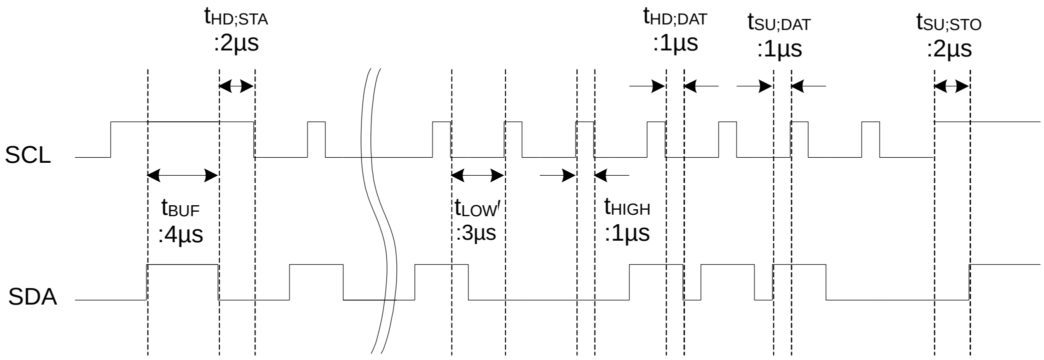
Table 1 Characteristics of the SDA and SCL bus lines for I^2C-bus devices
(Unless specified, Ta=25°C, V_{CC}=8.5V)

Parameter		Symbol	Fast-mode I^2C-bus		Unit
			Min	Max	
1	SCL clock frequency	f_{SCL}	0	400	kHz
2	Bus free time between a STOP and START condition	t_{BUF}	1.3	-	μS
3	Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	0.6	-	μS
4	LOW period of the SCL clock	t_{LOW}	1.3	-	μS
5	HIGH period of the SCL clock	t_{HIGH}	0.6	-	μS
6	Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	-	μS
7	Data hold time	$t_{HD;DAT}$	0 (Note)	-	μS
8	Data set-up time	$t_{SU;DAT}$	100	-	ns
9	Set-up time for STOP condition	$t_{SU;STO}$	0.6	-	μS

All values referred to VIH Min and VIL Max Levels (see Table 2).
(Note) To avoid sending right after the fall-edge of SCL (VIH min of the SCL signal), the transmitter sets a holding time of 300ns or more for the SDA signal.
About 7($t_{HD;DAT}$), 8($t_{SU;DAT}$), make it the setup which a margin is fully in .

Table 2 Characteristics of the SDA and SCL I/O stages for I^2C-bus devices

Parameter		Symbol	Fast-mode devices		Unit
			Min	Max	
10	LOW level input voltage	V_{IL}	-0.5	+1	V
11	HIGH level input voltage	V_{IH}	2.3	-	V
12	Pulse width of spikes which must be suppressed by the input filter.	t_{SP}	0	50	ns
13	LOW level output voltage (open drain or open collector) at 3mA sink current	V_{OL1}	0	0.4	V
14	Input current of each I/O pin with an input voltage between 0.4V and 4.5V	I_I	-10	+10	μA



SCL clock frequency : 250 kHz

Figure16. I^2C Command Data Transmission Timing Diagram

(2) I²C BUS FORMAT

	MSB	LSB		MSB	LSB		MSB	LSB		
S	Slave Address		A	Select Address		A	Data		A	P
1bit	8bit		1bit	8bit		1bit	8bit		1bit	1bit

S = Start condition (Recognition of start bit)
Slave Address = Recognition of slave address. The first 7 bits correspond to the slave address. The least significant bit is “L” which corresponds to write mode.
A = ACKNOWLEDGE bit (Recognition of acknowledgement)
Select Address = Select address corresponding to volume, bass or treble.
Data = Data on every volume and tone.
P = Stop condition (Recognition of stop bit)

(3) I²C BUS Interface Protocol

(a) Basic format

S	Slave Address	A	Select Address	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		

(b) Automatic increment (Select Address increases (+1) according to the number of data.

S	Slave Address	A	Select Address	A	Data1	A	Data2	A	· · · ·	DataN	A	P
	MSB LSB		MSB LSB		MSB LSB		MSB LSB			MSB LSB		

(Example) ①Data1 shall be set as data of address specified by Select Address.
②Data2 shall be set as data of address specified by Select Address +1.
③DataN shall be set as data of address specified by Select Address +N-1.

(c) Configuration unavailable for transmission (In this case, only Select Address1 is set.

S	Slave Address	A	Select Address1	A	Data	A	Select Address 2	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		MSB LSB		MSB LSB		

(Note)If any data is transmitted as Select Address 2 next to data, it is recognized as data, not as Select Address 2.

(4) Slave Address

Because the slave address can be changed by the setting of CS, it is possible to use two chips at the same time on identical BUS.

SEL Voltage Condition	A6 (MSB)	A5	A4	A3	A2	A1	A0	R/W (LSB)	
GND to 0.2 x V_{CC}	1	0	0	0	0	0	0	0	80H
0.8 x V_{CC} to V_{CC}	1	0	0	0	0	1	0	0	84H

Establish the CS voltage to define the setting.

(5) Select Address & Data

Items to be set	Select Address (hex)	MSB	Data						LSB
		D7	D6	D5	D4	D3	D2	D1	D0
Initial Setup 1	01	0	0	0	0	0	0	0	0
Volume 1ch Front	28	Volume Gain / Attenuation							
Volume 2ch Front	29	Volume Gain / Attenuation							
Volume 1ch Rear	2A	Volume Gain / Attenuation							
Volume 2ch Rear	2B	Volume Gain / Attenuation							
Test Mode1	2C	1	1	1	1	1	1	1	1
Test Mode2	2D	1	1	1	1	1	1	1	1
Test Mode3	F0	0	0	0	0	0	0	0	0
System Reset	FE	1	0	0	0	0	0	0	1

Advanced Switch

(Note)
1. The Advanced Switch works in the latch part while changing from one function to another.
2. Upon continuous data transfer, the Select Address rolls over because of the automatic increment function, as shown below.

→01→28→29→2A→2B→2C→2D

Select address 28, 29, 2A, 2B(hex)

Gain & ATT	MSB	Volume Gain/Attenuation						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Prohibition (Note)	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	1
	:	:	:	:	:	:	:	:
	0	1	1	0	1	0	0	0
23dB	0	1	1	0	1	0	0	1
22dB	0	1	1	0	1	0	1	0
21dB	0	1	1	0	1	0	1	1
:	:	:	:	:	:	:	:	:
-78dB	1	1	0	0	1	1	1	0
-78dB	1	1	0	0	1	1	1	0
-79dB	1	1	0	0	1	1	1	1
Prohibition (Note)	1	1	0	1	0	0	0	0
	:	:	:	:	:	:	:	:
	1	1	1	1	1	1	1	0
-∞dB	1	1	1	1	1	1	1	1

(Note) Gain is set to "-∞dB" when sending "Prohibition data".

(6) About Power ON Reset

Initialization inside IC is carried out at one of supply voltage circuits. Initial data is sent to all addresses at supply voltage ON. Mute is ON until this initial data is sent.

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Rise Time of VCC	t_{RISE}	20	-	-	μsec	V_{CC} rise time from 0V to 3V
VCC Voltage of Release Power ON Reset	V_{POR}	-	4.1	-	V	

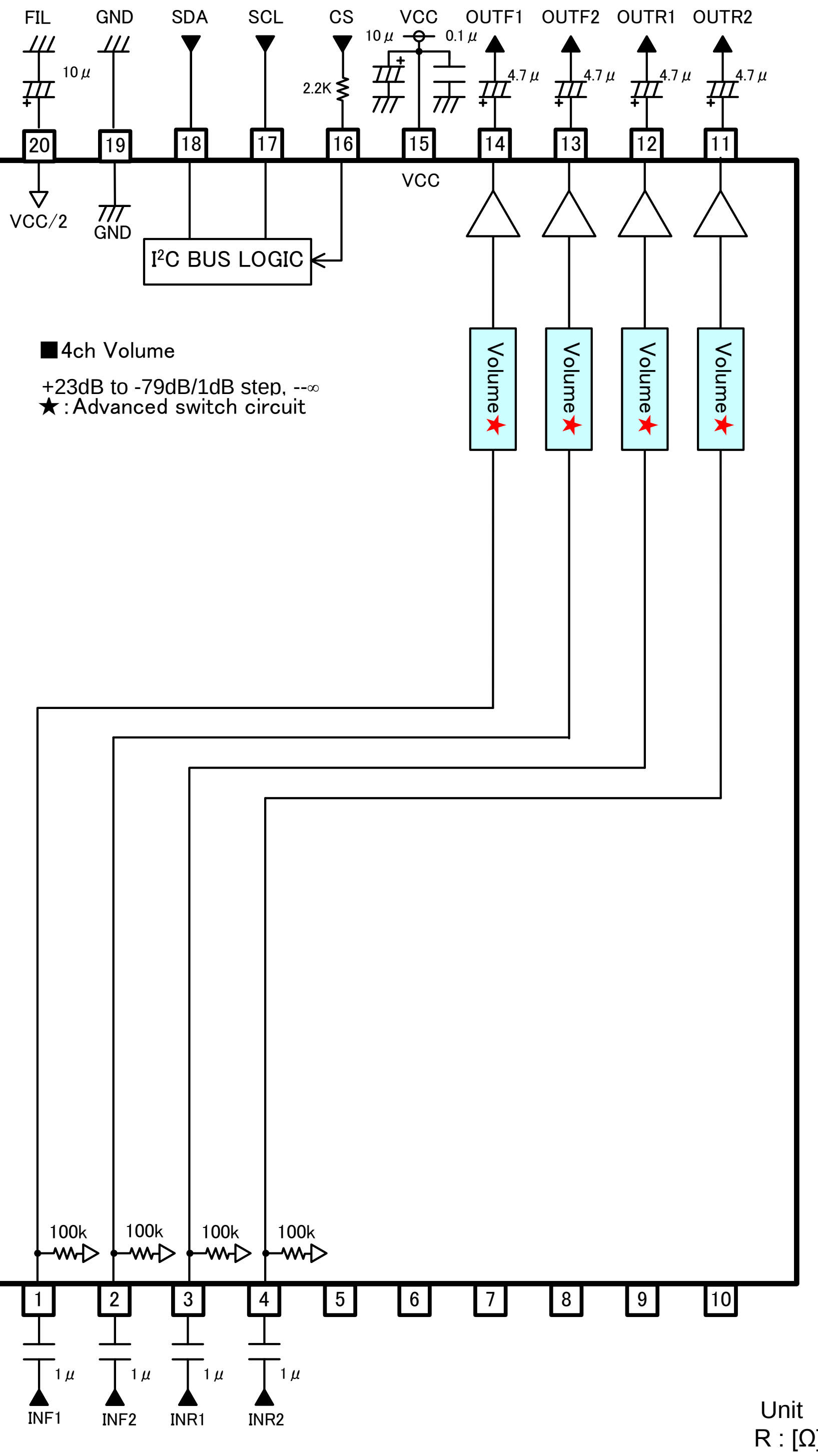
Application Information

1. Volume Gain/Attenuation of the details

(dB)	D7	D6	D5	D4	D3	D2	D1	D0	(dB)	D7	D6	D5	D4	D3	D2	D1	D0
+23	0	1	1	0	1	0	0	1	-29	1	0	0	1	1	1	0	1
+22	0	1	1	0	1	0	1	0	-30	1	0	0	1	1	1	1	0
+21	0	1	1	0	1	0	1	1	-31	1	0	0	1	1	1	1	1
+20	0	1	1	0	1	1	0	0	-32	1	0	1	0	0	0	0	0
+19	0	1	1	0	1	1	0	1	-33	1	0	1	0	0	0	0	1
+18	0	1	1	0	1	1	1	0	-34	1	0	1	0	0	0	1	0
+17	0	1	1	0	1	1	1	1	-35	1	0	1	0	0	0	1	1
+16	0	1	1	1	0	0	0	0	-36	1	0	1	0	0	1	0	0
+15	0	1	1	1	0	0	0	1	-37	1	0	1	0	0	1	0	1
+14	0	1	1	1	0	0	1	0	-38	1	0	1	0	0	1	1	0
+13	0	1	1	1	0	0	1	1	-39	1	0	1	0	0	1	1	1
+12	0	1	1	1	0	1	0	0	-40	1	0	1	0	1	0	0	0
+11	0	1	1	1	0	1	0	1	-41	1	0	1	0	1	0	0	1
+10	0	1	1	1	0	1	1	0	-42	1	0	1	0	1	0	1	0
+9	0	1	1	1	0	1	1	1	-43	1	0	1	0	1	0	1	1
+8	0	1	1	1	1	0	0	0	-44	1	0	1	0	1	1	0	0
+7	0	1	1	1	1	0	0	1	-45	1	0	1	0	1	1	0	1
+6	0	1	1	1	1	0	1	0	-46	1	0	1	0	1	1	1	0
+5	0	1	1	1	1	0	1	1	-47	1	0	1	0	1	1	1	1
+4	0	1	1	1	1	1	0	0	-48	1	0	1	1	0	0	0	0
+3	0	1	1	1	1	1	0	1	-49	1	0	1	1	0	0	0	1
+2	0	1	1	1	1	1	1	0	-50	1	0	1	1	0	0	1	0
+1	0	1	1	1	1	1	1	1	-51	1	0	1	1	0	0	1	1
0	1	0	0	0	0	0	0	0	-52	1	0	1	1	0	1	0	0
-1	1	0	0	0	0	0	0	1	-53	1	0	1	1	0	1	0	1
-2	1	0	0	0	0	0	1	0	-54	1	0	1	1	0	1	1	0
-3	1	0	0	0	0	0	1	1	-55	1	0	1	1	0	1	1	1
-4	1	0	0	0	0	1	0	0	-56	1	0	1	1	1	0	0	0
-5	1	0	0	0	0	1	0	1	-57	1	0	1	1	1	0	0	1
-6	1	0	0	0	0	1	1	0	-58	1	0	1	1	1	0	1	0
-7	1	0	0	0	0	1	1	1	-59	1	0	1	1	1	0	1	1
-8	1	0	0	0	1	0	0	0	-60	1	0	1	1	1	1	0	0
-9	1	0	0	0	1	0	0	1	-61	1	0	1	1	1	1	0	1
-10	1	0	0	0	1	0	1	0	-62	1	0	1	1	1	1	1	0
-11	1	0	0	0	1	0	1	1	-63	1	0	1	1	1	1	1	1
-12	1	0	0	0	1	1	0	0	-64	1	1	0	0	0	0	0	0
-13	1	0	0	0	1	1	0	1	-65	1	1	0	0	0	0	0	1
-14	1	0	0	0	1	1	1	0	-66	1	1	0	0	0	0	1	0
-15	1	0	0	0	1	1	1	1	-67	1	1	0	0	0	0	1	1
-16	1	0	0	1	0	0	0	0	-68	1	1	0	0	0	1	0	0
-17	1	0	0	1	0	0	0	1	-69	1	1	0	0	0	1	0	1
-18	1	0	0	1	0	0	1	0	-70	1	1	0	0	0	1	1	0
-19	1	0	0	1	0	0	1	1	-71	1	1	0	0	0	1	1	1
-20	1	0	0	1	0	1	0	0	-72	1	1	0	0	1	0	0	0
-21	1	0	0	1	0	1	0	1	-73	1	1	0	0	1	0	0	1
-22	1	0	0	1	0	1	1	0	-74	1	1	0	0	1	0	1	0
-23	1	0	0	1	0	1	1	1	-75	1	1	0	0	1	0	1	1
-24	1	0	0	1	1	0	0	0	-76	1	1	0	0	1	1	0	0
-25	1	0	0	1	1	0	0	1	-77	1	1	0	0	1	1	0	1
-26	1	0	0	1	1	0	1	0	-78	1	1	0	0	1	1	1	0
-27	1	0	0	1	1	0	1	1	-79	1	1	0	0	1	1	1	1
-28	1	0	0	1	1	1	0	0	-∞	1	1	1	1	1	1	1	1

(shaded) : Initial condition

2. Application Circuit Diagram



Unit
R : [Ω]
C : [F]

Figure 17. Application Circuit Diagram

Notes on wiring

① Please connect the decoupling capacitor of the power supply in the shortest distance as much as possible to GND.
② Lines of GND shall be one-point connected.
③ Wiring pattern of Digital shall be away from that of analog unit and cross-talk shall not be acceptable.
④ Lines of SCL and SDA of I²C BUS shall not be parallel if possible.
The lines shall be shielded, if they are adjacent to each other.
⑤ Lines of analog input shall not be parallel if possible. The lines shall be shielded, if they are adjacent to each other.

Power Dissipation

About the thermal design by the IC

Characteristics of an IC have a great deal to do with the temperature at which it is used, and exceeding absolute maximum ratings may degrade and destroy elements. Careful consideration must be given to the heat of the IC from the two standpoints of immediate damage and long-term reliability of operation.

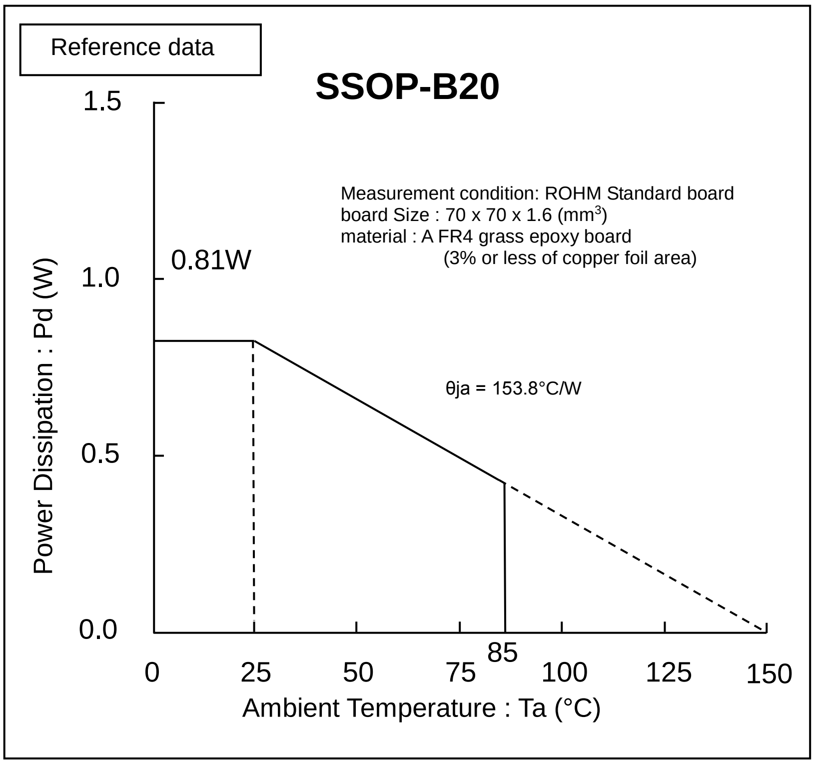
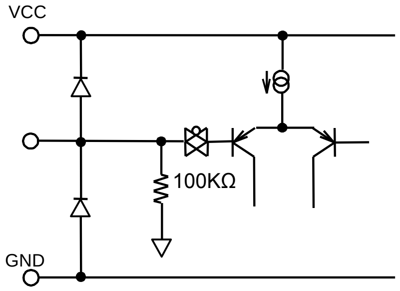
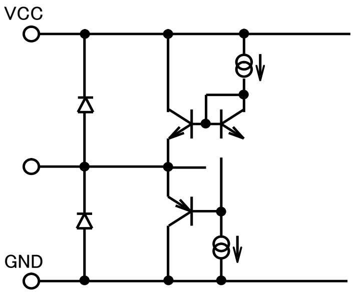
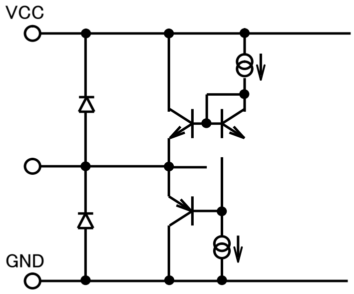


Figure 18. Temperature Derating Curve (SSOP-B20)

(Note) Values are actual measurements and are not guaranteed.

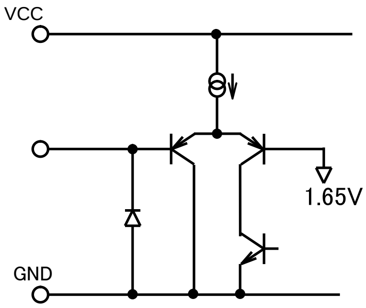
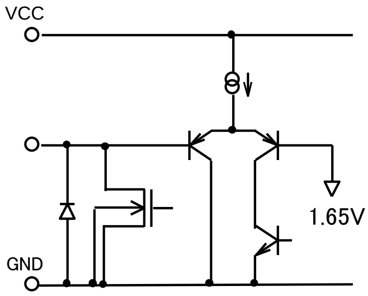
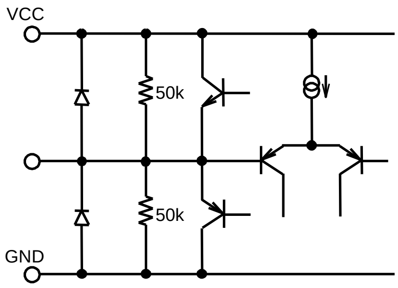
Power dissipation values vary according to the board on which the IC is mounted.

I/O Equivalent Circuits

Terminal No.	Terminal Voltage	Equivalent Circuit	Terminal Description
INF1 INF2 INR1 INR2	4.25		Signal input terminal. The input impedance is 100kΩ(typ).
OUTR2 OUTR1 OUTF2 OUTF1	4.25		Fader output terminal.
CS	-		Slave address selection terminal. “CS” is “High” to slave address “84 H” “CS” is “Low” to slave address “80 H”

The values in the input/output equivalent circuits are reference values only and are not guaranteed.

I/O Equivalent Circuits – continued

Terminal Name	Terminal Voltage	Equivalent Circuit	Terminal Description
VCC	8.5		Power supply terminal.
SCL	-		Clock input terminal of I^2C BUS communication.
SDA	-		Data input terminal of I^2C BUS communication.
GND	0		Ground terminal.
FIL	4.25		Voltage terminal for reference bias of analog signal system. The simple precharge circuit and simple discharge circuit for an external capacitor are built in.

The values in the input/output equivalent circuits are reference values only and are not guaranteed.

Operational Notes

1. **Reverse Connection of Power Supply**
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC’s power supply pins.

2. **Power Supply Lines**
Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC’s power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

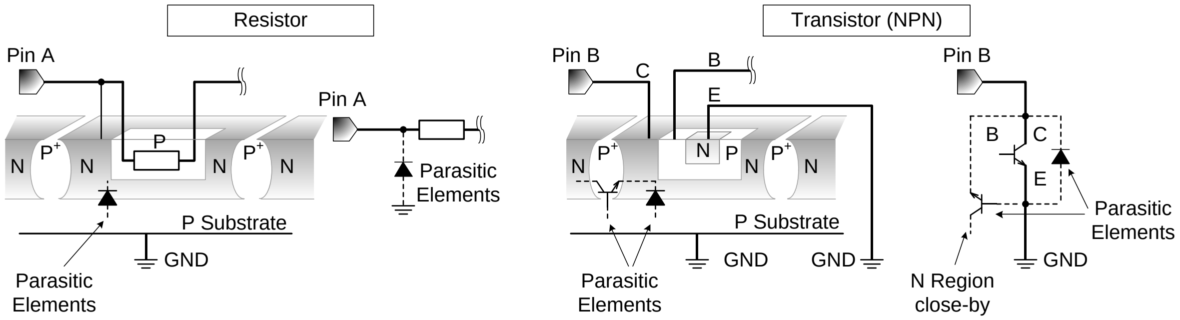
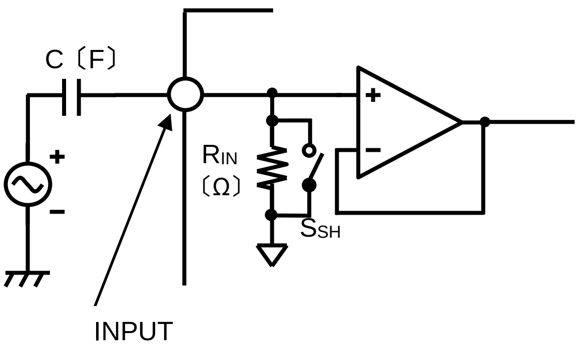


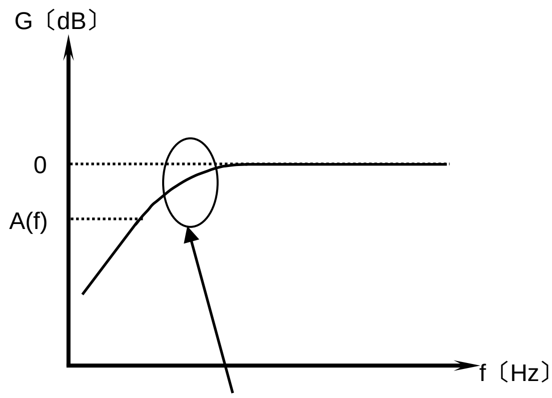
Figure 19. Example of monolithic IC structure

13. About a Signal Input Part

About Input Coupling Capacitor Constant Value

The constant value of input coupling capacitor C(F) is decided with respect to the input impedance R_{IN}(Ω) at the input signal terminal of the IC. The first HPF characteristic of RC is composed.





$$A(f) = \sqrt{\frac{(2\pi fCR_{IN})^2}{1+(2\pi fCR_{IN})^2}}$$

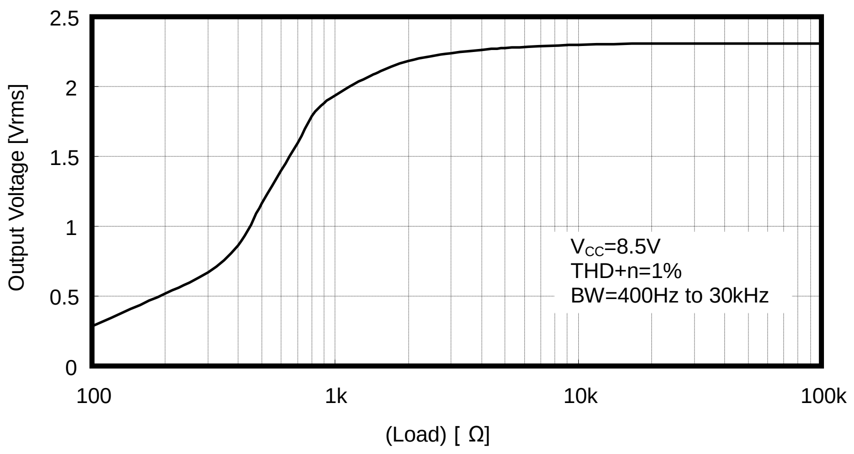
Operational Notes – continued

14. About Output Load Characteristics

The usages of output load are below (reference). Please use more than 10[kΩ] (TYP) load.

Output pin on target

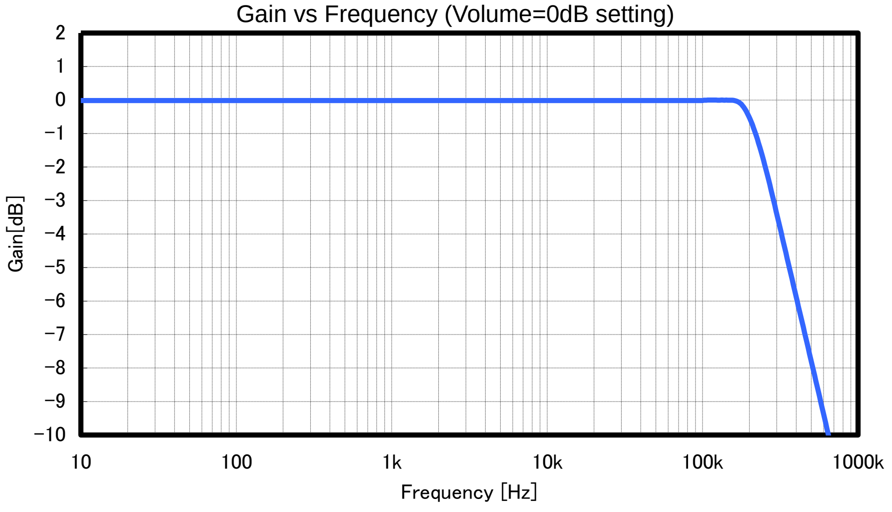
Pin Name	Pin Name
OUTF1	OUTR1
OUTF2	OUTR2



Output Load Characteristic at V_{CC}=8.5V. (Reference)

15. Frequency Characteristic at Large Output Level

High slew-rate amplifiers are used for high quality sound. This IC corresponds to “192kHz sampling on DVD-Audio” which is highest quality. Output level is “2Vrms, 192kHz flat(typ)”.
(See the below graph (reference)).

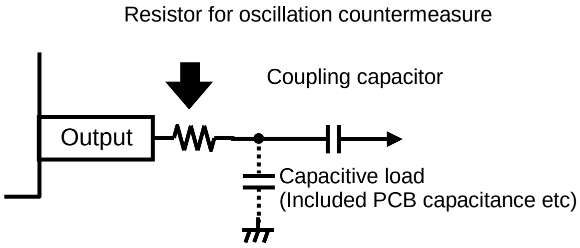


Operational Notes – continued

16. Oscillation Countermeasure for Volume Outputs at Power Supply ON/OFF

Using higher capacitance than 22pF at volume outputs may cause oscillation at the moment you turn ON/OFF the power supply (when V_{CC} is about 3V to 4V). As oscillation countermeasure, insert resistor in series to terminal directly as shown below, and set volume output to mute outside this device when turning ON/OFF the power supply.

Capacitance	Resistor in series to terminal directly
C < 22pF	Not necessary
22 < C < 220pF	220Ω



17. I²C BUS Transferring Data

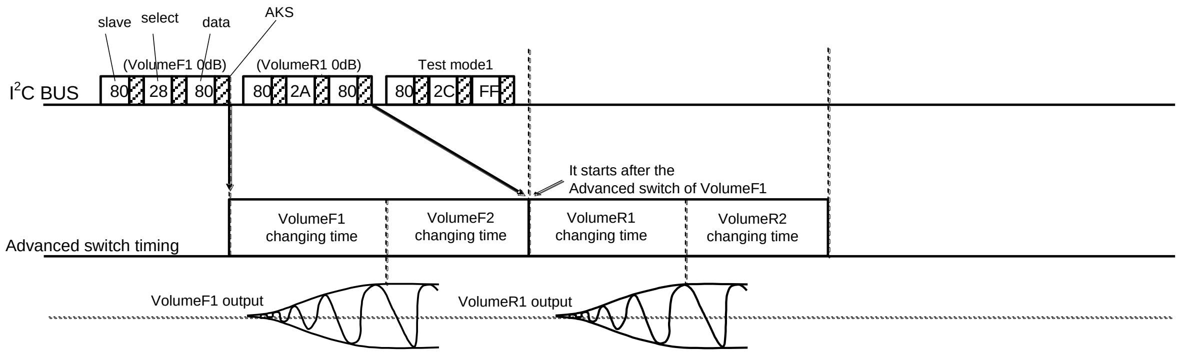
[1] Types of Data Transfer

1-1. The data transfer without Advanced Switch (data transfer without data latching format) does not have regulations on transferring data.
1-2. The data transfer with Advanced Switch (data transfer with data latching format) does not have regulations on transferring data too. But Advanced Switch data transfer follows the order in [2].

[2] Advanced Switch Data Transfer

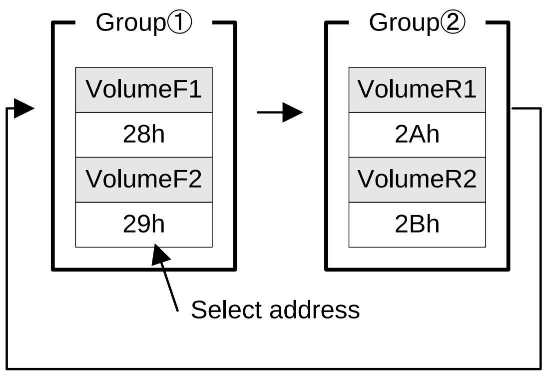
2-1. The timing chart of Advanced Switch data transfer is as follows.

- Data Transfer Example 1



(Note) It is the same even if it transfers data in auto increment mode.

There are no timing regulations in I²C BUS transferring data. But the changing time starts after the end of the present change. In addition, the timing of Advanced Switch is not dependent on transferring data turn. Instead, it follows the following turn.

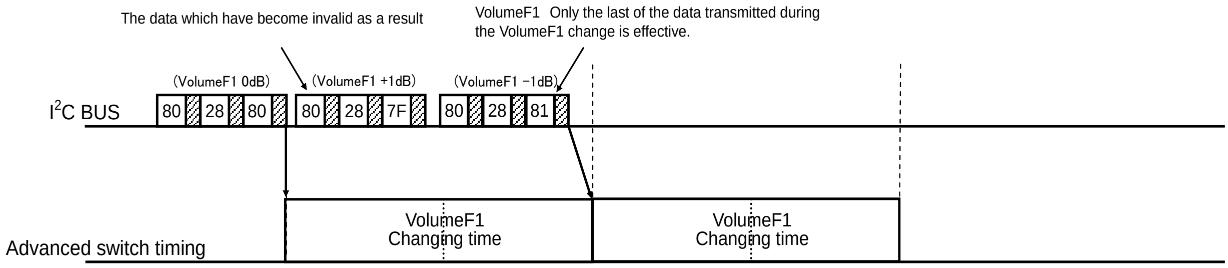


Advanced Switch Start Turn

(Note) The block in the same group can start the Advanced Switch at the same time.

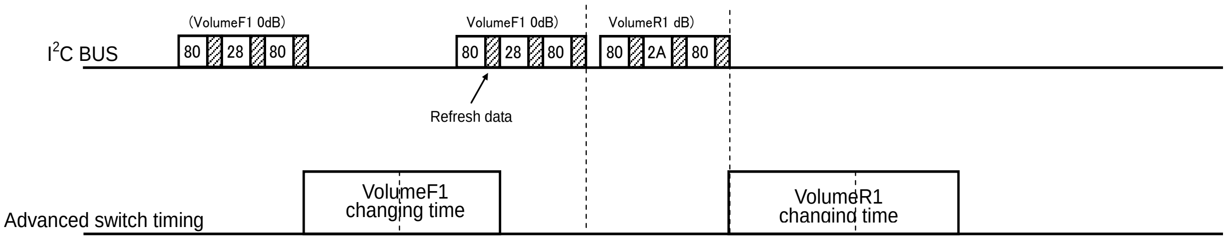
Operational Notes – continued

- Data Transfer Example 2
  Priority is given to the data of the same select address when it is transferred to the timing which Advanced Switch has not ended. In addition, when two or more data are transferred to the same select address, the end transferred data is effective.



- Data Transfer Example 3
  Refresh data is the same as the present setup data, therefore Advanced switch does not change.

The gain change data of other channels are transferred after refresh data as below.



Operational Notes – continued

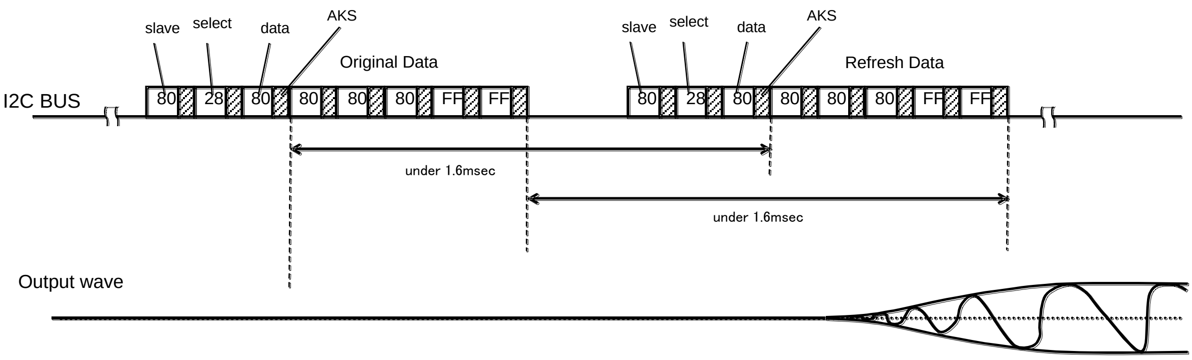
[3] Attention on Transferring Data

BD3464FV cannot set the data transfer from a microcomputer correctly on very rare occasions. In such cases, the following phenomenon may occur.

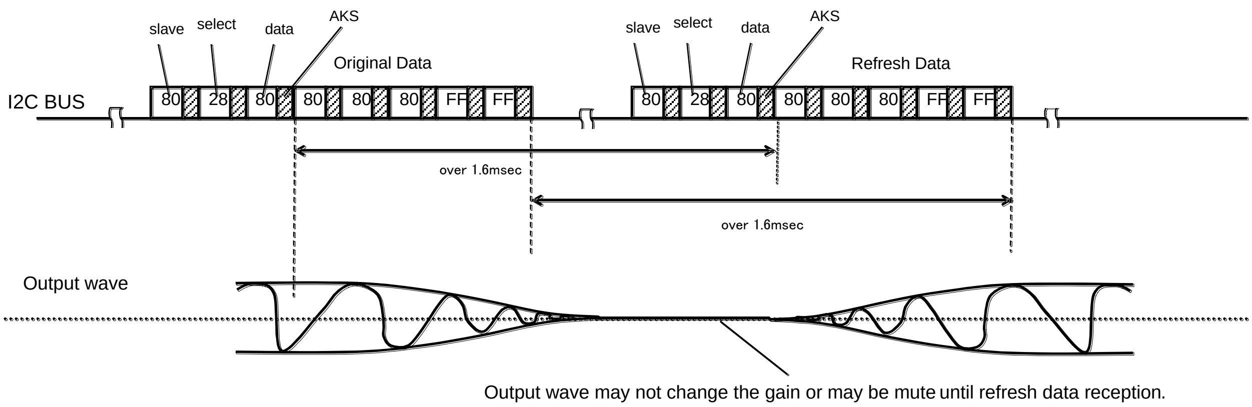
1. Volume gain does not change.
2. Volume gain changes to MUTE.

Therefore, the data transfer from a microcomputer should send data as shown in the following conditions.

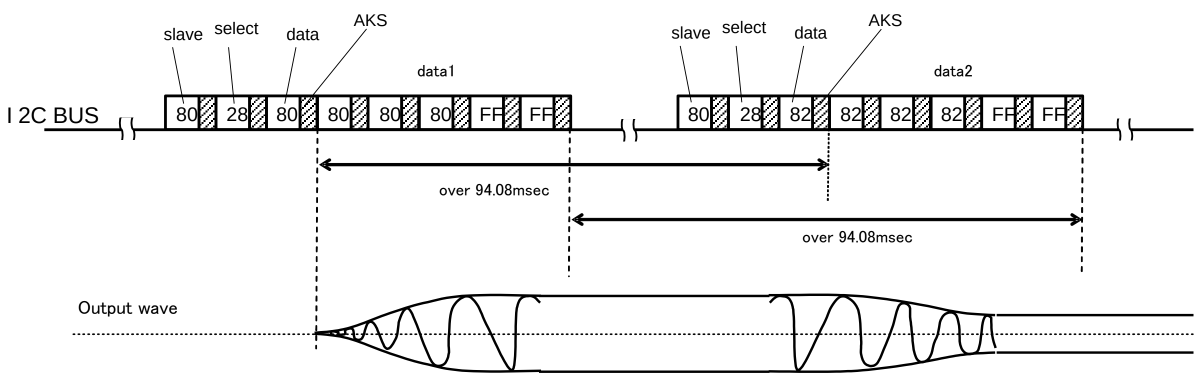
① When sending the Volume change data, please send the same data twice as below.



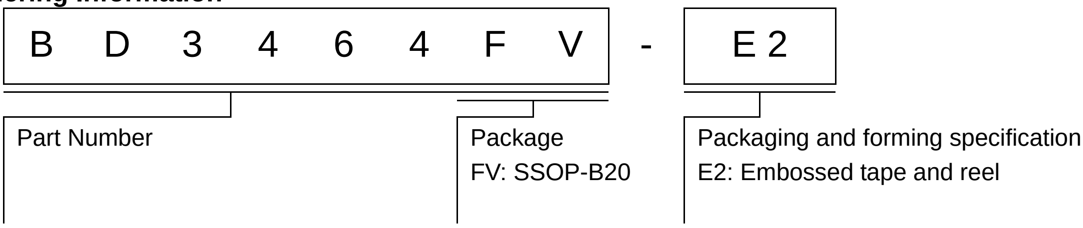
If Refresh data can't be sent like ①timing, the output wave may be put on mute momentarily.



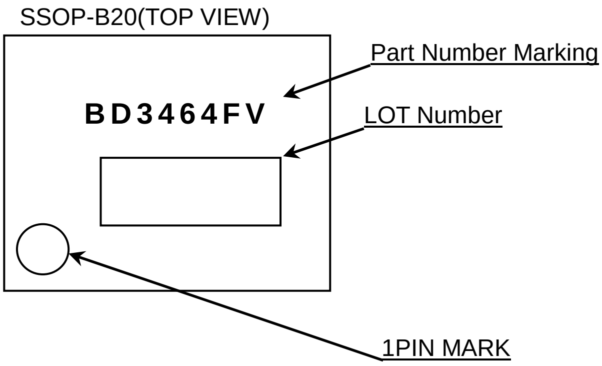
② If Volume change data can send over 94.08msec interval transferring data, there is no need to send Refresh data.



Ordering Information

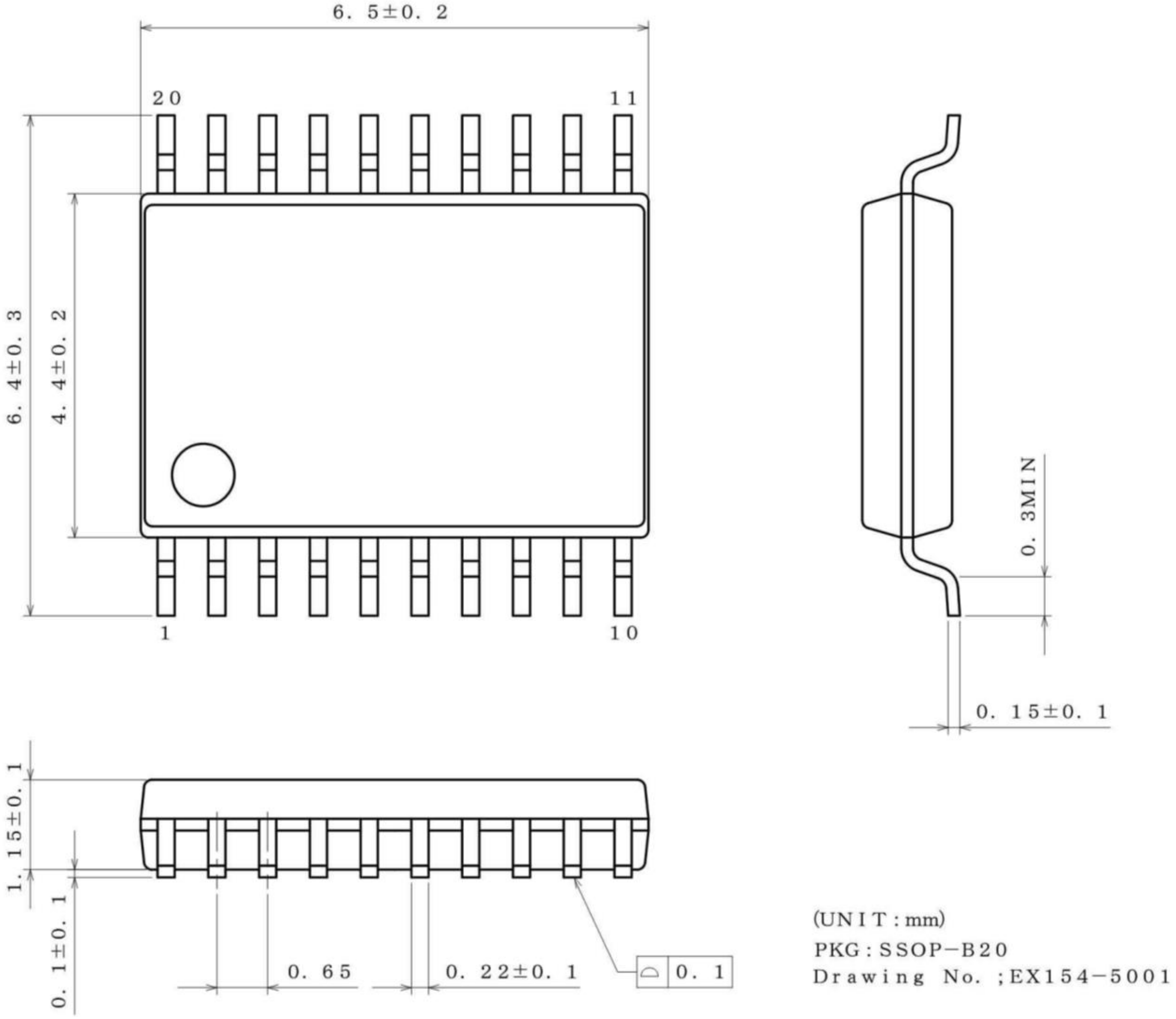


Marking Diagram



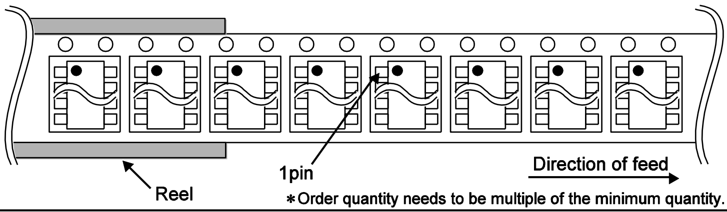
Physical Dimension, Tape and Reel Information

Package Name	SSOP-B20



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
16.Dec.2015	001	New Release

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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