

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in an MLPAK33 (SOT8002) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Trench MOSFET technology
- MLPAK33 package (3.3 x 3.3 mm footprint)

3. Applications

- High-side load switch
- Battery management
- DC-to-DC conversion
- Switching circuits

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-	-20	V
V _{GS}	gate-source voltage	_		-12	-	12	V
I _D	drain current	V_{GS} = -4.5 V; T_{amb} = 25 °C; t ≤ 5 s	[1]	-	-	-12.1	А
Static chara	acteristics						
R _{DSon}	drain-source on-state	V _{GS} = -4.5 V; I _D = -7.7 A; T _j = 25 °C		-	16	20	mΩ
	resistance	V _{GS} = -2.5 V; I _D = -5.8 A; T _j = 25 °C		-	26.4	35.2	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².



5. Pinning information

Table 2. Pinning information							
Pin	Symbol	Description	Simplified outline	Graphic symbol			
1	S	source		D			
2	S	source					
3	S	source		G-UF			
4	G	gate	— П П	s s			
5	D	drain		017aaa257			
6	D	drain					
7	D	drain	MLPAK33 (SOT8002-1)				
8	D	drain					

6. Ordering information

Table 3. Ordering information Type number			
	Name	Description	Version
PXP020-20QX	MLPAK33	plastic thermal enhanced surface mounted package; mini leads; 8 terminals; pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-1

7. Marking

Table 4. Marking codes	
Type number	Marking code
PXP020-20QX	8AD

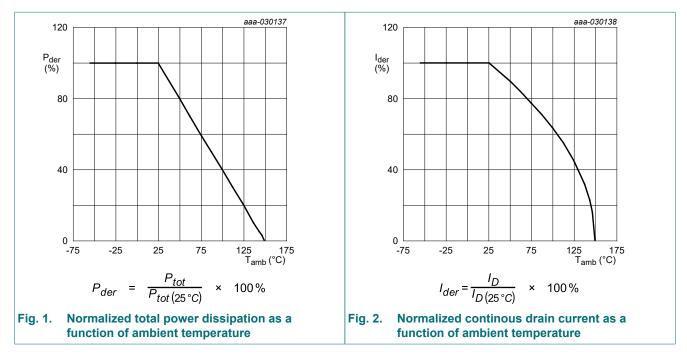
8. Limiting values

Table 5. Limiting values

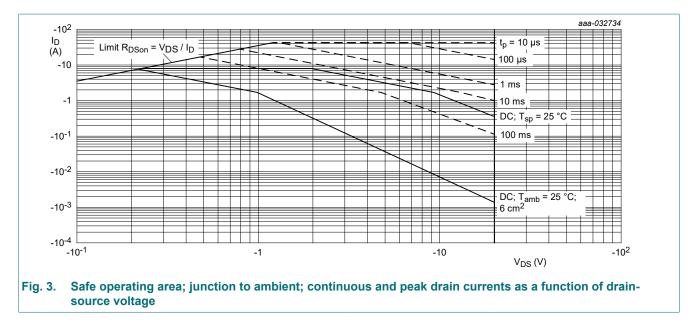
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-20	V
V _{GS}	gate-source voltage	_		-12	12	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	-12.1	А
		V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-8	А
		V _{GS} = -4.5 V; T _{amb} = 100 °C	[1]	-	-4.8	А
		V _{GS} = -4.5 V; T _{sp} = 25 °C		-	-23.5	А
I _{DM}	peak drain current	T_{amb} = 25 °C; single pulse; $t_p \le 10 \ \mu s$		-	-42.4	А
P _{tot}	total power dissipation	T _{amb} = 25 °C; t ≤ 5 s	[1]	-	4.8	W
		T _{amb} = 25 °C	[1]	-	1.8	W
		T _{sp} = 25 °C		-	50	W
Tj	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drai	n diode					
I _S	source current	T _{amb} = 25 °C	[1]	-	-1.7	А

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².



20 V, P-channel Trench MOSFET



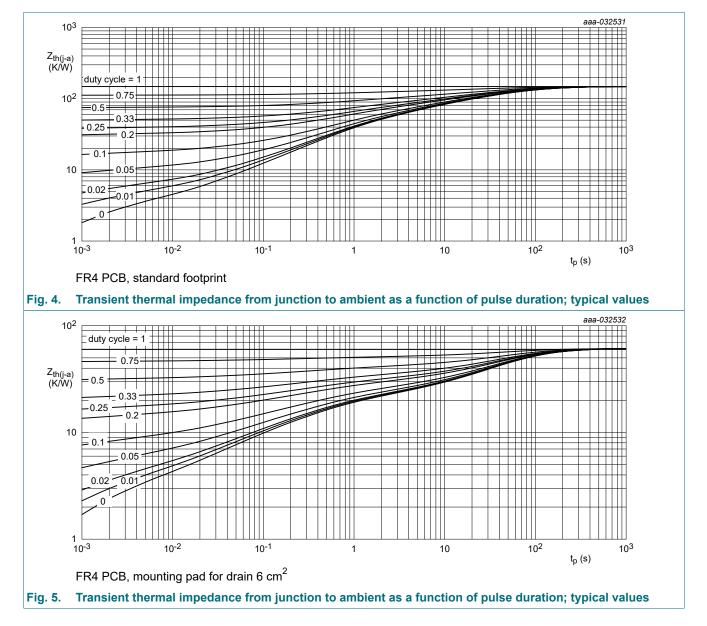
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9. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	150	190	K/W
			[2]	-	60	75	K/W
		in free air; t ≤ 5 s	[2]	-	25	30	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	4	8	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

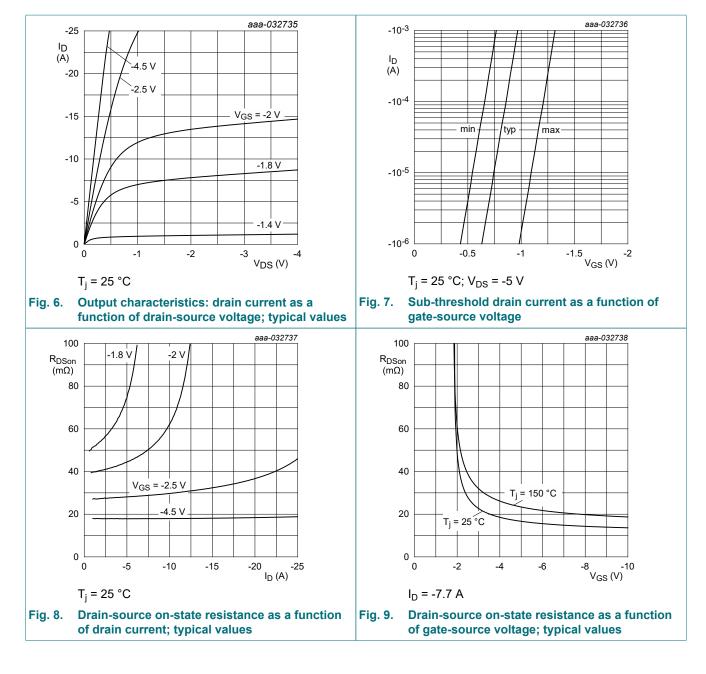
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².



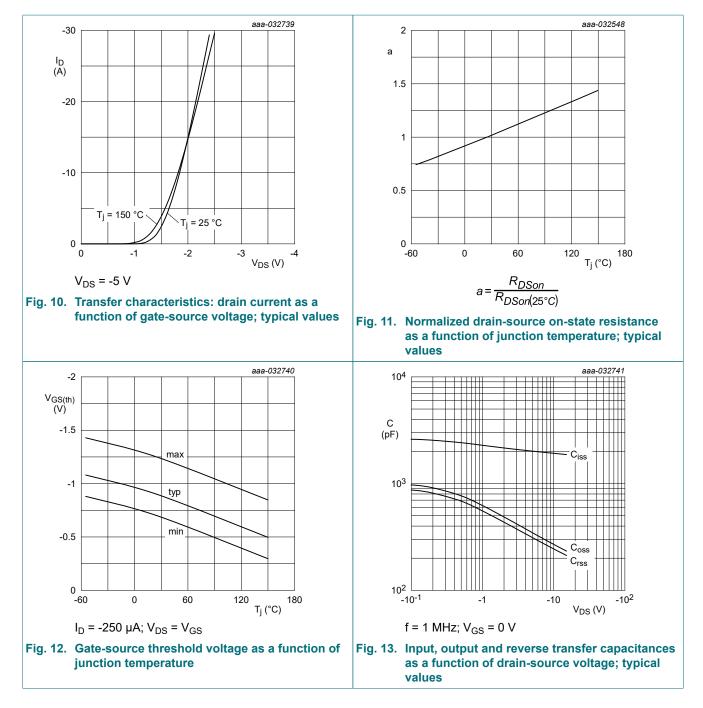
10. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	cteristics					
V _{(BR)DSS}	drain-source breakdown voltage	I _D = -250 μA; V _{GS} = 0 V; T _j = 25 °C	-20	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = -250 μA; V _{DS} =V _{GS} ; T _j = 25 °C	-0.7	-0.9	-1.25	V
I _{DSS}	drain leakage current	V _{DS} = -20 V; V _{GS} = 0 V; T _j = 25 °C	-	-	-1	μA
I _{GSS}	gate leakage current	V _{GS} = -12 V; V _{DS} = 0 V; T _j = 25 °C	-	-	-100	nA
		V _{GS} = 12 V; V _{DS} = 0 V; T _j = 25 °C	-	-	100	nA
R _{DSon}	drain-source on-state	V _{GS} = -4.5 V; I _D = -7.7 A; T _j = 25 °C	-	16	20	mΩ
	resistance	V _{GS} = -4.5 V; I _D = -7.7 A; T _j = 150 °C	-	22.7	28.4	mΩ
		V _{GS} = -2.5 V; I _D = -5.8 A; T _j = 25 °C	-	26.4	35.2	mΩ
9fs	forward transconductance	V _{DS} = -10 V; I _D = -7.7 A; T _j = 25 °C	-	21.4	-	S
R _G	gate resistance	f = 1 MHz	-	6.4	-	Ω
Dynamic ch	aracteristics	1				
Q _{G(tot)}	total gate charge	V _{DS} = -10 V; I _D = -7.7 A; V _{GS} = -4.5 V;	-	19.4	29.1	nC
Q _{GS}	gate-source charge	T _j = 25 °C	-	3.4	-	nC
Q _{GS(th)}	pre-threshold gate- source charge		-	1.6	-	nC
Q _{GS(th-pl)}	post-threshold gate- source charge		-	1.8	-	nC
Q _{GD}	gate-drain charge	1 F	-	6.2	-	nC
V _{GSpl}	gate-source plateau voltage	V _{DS} = -10 V; I _D = -7.7 A; T _j = 25 °C	-	-1.8	-	V
C _{iss}	input capacitance	V _{DS} = -10 V; f = 1 MHz; V _{GS} = 0 V;	-	1900	-	pF
C _{oss}	output capacitance	T _j = 25 °C	-	275	-	pF
C _{rss}	reverse transfer capacitance		-	250	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = -10 V; I _D = -5.8 A; V _{GS} = -4.5 V;	-	6	-	ns
t _r	rise time	R _{G(ext)} = 5 Ω; T _j = 25 °C	-	23	-	ns
t _{d(off)}	turn-off delay time	1 1	-	46	-	ns
-(, t _f	fall time	1 1	-	31	-	ns
Source-drai	n diode	· · ·				
V _{SD}	source-drain voltage	I _S = -1.7 A; V _{GS} = 0 V; T _j = 25 °C	-	-0.7	-1.2	V
t _{rr}	reverse recovery time	I _S = -1.7 A; dI _S /dt = 100 A/µs;	-	26	-	ns
Q _r	recovered charge	V _{GS} = -4.5 V; V _{DS} = -10 V; T _j = 25 °C	-	10	-	nC
t _a	reverse recovery rise time	1 [-	6	-	ns
t _b	reverse recovery fall time	-	-	20	-	ns

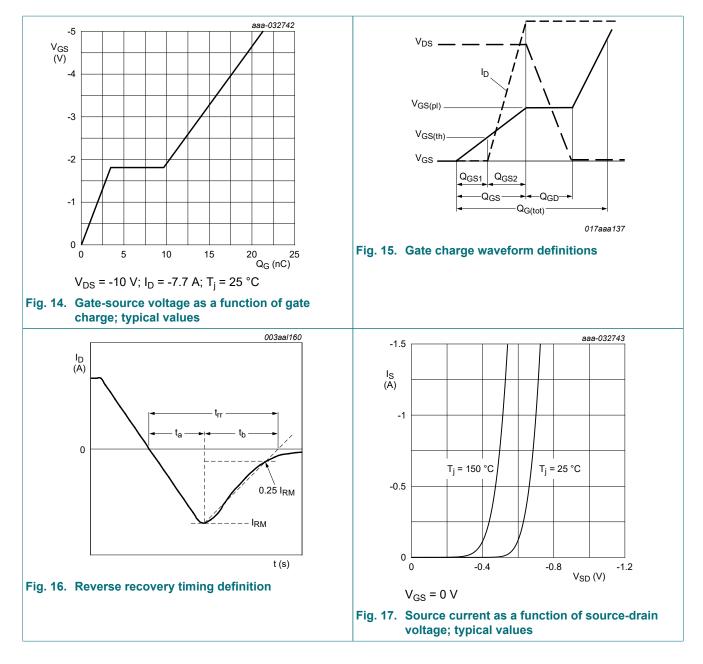
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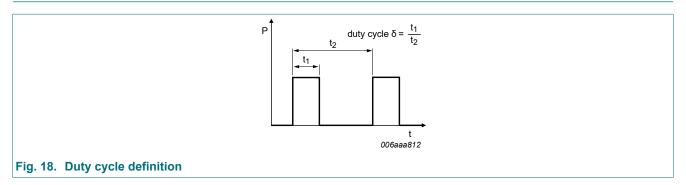
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20 V, P-channel Trench MOSFET



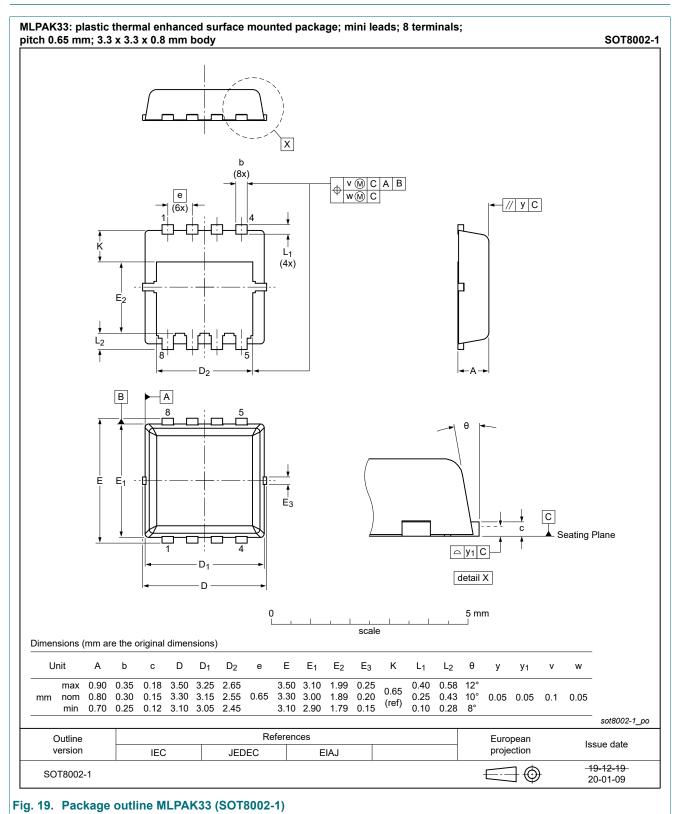
11. Test information



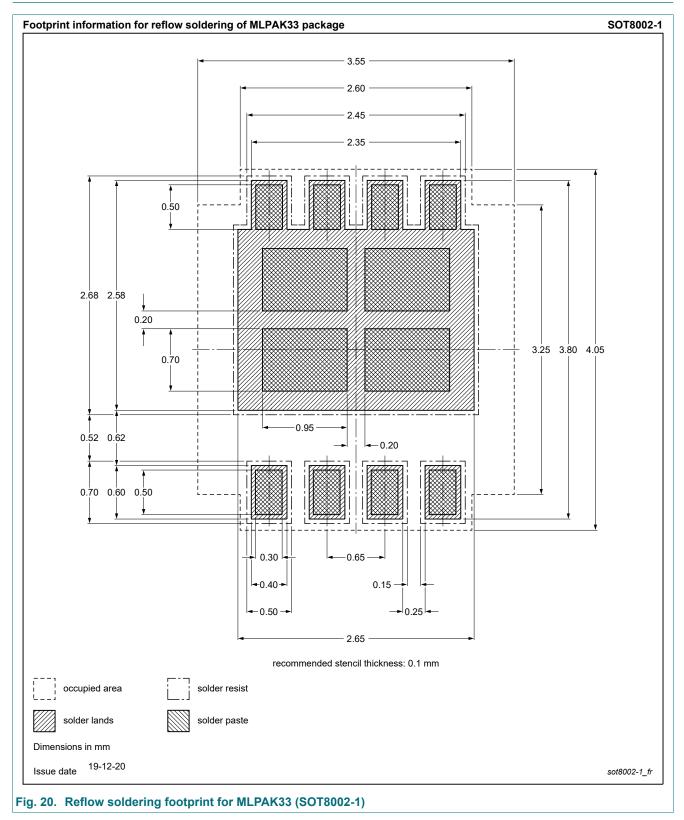
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12. Package outline



13. Soldering



14. Revision history

Table 8. Revision history						
Data sheet ID	Release date	Data sheet status	Change notice	Supersedes		
PXP020-20QX v.1	20210414	Product data sheet	-	-		

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15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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