

## DS90LV048A 3V LVDS Quad CMOS Differential Line Receiver

Check for Samples: [DS90LV048A](#)

### FEATURES

- >400 Mbps (200 MHz) Switching Rates
- Flow-Through Pinout Simplifies PCB Layout
- 150 ps Channel-to-Channel Skew (Typical)
- 100 ps Differential Skew (Typical)
- 2.7 ns Maximum Propagation Delay
- 3.3V Power Supply Design
- High Impedance LVDS Inputs on Power Down
- Low Power Design (40mW @ 3.3V Static)
- Interoperable with Existing 5V LVDS Drivers
- Accepts Small Swing (350 mV Typical) Differential Signal Levels
- Supports Open, Short and Terminated Input Fail-Safe
- 0V to -100mV Threshold Region
- Conforms to ANSI/TIA/EIA-644 Standard
- Industrial Temperature Operating Range (-40°C to +85°C)
- Available in SOIC and TSSOP Package

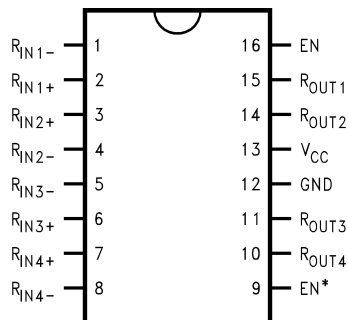
### DESCRIPTION

The DS90LV048A is a quad CMOS flow-through differential line receiver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 400 Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90LV048A accepts low voltage (350 mV typical) differential input signals and translates them to 3V CMOS output levels. The receiver supports a TRI-STATE function that may be used to multiplex outputs. The receiver also supports open, shorted and terminated (100Ω) input fail-safe. The receiver output will be HIGH for all fail-safe conditions. The DS90LV048A has a flow-through pinout for easy PCB layout.

The EN and EN\* inputs are ANDed together and control the TRI-STATE outputs. The enables are common to all four receivers. The DS90LV048A and companion LVDS line driver (eg. DS90LV047A) provide a new alternative to high power PECL/ECL devices for high speed point-to-point interface applications.

### Connection Diagram



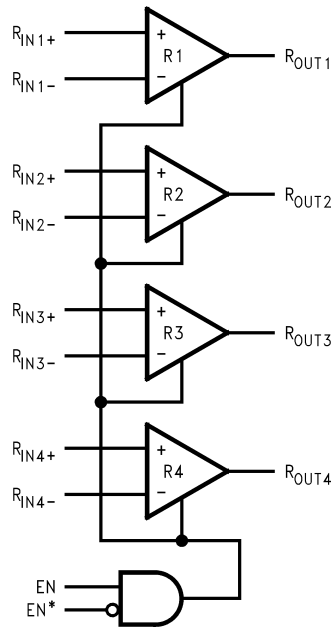
Order Number DS90LV048ATM, DS90LV048ATMTC  
D0016A, PW0016A Packages



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### Functional Diagram



**TRUTH TABLE**

ENABLES		INPUTS	OUTPUT
EN	EN*	R <sub>IN+</sub> – R <sub>IN-</sub>	R <sub>OUT</sub>
H	L or Open	$V_{ID} \geq 0V$	H
		$V_{ID} \leq -0.1V$	L
		Full Fail-safe OPEN/SHORT or Terminated	H
All other combinations of ENABLE inputs		X	Z



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)</sup>**

Supply Voltage ( $V_{CC}$ )	-0.3V to +4V	
Input Voltage ( $R_{IN+}$ , $R_{IN-}$ )	-0.3V to 3.9V	
Enable Input Voltage (EN, EN*)	-0.3V to ( $V_{CC} + 0.3V$ )	
Output Voltage ( $R_{OUT}$ )	-0.3V to ( $V_{CC} + 0.3V$ )	
Maximum Package Power Dissipation @ +25°C	D0016A Package	1025 mW
	PW0016A Package	866 mW
	Derate D0016A Package	8.2 mW/°C above +25°C
	Derate PW0016A Package	6.9 mW/°C above +25°C
Storage Temperature Range	-65°C to +150°C	
Lead Temperature Range Soldering	(4 sec.)	+260°C
Maximum Junction Temperature	+150°C	
ESD Rating <sup>(3)</sup>	(HBM, 1.5 k $\Omega$ , 100 pF)	$\geq 10$ kV
	(EIAJ, 0 $\Omega$ , 200 pF)	$\geq 1200$ V

- (1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be specified. They are not meant to imply that the devices should be operated at these limits. [ELECTRICAL CHARACTERISTICS](#) specifies conditions of device operation.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) ESD Rating:  
     HBM (1.5 k $\Omega$ , 100 pF)  $\geq 10$ kV  
     EIAJ (0 $\Omega$ , 200 pF)  $\geq 1200$ V

**RECOMMENDED OPERATING CONDITIONS**

	Min	Typ	Max	Units
Supply Voltage ( $V_{CC}$ )	+3.0	+3.3	+3.6	V
Receiver Input Voltage	GND		+3.0	V
Operating Free Air Temperature ( $T_A$ )	-40	25	+85	°C

## ELECTRICAL CHARACTERISTICS

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. <sup>(1)(2)</sup>

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
$V_{TH}$	Differential Input High Threshold	$V_{CM} = +1.2V, 0.05V, 2.95V^{(3)}$	$R_{IN+}$ $R_{IN-}$		-35	0	mV
$V_{TL}$	Differential Input Low Threshold			-100	-35		mV
VCMR	Common-Mode Voltage Range	$VID = 200mV$ pk to pk <sup>(4)</sup>		0.1		2.3	V
$I_{IN}$	Input Current	$V_{IN} = +2.8V$	$V_{CC} = 3.6V$ or $0V$	-10	$\pm 5$	+10	$\mu A$
		$V_{IN} = 0V$		-10	$\pm 1$	+10	$\mu A$
		$V_{IN} = +3.6V$		$V_{CC} = 0V$	-20	$\pm 1$	+20
$V_{OH}$	Output High Voltage	$I_{OH} = -0.4$ mA, $V_{ID} = +200$ mV	$R_{OUT}$	2.7	3.3		V
		$I_{OH} = -0.4$ mA, Input terminated		2.7	3.3		V
		$I_{OH} = -0.4$ mA, Input shorted		2.7	3.3		V
$V_{OL}$	Output Low Voltage	$I_{OL} = 2$ mA, $V_{ID} = -200$ mV			0.05	0.25	V
$I_{OS}$	Output Short Circuit Current	Enabled, $V_{OUT} = 0V^{(5)}$		-15	-47	-100	mA
$I_{OZ}$	Output TRI-STATE Current	Disabled, $V_{OUT} = 0V$ or $V_{CC}$		-10	$\pm 1$	+10	$\mu A$
$V_{IH}$	Input High Voltage		EN, EN*	2.0		$V_{CC}$	V
$V_{IL}$	Input Low Voltage			GND		0.8	V
$I_I$	Input Current	$V_{IN} = 0V$ or $V_{CC}$ . Other Input = $V_{CC}$ or GND		-10	$\pm 5$	+10	$\mu A$
$V_{CL}$	Input Clamp Voltage	$I_{CL} = -18$ mA		-1.5	-0.8		V
$I_{CC}$	No Load Supply Current Receivers Enabled	EN = $V_{CC}$ , Inputs Open	$V_{CC}$		9	15	mA
$I_{CCZ}$	No Load Supply Current Receivers Disabled	EN = GND, Inputs Open			1	5	mA

- (1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.
- (2) All typicals are given for:  $V_{CC} = +3.3V$ ,  $T_A = +25^\circ C$ .
- (3)  $V_{CC}$  is always higher than  $R_{IN+}$  and  $R_{IN-}$  voltage.  $R_{IN-}$  and  $R_{IN+}$  are allowed to have a voltage range  $-0.2V$  to  $V_{CC} - VID/2$ . However, to be compliant with AC specifications, the common voltage range is 0.1V to 2.3V
- (4) The VCMR range is reduced for larger VID. Example: if  $VID = 400mV$ , the VCMR is 0.2V to 2.2V. The fail-safe condition with inputs shorted is not supported over the common-mode range of 0V to 2.4V, but is supported only with inputs shorted and no external common-mode voltage applied. A VID up to  $V_{CC} - 0V$  may be applied to the  $R_{IN+}/R_{IN-}$  inputs with the Common-Mode voltage set to  $V_{CC}/2$ . Propagation delay and Differential Pulse skew decrease when VID is increased from 200mV to 400mV. Skew specifications apply for  $200mV \leq VID \leq 800mV$  over the common-mode range.
- (5) Output short circuit current ( $I_{OS}$ ) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.

## SWITCHING CHARACTERISTICS

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. <sup>(1)</sup><sup>(2)</sup><sup>(3)</sup><sup>(4)</sup>

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{PHLD}$	Differential Propagation Delay High to Low	$C_L = 15\text{ pF}$ $V_{ID} = 200\text{ mV}$ (Figure 1 and Figure 2)	1.2	2.0	2.7	ns
$t_{PLHD}$	Differential Propagation Delay Low to High		1.2	1.9	2.7	ns
$t_{SKD1}$	Differential Pulse Skew $ t_{PHLD} - t_{PLHD} $ <sup>(5)</sup>		0	0.1	0.4	ns
$t_{SKD2}$	Differential Channel-to-Channel Skew; same device <sup>(3)</sup>		0	0.15	0.5	ns
$t_{SKD3}$	Differential Part to Part Skew <sup>(4)</sup>				1.0	ns
$t_{SKD4}$	Differential Part to Part Skew <sup>(6)</sup>				1.5	ns
$t_{TLH}$	Rise Time	$R_L = 2\text{ k}\Omega$ $C_L = 15\text{ pF}$ (Figure 3 and Figure 4)		0.5	1.0	ns
$t_{THL}$	Fall Time			0.35	1.0	ns
$t_{PHZ}$	Disable Time High to Z	All Channels Switching		8	14	ns
$t_{PLZ}$	Disable Time Low to Z			8	14	ns
$t_{PZH}$	Enable Time Z to High			9	14	ns
$t_{PZL}$	Enable Time Z to Low			9	14	ns
$f_{MAX}$	Maximum Operating Frequency <sup>(7)</sup>		200	250		MHz

- (1) All typicals are given for:  $V_{CC} = +3.3\text{V}$ ,  $T_A = +25^\circ\text{C}$ .
- (2) Generator waveform for all tests unless otherwise specified:  $f = 1\text{ MHz}$ ,  $Z_O = 50\Omega$ ,  $t_r$  and  $t_f$  (0% to 100%)  $\leq 3\text{ ns}$  for  $R_{IN}$ .
- (3)  $t_{SKD2}$ , Channel-to-Channel Skew is defined as the difference between the propagation delay of one channel and that of the others on the same chip with any event on the inputs.
- (4)  $t_{SKD3}$ , part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same  $V_{CC}$ , and within  $5^\circ\text{C}$  of each other within the operating temperature range.
- (5)  $t_{SKD1}$  is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel
- (6)  $t_{SKD4}$ , part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution.  $t_{SKD4}$  is defined as  $|\text{Max}-\text{Min}|$  differential propagation delay.
- (7)  $f_{MAX}$  generator input conditions:  $t_r = t_f < 1\text{ ns}$  (0% to 100%), 50% duty cycle, differential (1.05V to 1.35V peak to peak). Output criteria: 60/40% duty cycle,  $V_{OL}$  (max 0.4V),  $V_{OH}$  (min 2.7V), Load = 15 pF (stray plus probes).

### PARAMETER MEASUREMENT INFORMATION

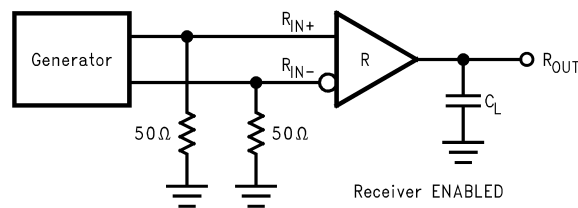


Figure 1. Receiver Propagation Delay and Transition Time Test Circuit

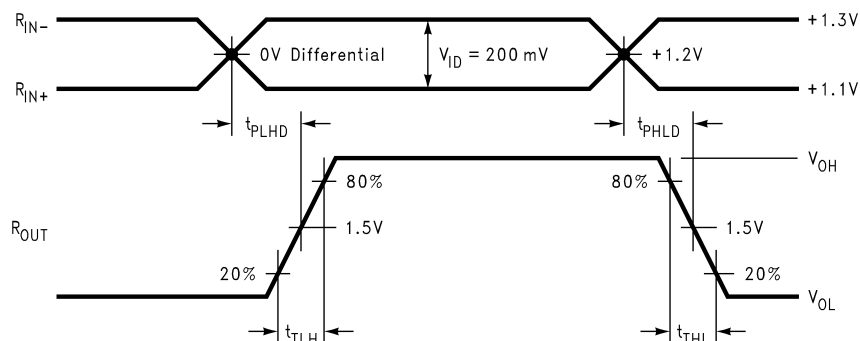
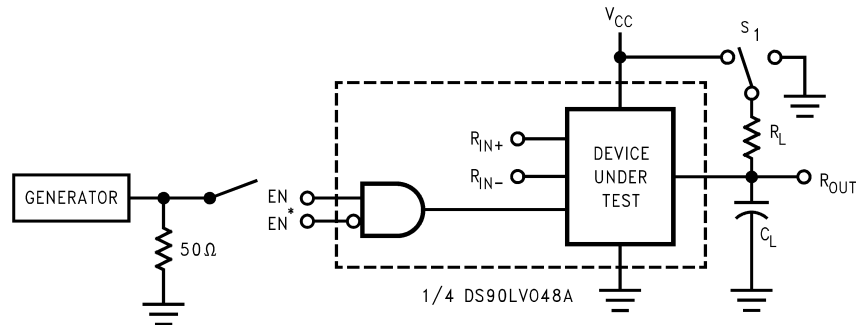


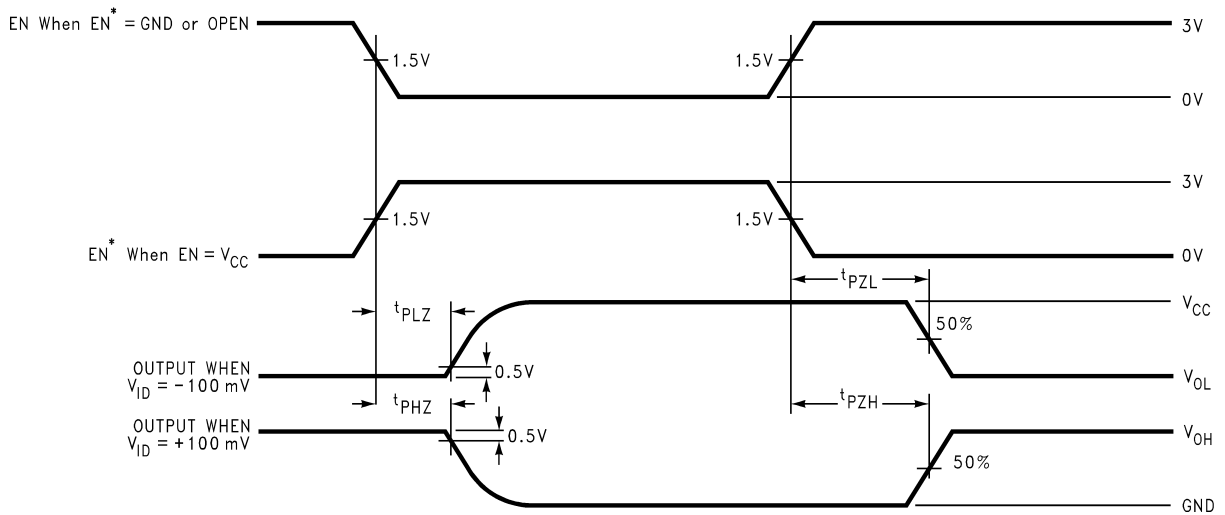
Figure 2. Receiver Propagation Delay and Transition Time Waveforms

**PARAMETER MEASUREMENT INFORMATION (continued)**



$C_L$  includes load and test jig capacitance.  
 $S_1 = V_{CC}$  for  $t_{PZL}$  and  $t_{PLZ}$  measurements.  
 $S_1 = GND$  for  $t_{PZH}$  and  $t_{PHZ}$  measurements.

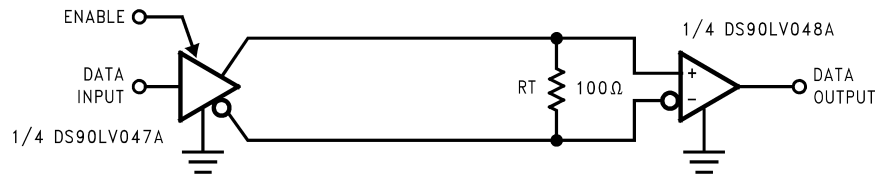
**Figure 3. Receiver TRI-STATE Delay Test Circuit**



**Figure 4. Receiver TRI-STATE Delay Waveforms**

**TYPICAL APPLICATION**

**Balanced System**



**Figure 5. Point-to-Point Application**

## APPLICATION INFORMATION

General application guidelines and hints for LVDS drivers and receivers may be found in the following application notes: LVDS Owner's Manual (lit #550062-002), AN-808 ([SNLA028](#)), AN-977 ([SNLA166](#)), AN-971 ([SNLA165](#)), AN-916 ([SNLA219](#)), AN-805 ([SNOA233](#)), AN-903 ([SNLA034](#)). The latest applications material is available on the web at: [www.ti.com](http://www.ti.com)

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in [Figure 5](#). This configuration provides a clean signaling environment for the fast edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω (selected to match the media), and is located as close to the receiver input pins as possible. The termination resistor converts the driver output (current mode) into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90LV048A differential line receiver is capable of detecting signals as low as 100mV, over a ±1V common-mode range centered around +1.2V. This is related to the driver offset voltage which is typically +1.2V. The driven signal is centered around this voltage and may shift ±1V around this center point. The ±1V shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common-mode effects of coupled noise, or a combination of the two. The AC parameters of both receiver input pins are optimized for a recommended operating input voltage range of 0V to +2.4V (measured from each pin to ground). The device will operate for receiver input voltages up to  $V_{CC}$ , but exceeding  $V_{CC}$  will turn on the ESD protection circuitry which will clamp the bus voltages.

The DS90LV048A has a flow-through pinout that allows for easy PCB layout. The LVDS signals on one side of the device easily allows for matching electrical lengths of the differential pair trace lines between the driver and the receiver as well as allowing the trace lines to be close together to couple noise as common-mode. Noise isolation is achieved with the LVDS signals on one side of the device and the TTL signals on the other side.

### Power Decoupling Recommendations

Bypass capacitors must be used on power pins. Use high frequency ceramic (surface mount is recommended) 0.1μF and 0.001μF capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin. Additional scattered capacitors over the printed circuit board will improve decoupling. Multiple vias should be used to connect the decoupling capacitors to the power planes. A 10μF (35V) or greater solid tantalum capacitor should be connected at the power entry point on the printed circuit board between the supply and ground.

### PC Board considerations

Use at least 4 PCB layers (top to bottom); LVDS signals, ground, power, TTL signals.

Isolate TTL signals from LVDS signals, otherwise the TTL may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by a power/ground plane(s)

Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

### Differential Traces

Use controlled impedance traces which match the differential impedance of your transmission medium (ie. cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs should be < 10mm long). This will help eliminate reflections and ensure noise is coupled as common-mode. In fact, we have seen that differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is much better with the closer traces. In addition, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result. (Note the velocity of propagation,  $v = c/\epsilon_r$  where  $c$  (the speed of light) = 0.2997mm/ps or 0.0118 in/ps). Do not rely solely on the autoroute function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number of vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

## Termination

Use a termination resistor which best matches the differential impedance or your transmission line. The resistor should be between 90Ω and 130Ω. Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work without resistor termination. Typically, connecting a single resistor across the pair at the receiver end will suffice.

Surface mount 1% to 2% resistors are best. PCB stubs, component lead, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be < 10mm (12mm MAX)

## Probing LVDS Transmission Lines

Always use high impedance (> 100kΩ), low capacitance (< 2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing will give deceiving results.

## Cables and Connectors, General Comments

When choosing cable and connectors for LVDS it is important to remember:

Use controlled impedance media. The cables and connectors you use should have a matched differential impedance of about 100Ω. They should not introduce major impedance discontinuities.

Balanced cables (e.g. twisted pair) are usually better than unbalanced cables (ribbon cable, simple coax.) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation a common-mode (not differential mode) noise which is rejected by the receiver.

For cable distances < 0.5M, most cables can be made to work effectively. For distances  $0.5M \leq d \leq 10M$ , CAT 3 (category 3) twisted pair cable works well, is readily available and relatively inexpensive.

## Threshold

The LVDS Standard (ANSI/TIA/EIA-644) specifies a maximum threshold of ±100mV for the LVDS receiver. The DS90LV048A supports an enhanced threshold region of -100mV to 0V. This is useful for fail-safe biasing. The threshold region is shown in the Voltage Transfer Curve (VTC) in [Figure 6](#). The typical DS90LV048A LVDS receiver switches at about -35mV. Note that with  $V_{ID} = 0V$ , the output will be in a HIGH state. With an external fail-safe bias of +25mV applied, the typical differential noise margin is now the difference from the switch point to the bias point. In the example below, this would be 60mV of Differential Noise Margin (+25mV - (-35mV)). With the enhanced threshold region of -100mV to 0V, this small external fail-safe biasing of +25mV (with respect to 0V) gives a DNM of a comfortable 60mV. With the standard threshold region of ±100mV, the external fail-safe biasing would need to be +25mV with respect to +100mV or +125mV, giving a DNM of 160mV which is stronger fail-safe biasing than is necessary for the DS90LV048A. If more DNM is required, then a stronger fail-safe bias point can be set by changing resistor values.



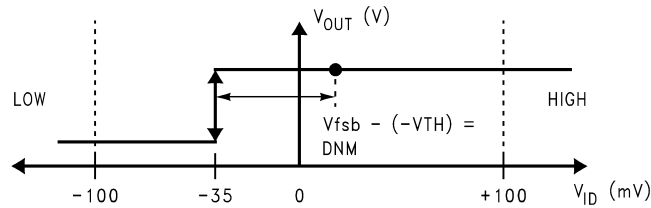


Figure 6. VTC of the DS90LV048A LVDS Receiver

### Fail-Safe Feature

The LVDS receiver is a high gain, high speed device that amplifies a small differential signal (20mV) to CMOS logic levels. Due to the high gain and tight threshold of the receiver, care should be taken to prevent noise from appearing as a valid signal.

The receiver's internal fail-safe circuitry is designed to source/sink a small amount of current, providing fail-safe protection (a stable known state of HIGH output voltage) for floating, terminated or shorted receiver inputs.

1. **Open Input Pins.** The DS90LV048A is a quad receiver device, and if an application requires only 1, 2 or 3 receivers, the unused channel(s) inputs should be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is biased by internal high value pull up and pull down resistors to set the output to a HIGH state. This internal circuitry will ensure a HIGH, stable output state for open inputs.
2. **Terminated Input.** If the driver is disconnected (cable unplugged), or if the driver is in a TRI-STATE or power-off condition, the receiver output will again be in a HIGH state, even with the end of cable 100Ω termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10mV of differential noise, the receiver may see the noise as a valid signal and switch. To insure that any noise is seen as common-mode and not differential, a balanced interconnect should be used. Twisted pair cable will offer better balance than flat ribbon cable.
3. **Shorted Inputs.** If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0V differential input voltage, the receiver output will remain in a HIGH state. Shorted input fail-safe is not supported across the common-mode range of the device (GND to 2.4V). It is only supported with inputs shorted and no external common-mode voltage applied.

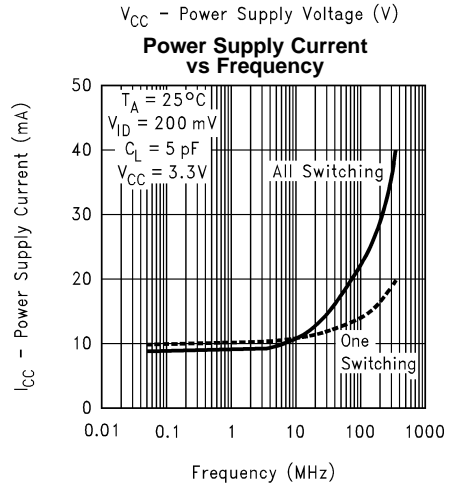
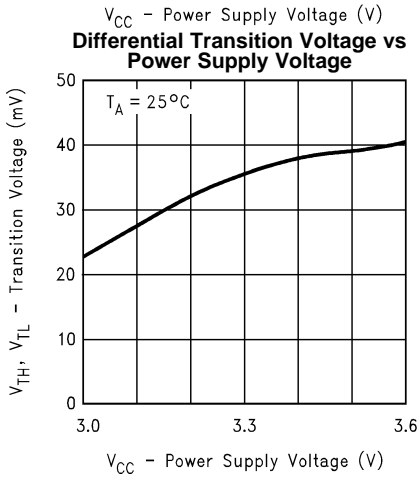
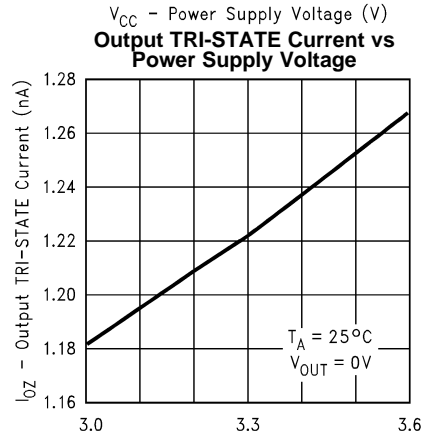
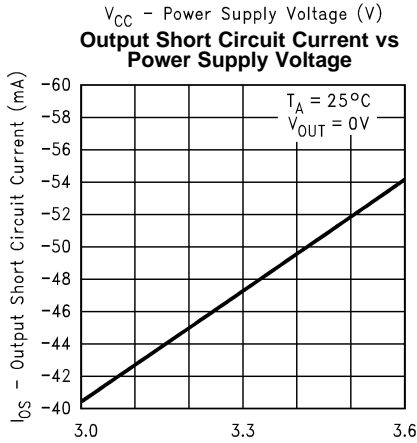
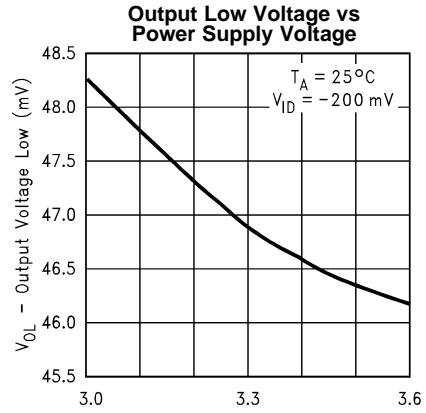
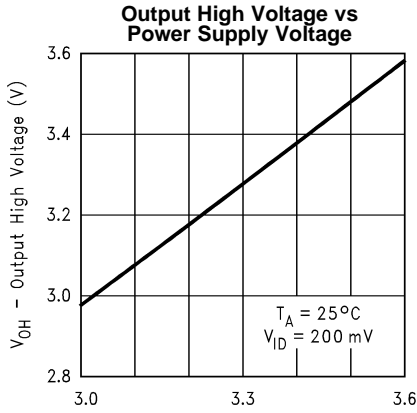
External lower value pull up and pull down resistors (for a stronger bias) may be used to boost fail-safe in the presence of higher noise levels. The pull up and pull down resistors should be in the 5kΩ to 15kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point should be set to approximately 1.2V (less than 1.75V) to be compatible with the internal circuitry.

Additional information on fail-safe biasing of LVDS devices may be found in AN-1194.

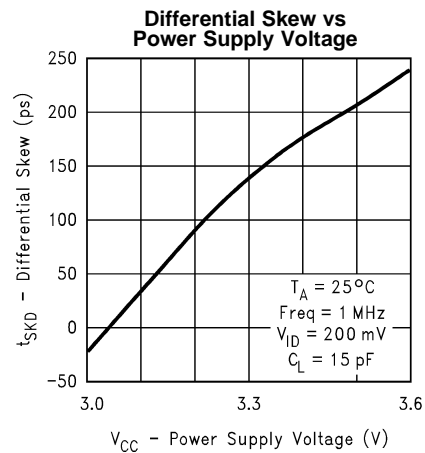
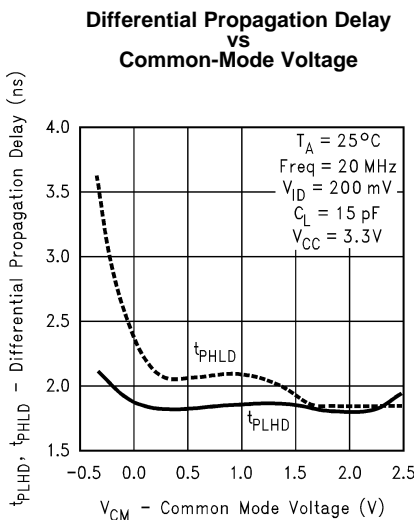
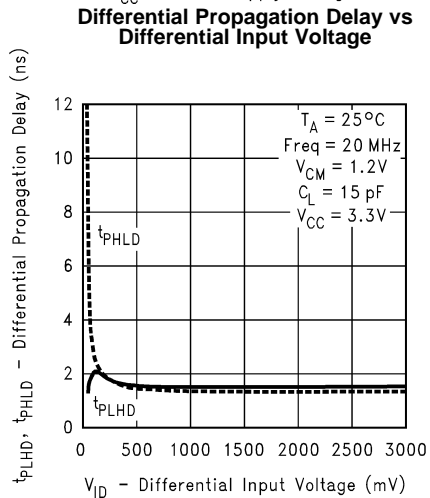
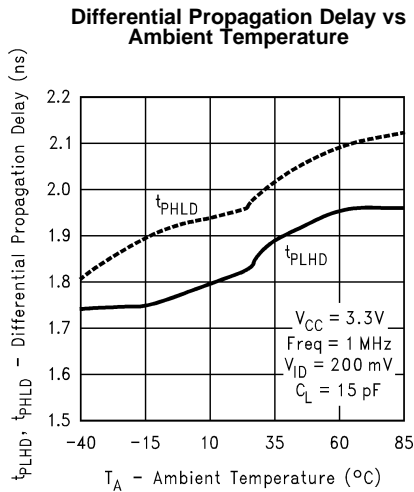
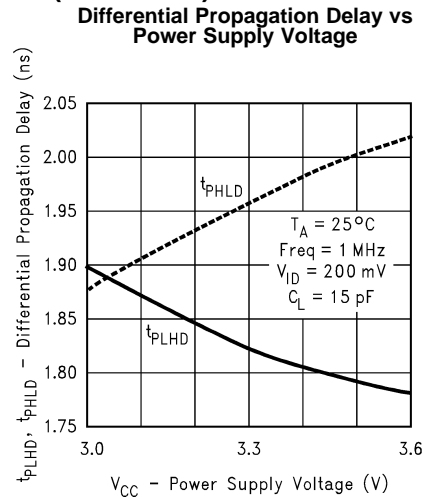
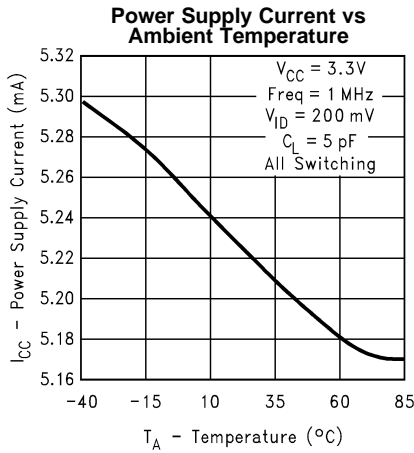
### PIN DESCRIPTIONS

Pin No.	Name	Description
2, 3, 6, 7	R <sub>IN+</sub>	Non-inverting receiver input pin
1, 4, 5, 8	R <sub>IN-</sub>	Inverting receiver input pin
10, 11, 14, 15	R <sub>OUT</sub>	Receiver output pin
16	EN	Receiver enable pin: When EN is low, the receiver is disabled. When EN is high and EN* is low or open, the receiver is enabled. If both EN and EN* are open circuit, then the receiver is disabled.
9	EN*	Receiver enable pin: When EN* is high, the receiver is disabled. When EN* is low or open and EN is high, the receiver is enabled. If both EN and EN* are open circuit, then the receiver is disabled.
13	V <sub>CC</sub>	Power supply pin, +3.3V ± 0.3V
12	GND	Ground pin

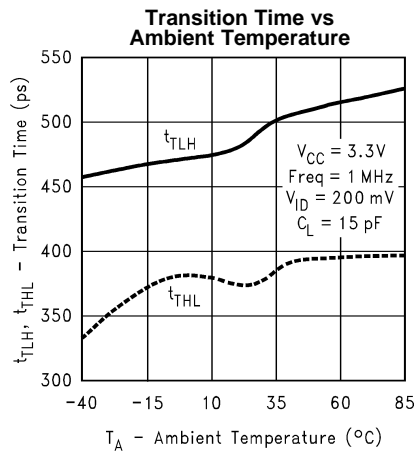
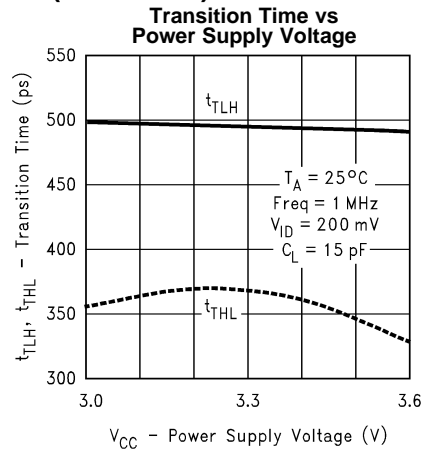
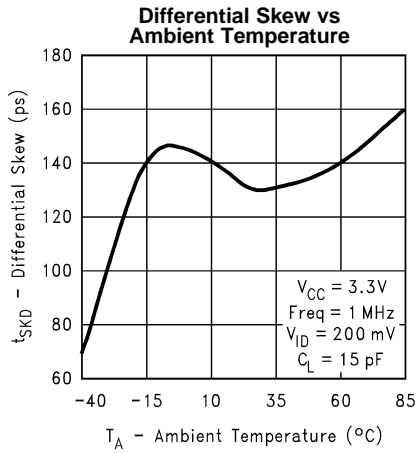
**TYPICAL PERFORMANCE CURVES**



**TYPICAL PERFORMANCE CURVES (continued)**



**TYPICAL PERFORMANCE CURVES (continued)**



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**REVISION HISTORY**

<b>Changes from Revision A (April 2013) to Revision B</b>	<b>Page</b>
<hr/> <ul style="list-style-type: none"><li>• Changed layout of National Data Sheet to TI format .....</li></ul>	<hr/> <a href="#">12</a>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90LV048ATM	NRND	SOIC	D	16	48	TBD	Call TI	Call TI	-40 to 85	DS90LV048A TM	
DS90LV048ATM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS90LV048A TM	<b>Samples</b>
DS90LV048ATMTC	NRND	TSSOP	PW	16	92	TBD	Call TI	Call TI	-40 to 85	DS90LV 048AT	
DS90LV048ATMTC/NOPB	ACTIVE	TSSOP	PW	16	92	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS90LV 048AT	<b>Samples</b>
DS90LV048ATMTCX	NRND	TSSOP	PW	16	2500	TBD	Call TI	Call TI	-40 to 85	DS90LV 048AT	
DS90LV048ATMTCX/NOPB	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS90LV 048AT	<b>Samples</b>
DS90LV048ATMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS90LV048A TM	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90LV048ATMTCX	TSSOP	PW	16	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
DS90LV048ATMTCX/NO PB	TSSOP	PW	16	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
DS90LV048ATMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90LV048ATMTCX	TSSOP	PW	16	2500	367.0	367.0	35.0
DS90LV048ATMTCX/NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0
DS90LV048ATMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

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