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NTE74LS42
Integrated Circuit
TTL – 4–Line–to–10–Line BDC–to–Decimal Decoder

Description:

The NTE74LS42 is a monolithic BCD–to–Decimal decoder in a 16–Lead plastic DIP type package that consists of eight inverters and ten four–input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The NTE74LS42 BCD–to–Decimal decoder features inputs and outputs that are compatible with most TTL and other saturated low–level logic circuits. DC noise margins are typically one volt.

Features:

- All Outputs are High for Invalid Input Conditions
- Diode–Clamped Inputs
- Also for Application as:
  4–Line–to–16–Line Decoder
  3–Line–to–8–Line Decoder

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High–Level Output Current	I_{OH}	–	–	–400	μA
Low–Level Output Current	I_{OL}	–	–	8	mA
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}			2	–	–	V
Low Level Input Voltage	V_{IL}			–	–	0.8	V
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −18mA		–	–	−1.5	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX, I_{OH} = −400μA		2.7	3.5		V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX	I_{OL} = 4mA	–	0.25	0.4	V
			I_{OL} = 8mA	–	0.35	0.5	V
Input Current	I_I	V_{CC} = MAX, V_I = 7V		–	–	0.1	mA
High Level Input Current	I_{IH}	V_{CC} = MAX, V_I = 2.7V		–	–	20	μA
Low Level Input Current	I_{IL}	V_{CC} = MAX, V_I = 0.4V		–	–	−0.4	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 4		−20	–	−100	mA
Supply Current	I_{CC}	V_{CC} = MAX, Note 5		–	7	13	mA

Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 3. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 4. Not more than one output should be shorted at a time, and duration of the short−circuit should not exceed one second.

Note 5. I_{CC} is measured with all outputs open and inputs grounded.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time (From A, B, C, or D input Through 2 Levels of Logic)	t_{PHL}	R_L = 2kΩ, C_L = 15pF	–	15	25	ns
Propagation Delay Time (From A, B, C, or D input Through 3 Levels of Logic)	t_{PHL}		–	20	30	ns
Propagation Delay Time (From A, B, C, or D input Through 2 Levels of Logic)	t_{PLH}		–	15	25	ns
Propagation Delay Time (From A, B, C, or D input Through 3 Levels of Logic)	t_{PLH}		–	20	30	ns

Function Tables:

No.	BCD Input				Decimal Output									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
Invalid	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Level, L = LOW Level

Pin Connection Diagram