LPC5500 MCU Series

NXP Communicator

LPC553x/S3x MCU Family

This Arm® Cortex®-M33 MCU brings new levels of analog integration and high system reliability to the LPC5500 series

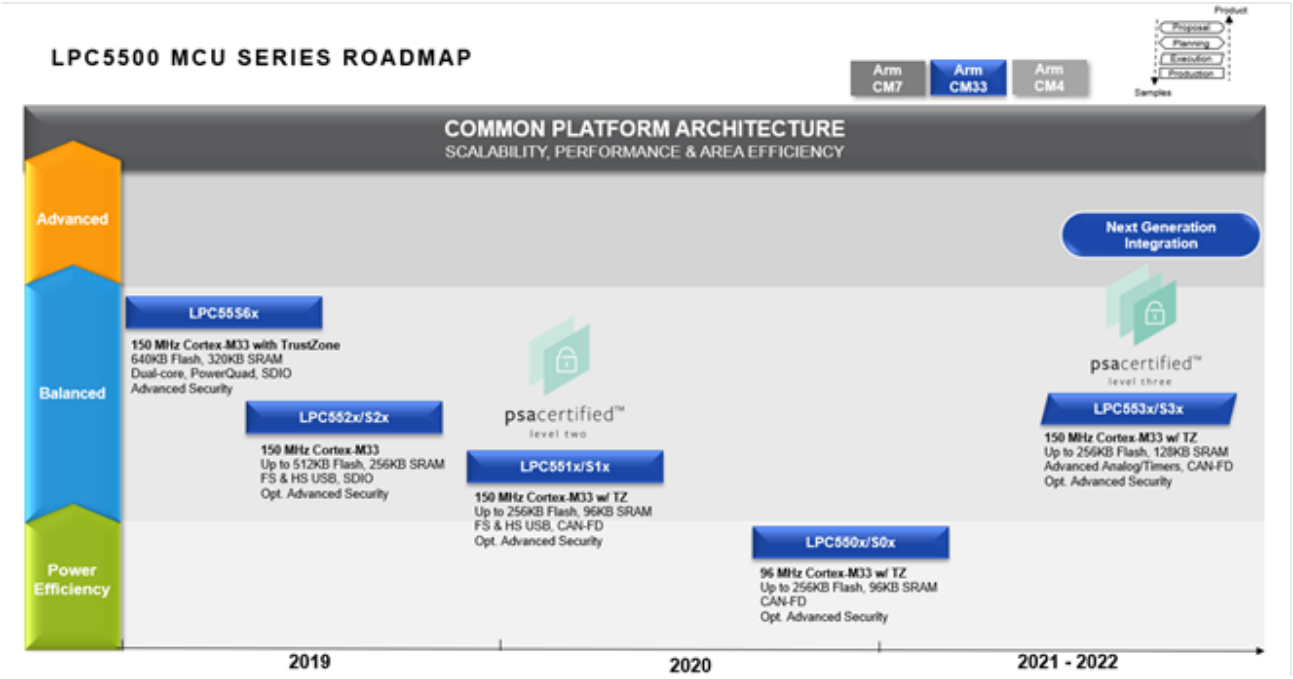
Featuring the LPC553x Series

Communicator Date: March 2022

Global Full Market Launch Date: April 4, 2022

LPC5500 MCU Series | Introduction

The LPC5500 MCU Series leverages the Arm® Cortex®-M33 technology, combining significant product architecture enhancements and greater integration over previous generations; offering dramatic power consumption improvements and advanced security features including SRAM PUF based root of trust and provisioning, real-time execution from encrypted images (internal flash), and asset protection with Arm TrustZone®-M. In addition, the LPC5500 MCU series provides a comprehensive offering and several scalability options, all of which benefit from 40-nm cost advantages, broad scalable packages and memory options, as well as a comprehensive enablement including the MCUXpresso Software and Tools ecosystem and fully featured development boards.



LPC553x/S3x MCU Family | Overview

The LPC553x/S3x MCU family further expands the world's first general purpose Cortex-M33-based MCU series, offering significant performance enhancement, all on-chip RAM with Parity or ECC, renewed security features and precision analog additions, leveraging the cost-effective 40-nm NVM process technology.

The LPC553x/S3x family includes a proprietary DSP accelerator offering 10x clock cycle reduction, bringing significant signal processing efficiency gains.

The LPC553x/S3x MCU family will be launched in two phases. Phase one will focus on the launch of the LPC553x series and EVK which will launch April 4, 2022. While phase two will focus on the launch of the LPC55S3x series and EVK which will launch later in Q4 2022. This communicator will cover the features of the entire LPC553x/S3x family, however the stocking table and enablement sections will focus primarily on phase one which includes the LPC553x launch.

LPC553x/S3x MCU Family | Key Messages

An Arm® Cortex®-M33 MCU family

- High-efficient 40-nm flash technology with 112kB Parity + 16kB ECC RAM
- Over 600 Core Mark (4.17 /MHz running in Flash with Cache) and active power as low as 57 uA/MHz
- Enhanced safety and security with TrustZone-M
- System Integration with DSP acceleration –Cordic engine providing >3.5X improvement for Motor Control Applications
- High-precision & fast ADCs, instrumentation class OpAmp with programmable gain up to 64x, and DAC
- Motor Control PWM and Quad Encoder/Decoder
- Comprehensive enablement with MCUXpresso Ecosystem

LPC553x/S3x MCU Family | Target Applications

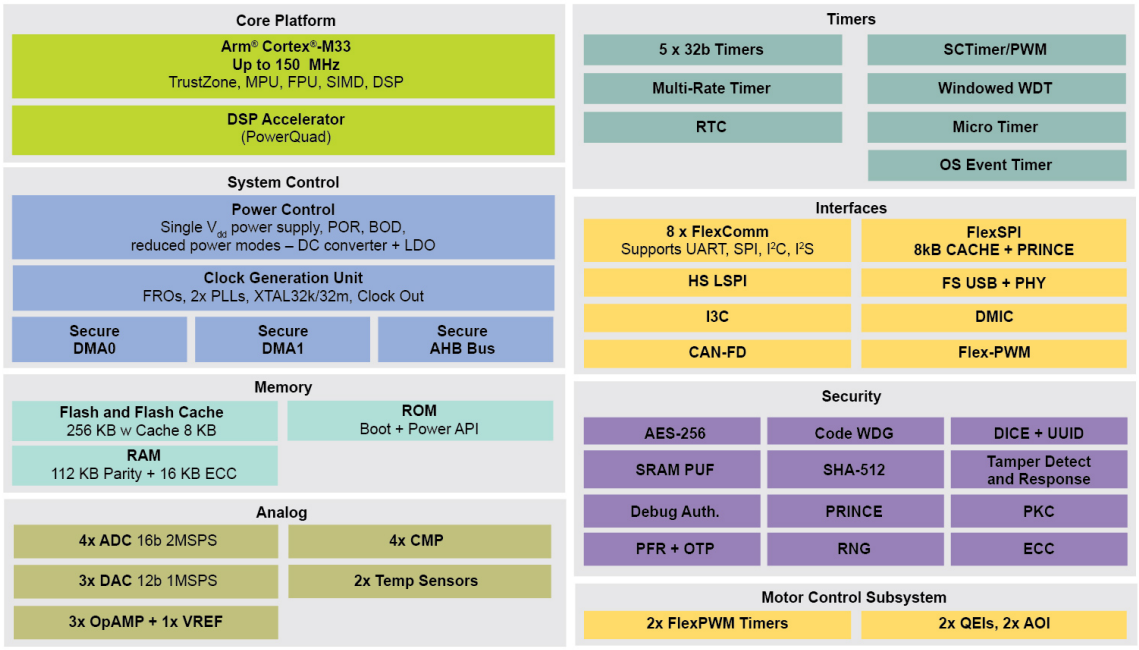
- **Industrial & Building Automation**
  - Motor Control
  - Power Inverters

- **Consumer Products**
  - Power Tools
  - Appliances

- **Smart Home**
  - Secure/Biometric Access Control
  - Security Systems

LPC553x/S3x MCU Family | Specifications

Block Diagram



Key Features

Core Platform

- Cortex-M33 processor up to 150 MHz
- Integrated digital signal processing (DSP) instructions.
- Floating Point Unit (FPU) and Memory Protection Unit (MPU)
- Arm Cortex M33 built-in Nested Vectored Interrupt Controller (NVIC)
- Non-maskable Interrupt (NMI) input with a selection of sources
- Serial Wire Debug with eight breakpoints and four watch points. Includes Serial Wire Output for enhanced debug capabilities and trace (ETM)
- System tick timer

On-chip Memory

- Up to 256 KB on-chip flash program memory with flash accelerator, 8 KB Low-power Cache and 512 byte page erase and write.
- Up to 128 KB total SRAM consisting of 16 KB SRAM on Code Bus, 112 KB SRAM on System Bus (112 KB is contiguous).

112 kB has Parity and 16 kB ECC SRAM

Serial interfaces

- FlexComm Interface contains up to nine serial peripherals. Each FlexComm Interface can be selected by software to be a USART, SPI, I2C, and I2S interface
- I2C-bus interfaces support Fast-mode and Fast-mode Plus with data rates of up to 1Mbit/s and with multiple address recognition and monitor mode
- High-Speed SPI (Flexcomm 8, 50 MHz for both controller and responder).
- A digital microphone interface supporting up to two channels with associated decimators and Voice Activation Detect. One pair of channels can be streamed directly to I2S. The DMIC supports DMA.
- One I3C bus interface.
- One CAN FD module with dedicated DMA controller.
- USB 2.0 full speed host/device controller with on-chip PHY and dedicated DMA controller supporting crystal-less operation in device mode.

Digital peripherals

- DMA0 controller with 52 channels and up to 52 programmable triggers, able to access all memories and DMA-capable peripherals
- DMA1 controller with 16 channels and up to 25 programmable triggers, able to access all memories and DMA-capable peripherals
- CRC engine block
- Up to 66 General-Purpose Input/Output (GPIO) pins
- GPIO registers are located on the AHB for fast access
- Up to eight GPIOs can be selected as Pin Interrupts (PINT), triggered by rising, falling or both input edges
- Two GPIO Grouped Interrupts (GINT) enable an interrupt based on a logical (AND/OR) combination of input states
- I/O pin configuration with support for up to 16 function options
- FlexSPI flash interface for external flash with 8 kB cache and dynamic decryption for execute-in-place and supports DMA.
- Two AOI (AND/OR/Invert) combinatorial logic modules with dedicated set of input and output signals.

Analog peripherals

- Four single-ended 16-bit or two-differential input ADCs (selectable) with sample rate of 2.0 Msamples/sec in 16-bit mode and 3.13 Msamples/sec in 12-bit mode. Eight differential channel pairs (or 16 single-ended channels), with multiple internal and external trigger inputs. The ADC supports four simultaneous conversions, under the control of two independent sequences.
- Integrated temperature sensor connected to both ADCs
- One Comparator in always-on domain with up to four input pins and internal reference voltage. Can be used as a wake-up source from low-power modes.
- Three High-Speed Comparators with up to five input pins and internal reference voltage.
- Three 12-bit DACs with sample rates of up to 1.0 Msamples/sec
- Three OpAmps with programmable VREF
- Programmable VREF

Timers

- Five 32-bit standard general purpose asynchronous timers/counters, which support up to four capture inputs and four compare outputs. Specific timer events can be selected to generate DMA requests
- One SCTimer/PWM with 8 inputs and 10 output functions (including 16 capture and match registers). Inputs and outputs can be routed to/from external pins and internally to/from selected peripherals. Internally, the SCTimer/PWM supports 16 match/captures, 16 events, and 32 states
- 32-bit Real-time clock (RTC) with 1 s resolution running in the always-on power domain. A timer in the RTC can be used for wake-up from all low power modes including deep power-down, with 1 ms resolution
- Multiple-channel multi-rate 24-bit timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates
- Windowed Watchdog Timer (WWDT) with FRO 1 MHZ as clock source
- Micro-Tick Timer running from the watchdog oscillator can be used to wake-up the device from sleep and deep-sleep modes
- Code Watchdog for detecting code flow integrity
- 42-bit free running OS Timer as continuous time-base for the system, available in any reduced power modes

Clock generation

- Internal Free Running Oscillator (FRO)
- 32 kHz Internal Free Running Oscillator FRO

- Internal low power oscillator (FRO 1 MHz)
- Crystal oscillator with an operating frequency of 12 MHz to 32 MHz. Option for external clock input (bypass mode) for clock frequencies of up to 25 MHz
- Crystal oscillator with 32.768 kHz operating frequency
- PLL0 and PLL1 allows CPU operation up to the maximum CPU rate without the need for a high-frequency external clock
- Clock output function with divider to monitor internal clocks
- Frequency measurement unit for measuring the frequency of any on-chip or off-chip clock signal
- Each crystal oscillator has one embedded capacitor bank, where each can be used as an integrated load capacitor for the crystal oscillators

Power-saving modes

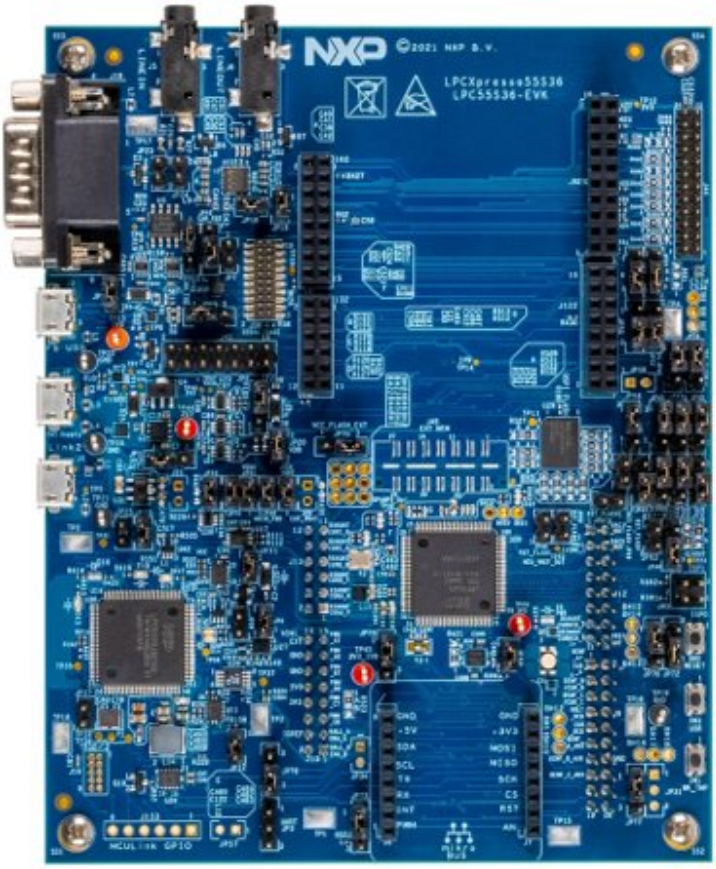
- Integrated Power Management Unit (PMU) to minimize power consumption
- Low power modes: Sleep, Deep-sleep with RAM retention, power-down with RAM retention and CPU retention, and deep power-down with RAM retention.
- Configurable wake-up options from peripheral interrupts
- The Micro-Tick Timer running from the watchdog oscillator, and the Real-Time Clock (RTC) running from the 32.678 kHz clock, can be used to wake up the device from sleep, deep-sleep, power-down, and deep power-down modes
- Power-On Reset (POR)
- Brown-Out-Detect (BOD) for external VDD_MAIN and internal VDD_CORE with separate thresholds for interrupt and forced reset

Additional information

- Operating from internal DC-DC converter or selectable LDO such that DC-DC converter can be bypassed.
- Single power supply 1.8 V to 3.6 V
- Two Main IO supplies (VDDIO_1: 1.8 V to 3.6 V, VDDIO_2: 1.08 v to 3.6 V).
- Separate VBAT supply 1.71 V to 3.6 V.
- JTAG boundary scan supported
- Operating temperature range -40 °C to +105 °C
- Available in HLQFP100, HTQFP64 and HVQFN48 packages

Enablement: Development Boards

LPC5536-EVK Board



The LPC5536-EVK development board provides the ideal platform for evaluation of and development with the LPC553x MCU based on the Arm® Cortex®-M33 architecture. The board includes a high-performance onboard debug probe and accelerometer, with several options for adding off-the-shelf add-on boards for networking, sensors, displays, and other interfaces.

The LPC5536-EVK is fully supported by the MCUXpresso suite of tools, which provides device drivers, middleware and examples to allow rapid development, plus configuration tools and an optional free IDE. Please refer to the LPCXpresso55S36 when searching for MCUXpresso SDK support. MCUXpresso software is compatible with tools from popular tool vendors such as Arm and IAR, and the LPCXpresso55S36 may also be used with the popular debug probes available from SEGGER and P&E Micro.

Features

- LPC5536JBD100 Cortex-M33 microcontroller running at up to 150 MHz
- NXP TJA1044GTJ High-Speed CAN Transceiver
- Stereo audio codec
- Support direct connection to FRDM-MC-LVPMSM: NXP® Freedom Development Platform for Low-Voltage, 3-Phase PMSM Motor Control
- Arduino and MikroEletronika click expansion options
- On-board debug probe with:
  - CMSIS-DAP and J-Link options
  - USB to SPI/I2C and UART bridge
  - On board power measurement
- PCB layout, schematic and board files available

Enablement: Software

- Integrated Development Environments (IDE)
  - MCUXpresso IDE
  - IAR® Embedded Workbench
  - Arm KEIL®
- MCUXpresso Software Development Kit (SDK)
  - Extensive suite of robust peripheral drivers, stacks, and middleware
  - Includes software examples demonstrating use of peripheral drivers and middleware
- MCUXpresso Config Tools
  - Includes pins, clocks, and peripheral tools for generation of MCUXpresso SDK code

Suggested Stocking, Timing, and Attach Products

The silicon part numbers, as well as the board are part of the Distributor PriceBook now.

LPC553x HLQFP100 and HTQFP64 are orderable now and shipment starts early May 2022.

LPC5536-EVK is orderable now and shipment starts early May 2022.

LPC553x HVQFN48 is orderable now and shipment starts mid June 2022.

Export compliance and additional information can be found in the Excel stocking files attached.

The below tables represent the suggested parts to stock for the launch.

Part Numbers

PN	DBC	Flash	SRAM	Suggested Resale for 10Ku	MOQ	Suggested Stocking	Order Open Date	Shipment Date	Package Type
LPC5534JBD100E		128 KB	80 KB		90	360	Now	May 2022	HLQFP100
LPC5534JBD64E		128 KB	80 KB		160	320	Now	May 2022	HTQFP64
LPC5534JHI48/00E		128 KB	80 KB		260	520	Now	June 2022	HVQFN48
LPC5536JBD100E		256 KB	128 KB		90	360	Now	May 2022	HLQFP100
LPC5536JBD64E		256 KB	128 KB		160	320	Now	May 2022	HTQFP64
LPC5536JHI48/00E		256 KB	128 KB		260	520	Now	June 2022	HVQFN48

All of the above part numbers are in single tray packing for initial launch stocking (with letter 'E' at end). For mass production which requires larger quantity at a later time, we will provide multi-tray (with letter 'K' at end) and Tape & Reel packing (with letter 'Y' at end) which have a higher MOQ.

Development Tools

PN	DBC	Flash	SRAM	Suggested Resale for 10Ku	MOQ	Suggested Stocking	Order Open Date	Shipment Date	Package Type
LPC5536-EVK					1	75	Now	May 2022	

**Below S parts and EVK will be available in Q4 2022.*

PN	DBC	Flash	SRAM	Resale for 10Ku	MOQ	Suggested Stocking	Open Date	Shipment Date	Package Type
LPC55**S**36JBD100E*		256 KB	128 KB		90				HLQFP100
LPC55**S**36JHI48/00E*		256 KB	128 KB		260				HVQFN48
LPC55**S**36-EVK*					1				

Available Documentation and Useful Links

NXP LPC MCUs landing page:
http://www.nxp.com/products/microcontrollers-and-processors/arm-processors/lpc-cortex-m-mcus:LPC-ARM-CORTEX-M-MCUS

LPC5500 Series landing page:
https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processors-and-mcus/lpc-cortex-m-mcus/lpc5500-series-cortex-m33-mcus:LPC5500_SERIES

LPC553x/S3x landing page:
www.nxp.com/LPC553x page will be live at launch

LPC553x/S3x MCU Family Fact Sheet:
On distributor marketing assets site and will be available on landing page at launch

LPC5536 Development Board landing page:
www.nxp.com/LPC55S36-EVK page will be live at launch

MCUXpresso Software and Tools for Arm® Cortex®-M cores:
www.nxp.com/products/software-and-tools/run-time-software/mcuxpresso-software-and-tools:MCUXPRESSO

MCUXpresso SDK Builder:
https://mcuxpresso.nxp.com/en/builder?hw=LPCXpresso55S36

LPC553x Fighting Guide:
https://www.nxp.com/webapp/Download?colCode=LPC553X-FIGHTING-GUIDE-DISTY

LPC553x 6 Pack:
https://www.nxp.com/webapp/Download?colCode=LPC553X-MCU-FAMILY-6-PACK-DISTY

Marketing Assets for the LPC553x/S3x can be found here:
https://nxp1.sharepoint.com/teams/ext131/distimkt/SitePages/Home.aspx

This communicator is available on NXP DistyNet:
https://www.nxp.com/app-distynet/distynet:DISTYNET#/

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