LAN8710A/LAN8710Ai

Small Footprint MII/RMII 10/100 Ethernet Transceiver with HP Auto-MDIX and flexPWR® Technology

PRODUCT FEATURES

Datasheet

Highlights

- Single-Chip Ethernet Physical Layer Transceiver (PHY)
- Comprehensive flexPWR® Technology
  - Flexible Power Management Architecture
  - LVCMOS Variable I/O voltage range: +1.6V to +3.6V
  - Integrated 1.2V regulator with disable feature
- HP Auto-MDIX support
- Small footprint 32-pin QFN lead-free RoHS compliant package (5 x 5 x 0.9mm height)

Target Applications

- Set-Top Boxes
- Networked Printers and Servers
- Test Instrumentation
- LAN on Motherboard
- Embedded Telecom Applications
- Video Record/Playback Systems
- Cable Modems/Routers
- DSL Modems/Routers
- Digital Video Recorders
- IP and Video Phones
- Wireless Access Points
- Digital Televisions
- Digital Media Adaptors/Servers
- Gaming Consoles
- POE Applications (Refer to SMSC Application Note 17.18)

Key Benefits

- High-Performance 10/100 Ethernet Transceiver
  - Compliant with IEEE802.3/802.3u (Fast Ethernet)
  - Compliant with ISO 802-3/IEEE 802.3 (10BASE-T)
  - Loop-back modes
  - Auto-negotiation
  - Automatic polarity detection and correction
  - Link status change wake-up detection
  - Vendor specific register functions
  - Supports both MII and the reduced pin count RMII interfaces
- Power and I/Os
  - Various low power modes
  - Integrated power-on reset circuit
  - Two status LED outputs
  - Latch-Up Performance Exceeds 150mA per EIA/JESD 78, Class II
  - May be used with a single 3.3V supply
- Additional Features
  - Ability to use a low cost 25Mhz crystal for reduced BOM
- Packaging
  - 32-pin QFN (5x5 mm) Lead-Free RoHS Compliant package with MII and RMII
- Environmental
  - Extended commercial temperature range (0°C to +85°C)
  - Industrial temperature range version available (-40°C to +85°C)

Order Numbers:

LAN8710Ai-EZK for 32-pin QFN lead-free RoHS compliant package (-40 to +85°C temp)

LAN8710Ai-EZK-TR for 32-pin QFN lead-free RoHS compliant package (-40 to +85°C temp)

LAN8710A-EZC for 32-pin QFN lead-free RoHS compliant package (0 to +85°C temp)

LAN8710A-EZC-TR for 32-pin QFN lead-free RoHS compliant package (0 to +85°C temp)

TR indicates tape & reel option. Reel size is 4,000.

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

Please contact your SMSC sales representative for additional documentation related to this product such as application notes, anomaly sheets, and design guidelines.

Chapter 1 Introduction

1.1 General Terms and Conventions

The following is list of the general terms used throughout this document:

BYTE	8-bits
FIFO	First In First Out buffer; often used for elasticity buffer
MAC	Media Access Controller
MII	Media Independent Interface
RMII™	Reduced Media Independent Interface™
N/A	Not Applicable
X	Indicates that a logic state is “don’t care” or undefined.
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
SMI	Serial Management Interface

1.2 General Description

The LAN8710A/LAN8710Ai is a low-power 10BASE-T/100BASE-TX physical layer (PHY) transceiver with variable I/O voltage that is compliant with the IEEE 802.3-2005 standards.

The LAN8710A/LAN8710Ai supports communication with an Ethernet MAC via a standard MII (IEEE 802.3u)/RMII interface. It contains a full-duplex 10-BASE-T/100BASE-TX transceiver and supports 10Mbps (10BASE-T) and 100Mbps (100BASE-TX) operation. The LAN8710A/LAN8710Ai implements auto-negotiation to automatically determine the best possible speed and duplex mode of operation. HP Auto-MDIX support allows the use of direct connect or cross-over LAN cables.

The LAN8710A/LAN8710Ai supports both IEEE 802.3-2005 compliant and vendor-specific register functions. However, no register access is required for operation. The initial configuration may be selected via the configuration pins as described in Section 3.7, "Configuration Straps," on page 36. Register-selectable configuration options may be used to further define the functionality of the transceiver.

Per IEEE 802.3-2005 standards, all digital interface pins are tolerant to 3.6V. The device can be configured to operate on a single 3.3V supply utilizing an integrated 3.3V to 1.2V linear regulator. The linear regulator may be optionally disabled, allowing usage of a high efficiency external regulator for lower system power dissipation.

The LAN8710A/LAN8710Ai is available in both extended commercial and industrial temperature range versions. A typical system application is shown in Figure 1.1.

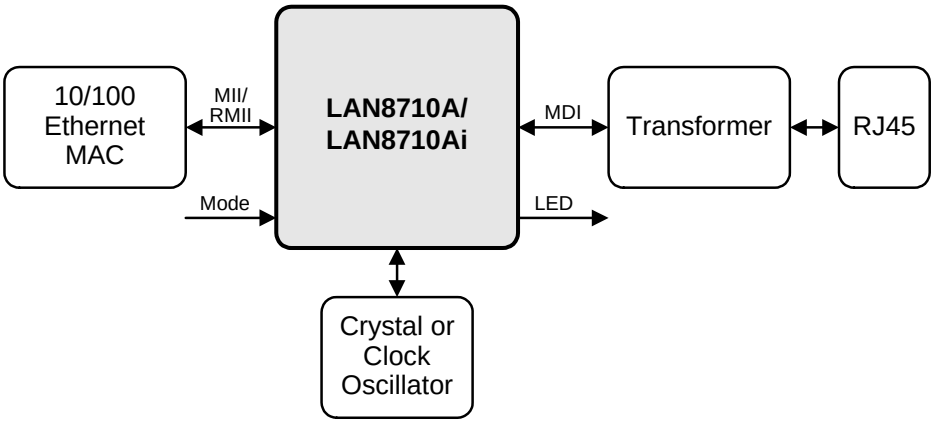


Figure 1.1 System Block Diagram

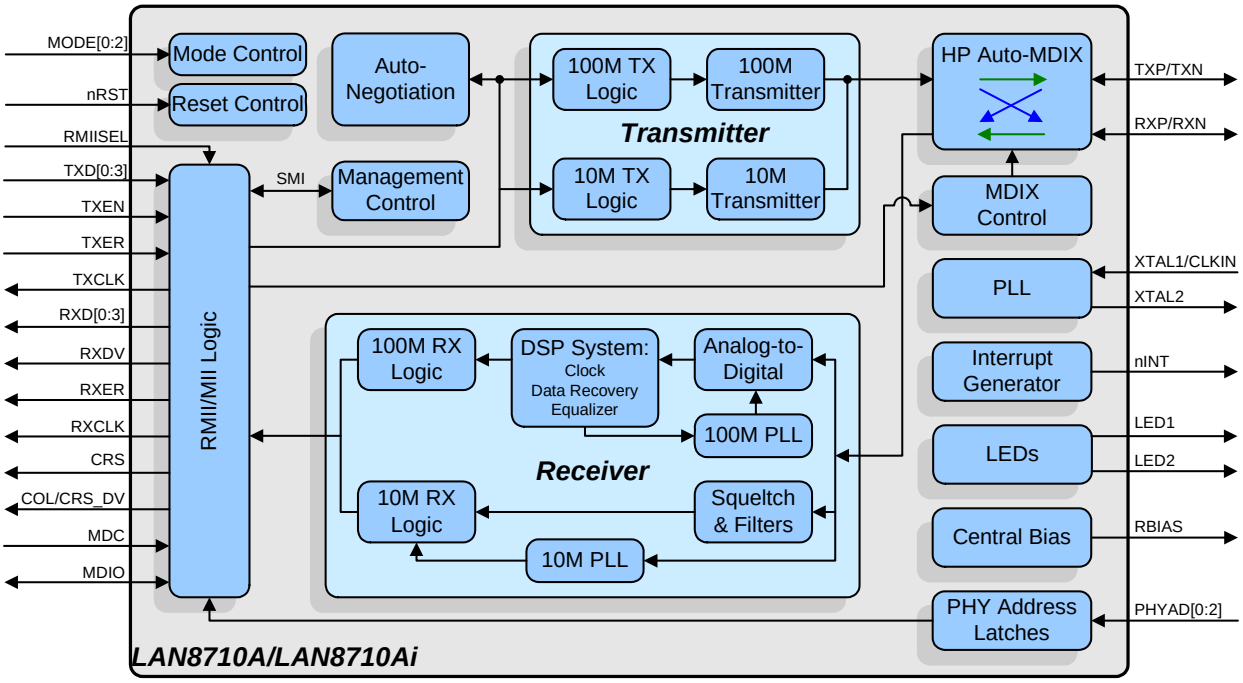
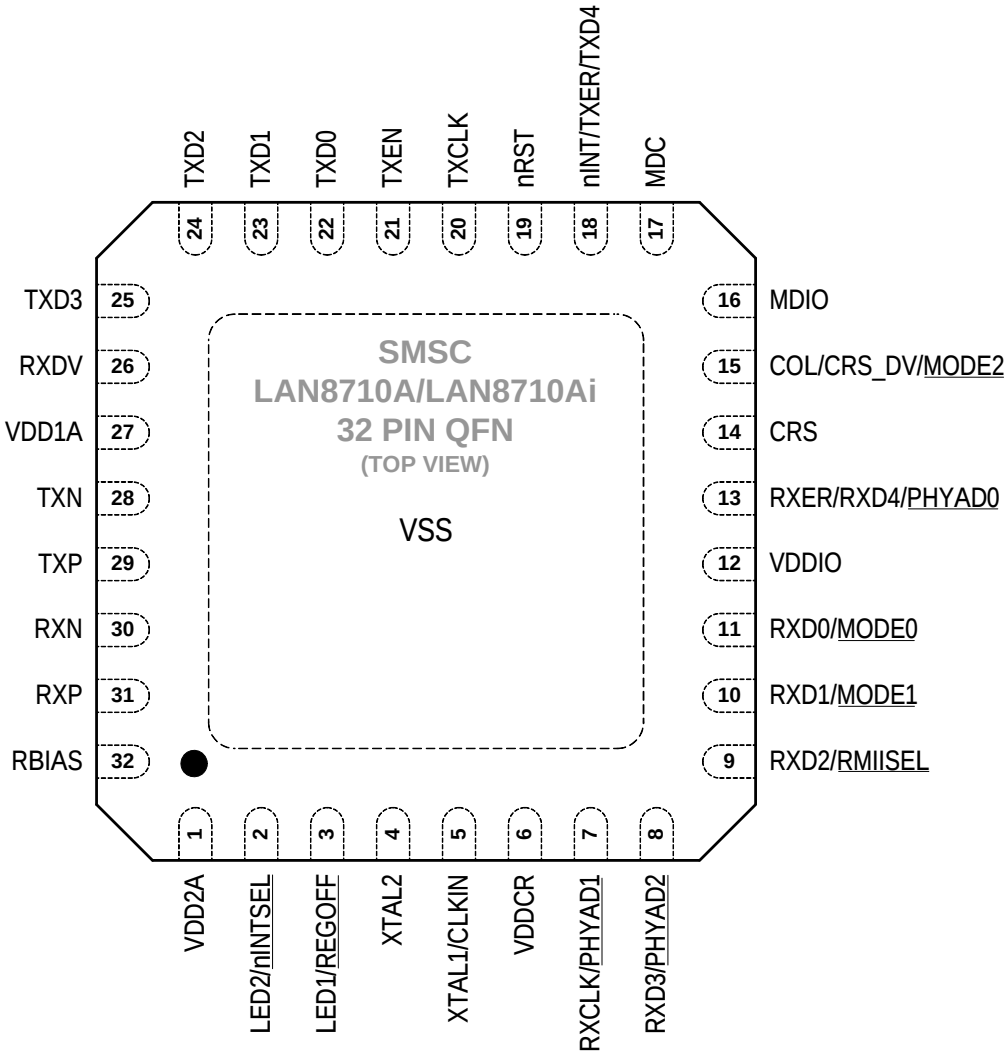


Figure 1.2 Architectural Overview

Chapter 2 Pin Description and Configuration



NOTE: Exposed pad (VSS) on bottom of package must be connected to ground

Figure 2.1 32-QFN Pin Assignments (TOP VIEW)

Note: When a lower case “n” is used at the beginning of the signal name, it indicates that the signal is active low. For example, nRST indicates that the reset signal is active low.

Note: The buffer type for each signal is indicated in the BUFFER TYPE column. A description of the buffer types is provided in Section 2.2.

Table 2.1 MII/RMII Signals

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Transmit Data 0	TXD0	VIS	The MAC transmits data to the transceiver using this signal in all modes.
1	Transmit Data 1	TXD1	VIS	The MAC transmits data to the transceiver using this signal in all modes.
1	Transmit Data 2 (MII Mode)	TXD2	VIS	The MAC transmits data to the transceiver using this signal in MII Mode. **Note:** This signal must be grounded in RMII Mode.
1	Transmit Data 3 (MII Mode)	TXD3	VIS	The MAC transmits data to the transceiver using this signal in MII Mode. **Note:** This signal must be grounded in RMII Mode.
1	Interrupt Output	nINT	VO8	Active low interrupt output. Place an external resistor pull-up to VDDIO. **Note:** Refer to Section 3.6, "Interrupt Management," on page 34 for additional details on device interrupts. **Note:** Refer to Section 3.8.1.2, "nINTSEL and LED2 Polarity Selection," on page 39 for details on how the nINTSEL configuration strap is used to determine the function of this pin.
	Transmit Error (MII Mode)	TXER	VIS (PU)	When driven high, the 4B/5B encode process substitutes the Transmit Error code-group (/H/) for the encoded data word. This input is ignored in the 10BASE-T mode of operation.
	Transmit Data 4 (MII Mode)	TXD4	VIS (PU)	In Symbol Interface (5B Decoding) mode, this signal becomes the MII Transmit Data 4 line (the MSB of the 5-bit symbol code-group). **Note:** This signal is not used in RMII Mode.
1	Transmit Enable	TXEN	VIS (PD)	Indicates that valid transmission data is present on TXD[3:0]. In RMII Mode, only TXD[1:0] provide valid data.
1	Transmit Clock (MII Mode)	TXCLK	VO8	Used to latch data from the MAC into the transceiver. ▪ MII (100BASE-TX): 25MHz ▪ MII (10BASE-T): 2.5MHz **Note:** This signal is not used in RMII Mode.

Table 2.1 MII/RMII Signals (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Receive Data 0	RXD0	VO8	Bit 0 of the 4 (2 in RMII Mode) data bits that are sent by the transceiver on the receive path.
	PHY Operating Mode 0 Configuration Strap	MODE0	VIS (PU)	Combined with MODE1 and MODE2, this configuration strap sets the default PHY mode. See Note 2.1 for more information on configuration straps. **Note:** Refer to Section 3.7.2, "MODE[2:0]: Mode Configuration," on page 36 for additional details.
1	Receive Data 1	RXD1	VO8	Bit 1 of the 4 (2 in RMII Mode) data bits that are sent by the transceiver on the receive path.
	PHY Operating Mode 1 Configuration Strap	MODE1	VIS (PU)	Combined with MODE0 and MODE2, this configuration strap sets the default PHY mode. See Note 2.1 for more information on configuration straps. **Note:** Refer to Section 3.7.2, "MODE[2:0]: Mode Configuration," on page 36 for additional details.
1	Receive Data 2 (MII Mode)	RXD2	VO8	Bit 2 of the 4 (in MII Mode) data bits that are sent by the transceiver on the receive path. **Note:** This signal is not used in RMII Mode.
	MII/RMII Mode Select Configuration Strap	RMIISEL	VIS (PD)	This configuration strap selects the MII or RMII mode of operation. When strapped low to VSS, MII Mode is selected. When strapped high to VDDIO RMII Mode is selected. See Note 2.1 for more information on configuration straps. **Note:** Refer to Section 3.7.3, "RMIISEL: MII/RMII Mode Configuration," on page 37 for additional details.
1	Receive Data 3 (MII Mode)	RXD3	VO8	Bit 3 of the 4 (in MII Mode) data bits that are sent by the transceiver on the receive path. **Note:** This signal is not used in RMII Mode.
	PHY Address 2 Configuration Strap	PHYAD2	VIS (PD)	Combined with PHYAD0 and PHYAD1, this configuration strap sets the transceiver's SMI address. See Note 2.1 for more information on configuration straps. **Note:** Refer to Section 3.7.1, "PHYAD[2:0]: PHY Address Configuration," on page 36 for additional information.

Table 2.1 MII/RMII Signals (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Receive Error	RXER	VO8	This signal is asserted to indicate that an error was detected somewhere in the frame presently being transferred from the transceiver. **Note:** This signal is optional in RMII Mode.
	Receive Data 4 (MII Mode)	RXD4	VO8	In Symbol Interface (5B Decoding) mode, this signal is the MII Receive Data 4 signal, the MSB of the received 5-bit symbol code-group. **Note:** Unless configured to the Symbol Interface mode, this pin functions as RXER.
	PHY Address 0 Configuration Strap	PHYAD0	VIS (PD)	Combined with PHYAD1 and PHYAD2, this configuration strap sets the transceiver's SMI address. See Note 2.1 for more information on configuration straps. **Note:** Refer to Section 3.7.1, "PHYAD[2:0]: PHY Address Configuration," on page 36 for additional information.
1	Receive Clock (MII Mode)	RXCLK	VO8	In MII mode, this pin is the receive clock output. ▪ MII (100BASE-TX): 25MHz ▪ MII (10BASE-T): 2.5MHz
1	PHY Address 1 Configuration Strap	PHYAD1	VIS (PD)	Combined with PHYAD0 and PHYAD2, this configuration strap sets the transceiver's SMI address. See Note 2.1 for more information on configuration straps. **Note:** Refer to Section 3.7.1, "PHYAD[2:0]: PHY Address Configuration," on page 36 for additional information.
1	Receive Data Valid	RXDV	VO8	Indicates that recovered and decoded data is available on the RXD pins.

Table 2.1 MII/RMII Signals (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Carrier Sense / Receive Data Valid (RMII Mode)	CRS_DV	VO8	This signal is asserted to indicate the receive medium is non-idle in RMII Mode. When a 10BASE-T packet is received, CRS_DV is asserted, but RXD[1:0] is held low until the SFD byte (10101011) is received. **Note:** Per the RMII standard, transmitted data is not looped back onto the receive data pins in 10BASE-T half-duplex mode.
	Collision Detect (MII Mode)	COL	VO8	This signal is asserted to indicate detection of a collision condition in MII Mode.
	PHY Operating Mode 2 Configuration Strap	MODE2	VIS (PU)	Combined with MODE0 and MODE1, this configuration strap sets the default PHY mode. See Note 2.1 for more information on configuration straps. **Note:** Refer to Section 3.7.2, "MODE[2:0]: Mode Configuration," on page 36 for additional details.
1	Carrier Sense (MII Mode)	CRS	VO8 (PD)	This signal indicates detection of a carrier in MII Mode.

Note 2.1 Configuration strap values are latched on power-on reset and system reset. Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load. Refer to Section 3.7, "Configuration Straps," on page 36 for additional information.

Table 2.2 LED Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	LED 1	LED1	O12	Link activity LED Indication. This pin is driven active when a valid link is detected and blinks when activity is detected. **Note:** Refer to Section 3.8.1, "LEDs," on page 39 for additional LED information.
	Regulator Off Configuration Strap	REGOFF	IS (PD)	This configuration strap is used to disable the internal 1.2V regulator. When the regulator is disabled, external 1.2V must be supplied to VDDCR. ▪ When REGOFF is pulled high to VDD2A with an external resistor, the internal regulator is disabled. ▪ When REGOFF is floating or pulled low, the internal regulator is enabled (default). See Note 2.2 for more information on configuration straps. **Note:** Refer to Section 3.7.4, "REGOFF: Internal +1.2V Regulator Configuration," on page 38 for additional details.

Table 2.2 LED Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
	LED 2	LED2	O12	Link Speed LED Indication. This pin is driven active when the operating speed is 100Mbps. It is inactive when the operating speed is 10Mbps or during line isolation. **Note:** Refer to Section 3.8.1, "LEDs," on page 39 for additional LED information.
1	nINT/TXER/ TXD4 Function Select Configuration Strap	nINTSEL	IS (PU)	This configuration strap selects the mode of the nINT/TXER/TXD4 pin. ▪ When nINTSEL is floated or pulled to VDD2A, nINT is selected for operation on the nINT/TXER/TXD4 pin (default). ▪ When nINTSEL is pulled low to VSS, TXER/TXD4 is selected for operation on the nINT/TXER/TXD4 pin. See Note 2.2 for more information on configuration straps. **Note:** Refer to See Section 3.8.1.2, "nINTSEL and LED2 Polarity Selection," on page 39 for additional information.

Note 2.2 Configuration strap values are latched on power-on reset and system reset. Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load. Refer to Section 3.7, "Configuration Straps," on page 36 for additional information.

Table 2.3 Serial Management Interface (SMI) Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	SMI Data Input/Output	MDIO	VIS/ VOD8	Serial Management Interface data input/output
1	SMI Clock	MDC	VIS	Serial Management Interface clock

Table 2.4 Ethernet Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Ethernet TX/RX Positive Channel 1	TXP	AIO	Transmit/Receive Positive Channel 1
1	Ethernet TX/RX Negative Channel 1	TXN	AIO	Transmit/Receive Negative Channel 1

Table 2.4 Ethernet Pins (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Ethernet TX/RX Positive Channel 2	RXP	AIO	Transmit/Receive Positive Channel 2
1	Ethernet TX/RX Negative Channel 2	RXN	AIO	Transmit/Receive Negative Channel 2

Table 2.5 Miscellaneous Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	External Crystal Input	XTAL1	ICLK	External crystal input
	External Clock Input	CLKIN	ICLK	Single-ended clock oscillator input. **Note:** When using a single ended clock oscillator, XTAL2 should be left unconnected.
1	External Crystal Output	XTAL2	OCLK	External crystal output
1	External Reset	nRST	VIS (PU)	System reset. This signal is active low.

Table 2.6 Analog Reference Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	External 1% Bias Resistor Input	RBIAS	AI	This pin requires connection of a 12.1k ohm (1%) resistor to ground. Refer to the LAN8710A/LAN8710Ai reference schematic for connection information. **Note:** The nominal voltage is 1.2V and the resistor will dissipate approximately 1mW of power.

Table 2.7 Power Pins

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	+1.6V to +3.6V Variable I/O Power	VDDIO	P	+1.6V to +3.6V variable I/O power Refer to the LAN8710A/LAN8710Ai reference schematic for connection information.
1	+1.2V Digital Core Power Supply	VDDCR	P	Supplied by the on-chip regulator unless configured for regulator off mode via the REGOFF configuration strap. Refer to the LAN8710A/LAN8710Ai reference schematic for connection information. **Note:** 1 uF and 470 pF decoupling capacitors in parallel to ground should be used on this pin.
1	+3.3V Channel 1 Analog Port Power	VDD1A	P	+3.3V Analog Port Power to Channel 1 Refer to the LAN8710A/LAN8710Ai reference schematic for connection information.
1	+3.3V Channel 2 Analog Port Power	VDD2A	P	+3.3V Analog Port Power to Channel 2 and the internal regulator. Refer to the LAN8710A/LAN8710Ai reference schematic for connection information.
1	Ground	VSS	P	Common ground. This exposed pad must be connected to the ground plane with a via array.

2.1 Pin Assignments

Table 2.8 32-QFN Package Pin Assignments

PIN NUM	PIN NAME	PIN NUM	PIN NAME
1	VDD2A	17	MDC
2	LED2/nINTSEL	18	nINT/TXER/TXD4
3	LED1/REGOFF	19	nRST
4	XTAL2	20	TXCLK
5	XTAL1/CLKIN	21	TXEN
6	VDDCR	22	TXD0
7	RXCLK/PHYAD1	23	TXD1
8	RXD3/PHYAD2	24	TXD2
9	RXD2/RMIISEL	25	TXD3
10	RXD1/MODE1	26	RXDV
11	RXD0/MODE0	27	VDD1A
12	VDDIO	28	TXN
13	RXER/RXD4/PHYAD0	29	TXP
14	CRS	30	RXN
15	COL/CRS_DV/MODE2	31	RXP
16	MDIO	32	RBIAS