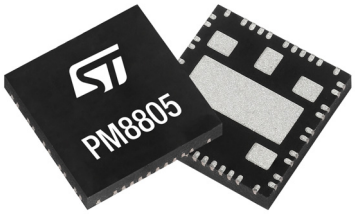
PM8805

IEEE 802.3bt PoE-PD interface with embedded dual active bridge

Datasheet - Production data



VFQFPN43 8x8mm exposed pad

Features

- Dual active bridge, hot swap MOSFETand PoE-PD interface in a system-in-package
- 100 V N-ch MOSFETs with 0.2 Ω total path resistance for each active bridge.
- 100 V, 0.1 Ω high-side N-ch hot swap MOSFET
- PoE-PD single-signature interface compliant with IEEE 802.3bt / at / af
- Supports 4-pair PoE applications
- Supports 12 V auxiliary sources
- Identifies which kind of PSE (standard or legacy) is connected with and provides successful IEEE802.3bt / at / af classification indication as a combination of the T0, T1 and T2 signals (open drain)
- Smart operational modes
- Programmable classification current with 3.3 ms delay.
- Optional Autoclass feature
- Advanced energy-saving MPS timings
- Two-step hot swap current protection: DC with 1 ms delay and short-circuit with 10 us delay.
- Controlled pre-charge of the output capacitor
- PGD signal (open drain) to enable an external PWM controller.
- Thermal shutdown protection

Applications

- High power wireless data systems
- Security cameras
- Access points
- Public information displays
- PoE lighting systems

Description

The PM8805 is a system-in-package for smart power supply of Power over Ethernet (PoE) Powered Devices (PD) and it is applicable for power level up to 99.9 W.

It embeds: two active bridges and their driving circuitry, a charge pump to drive the high-side MOSFETs, the hot swap MOSFET and the interface compliant with IEEE 802.3bt.

The device performs the physical layer classification, providing the indication of successful PSE type identification. A 4-pair PSE is identified and the information is available by a dedicated matrix of Tx signals.

The device works with power either from the Ethernet cable or from an external power source such as a wall adapter, with possible prevalence of the auxiliary source with respect to the PoE.

The PM8805 is suitable to build the interface section of PoE switch mode power supplies targeting the highest conversion efficiency. It provides a PGD signal that can be used to enable a PWM controller, a DC-DC converter or an LED driver.

Table 1. Device summary

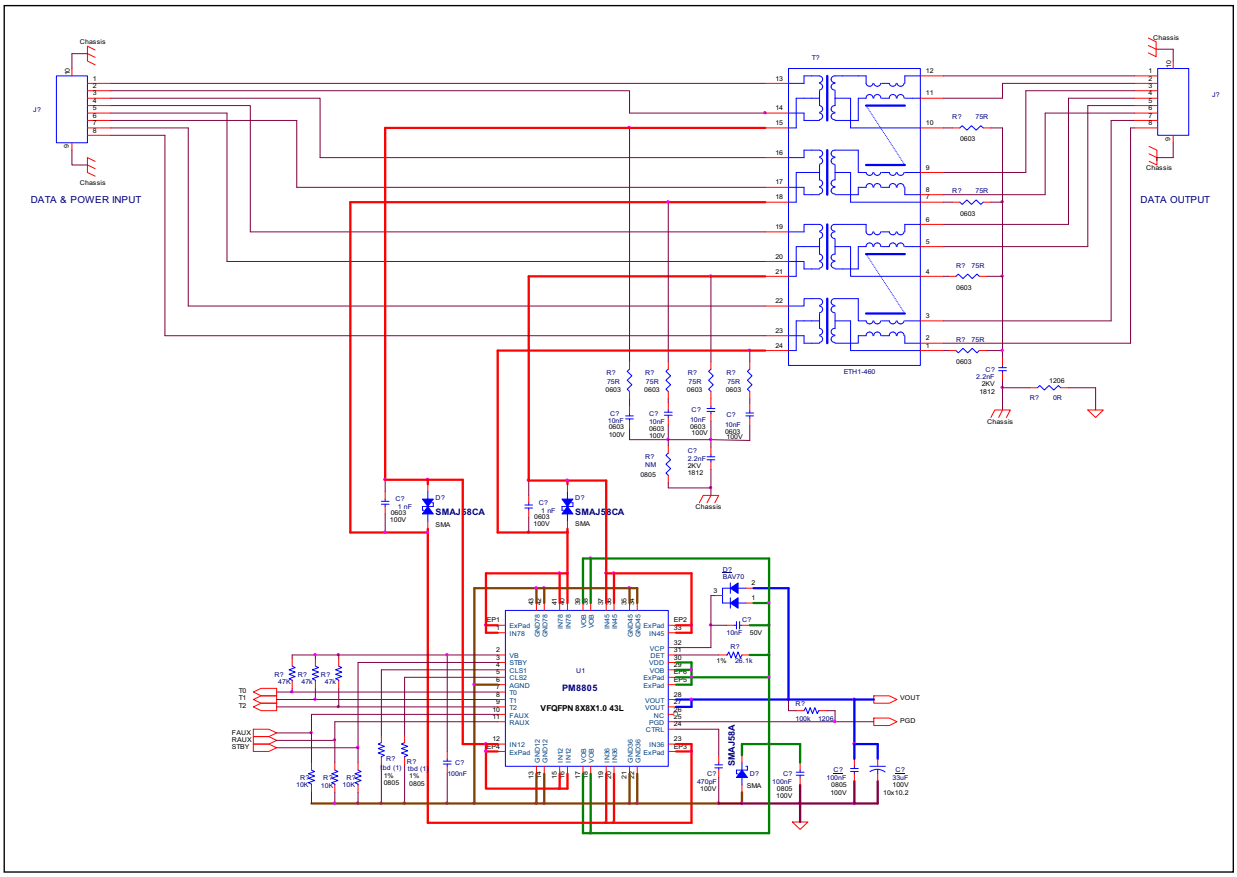
Part number	Package	Packing
PM8805TR	VFQFPN 8X8X1.0 43L PITCH 0.5	Tape and reel

Contents

1 Typical application circuit and block diagram

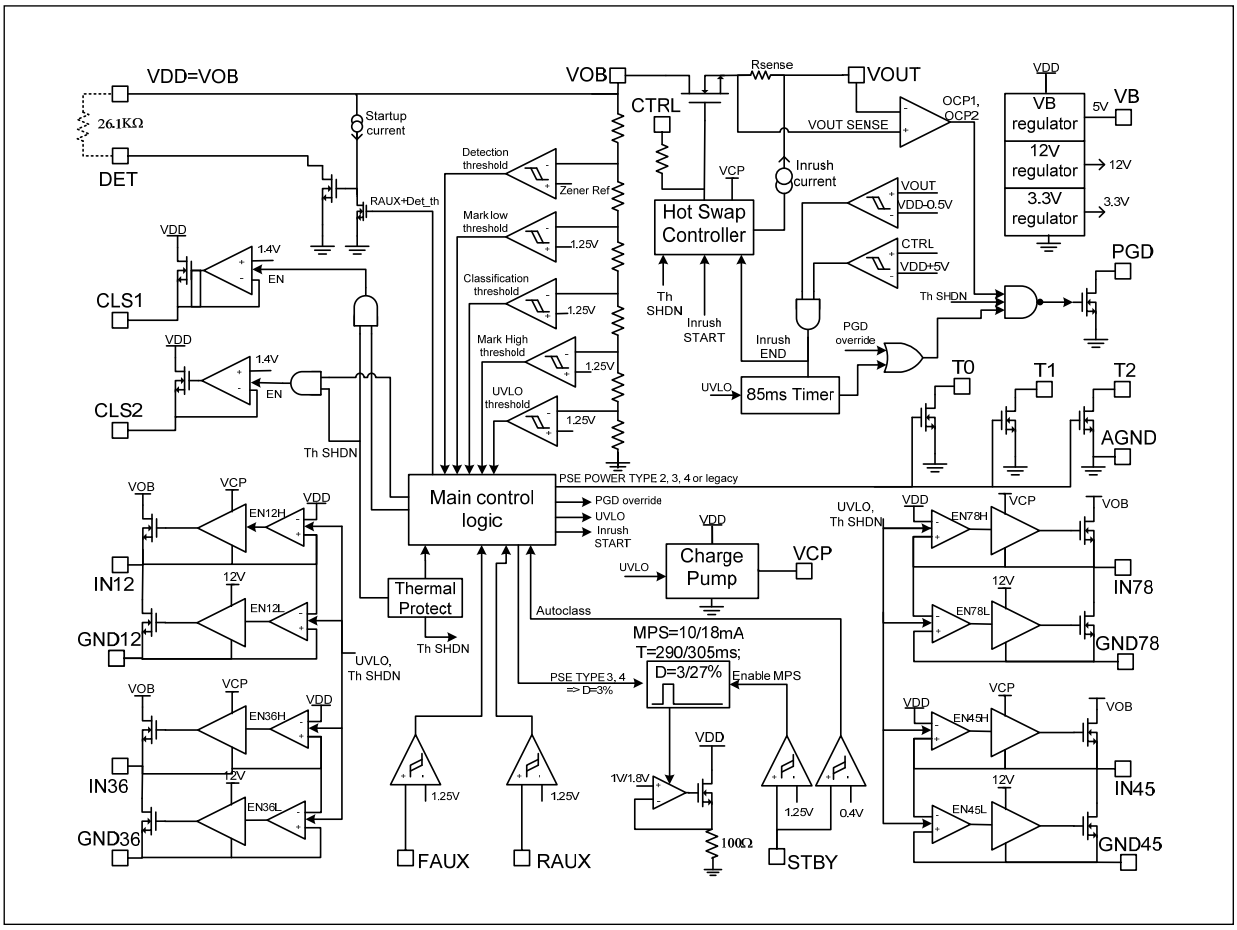
1.1 Application circuit

Figure 1. Simplified application schematic for a PD using PM8805 as input stage



1.2 Block diagram

Figure 2. PM8805 general internal block diagram



2 Pin description and connection diagram

Figure 3. Pin connections (top view)

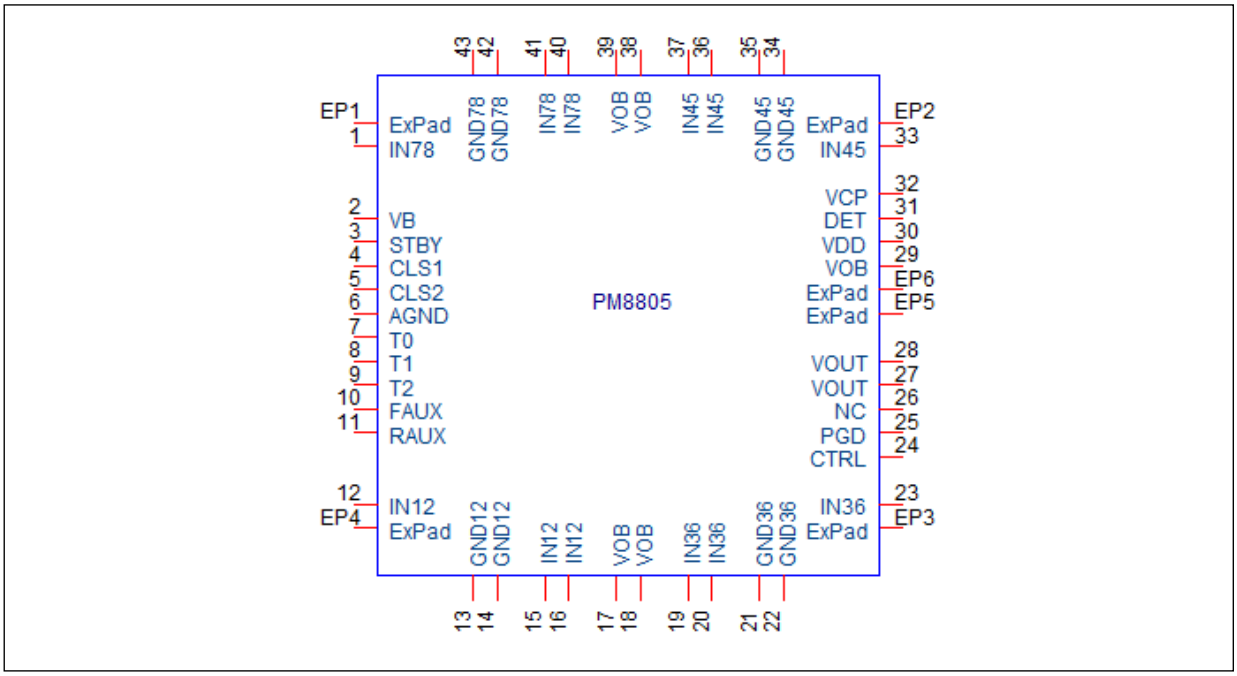


Table 2. Pin description

Pin#	Name	Function
1, 40, 41	IN78	Input for the signals connected to "Spare" pairs. This signal along with IN45 signals is used to feed the 2nd internal bridge.
2	VB	Internal reference voltage 5V up to 10mA; filter this pin with a ceramic capacitor of 100nF typ. connected to AGND. This voltage can be used to bias the I/O pins of PM8805, if needed.
3	STBY	A high level applied to this pin activates an internal 10 / 18mA current source to implement the MPS feature. Duty cycle is Long (.af /.at) or Short (.bt) depending on the detected PSE: Type 2, or Type 3 and 4. Use a resistor voltage divider to AGND to connect this 5V voltage rating pin: typical value for the threshold is 1.25V. If higher than 0.5V during first classification finger, Autoclass feature is enabled. Connect this pin to AGND if not used.
4	CLS1	Classification resistor pin for first and second Class Events. Connect a 0805 classification programming resistor from this pin to AGND. The external resistor is activated with a 3.3ms typ. delay with respect to the classification event.

Table 2. Pin description (continued)

Pin#	Name	Function
5	CLS2	Classification resistor pin for first and second Class Events. Connect a 0805 classification programming resistor from this pin to AGND. The external resistor is activated with a 3.3ms typ. delay with respect to the classification event.
6	AGND	This pin is the ground connection for the PM8805 controller. It must be connected to the other GNDxx pins with short and strong trace.
7	T0	PSE type identification signal. T0 open drain signal assertion happens as described in *Table 3*. This pin is an active low signal, and can be pulled up to VB with an external resistor.
8	T1	PSE type identification signal. T1 open drain signal assertion happens as described in *Table 3*. This pin is an active low signal, and can be pulled up to VB with an external resistor.
9	T2	PSE type identification signal. T2 open drain signal assertion happens as described in *Table 3*. This pin is an active low signal, and can be pulled up to VB with an external resistor.
10	FAUX	This pin can be used to allow the PD to be powered with an auxiliary power source like an external wall adapter connected before the hot swap MOSFET, with voltage lower than the nominal PoE voltage range. Pulling up this pin forces the hot swap MOSFET to turn on when VIN is below the internal UVLO threshold. It may also be used to implement a UVLO override for a low-voltage PoE application. It may be used in combination with RAUX and STBY pins to perform operational modes as described in *Table 4*. Use a resistor voltage divider from the auxiliary voltage to AGND to connect this 5V voltage rating pin: typical value for the threshold is 1.25V. Connect this pin to AGND if not used.
11	RAUX	This pin can be used to give high priority to an auxiliary power source like an external wall adapter connected after the hot swap MOSFET, without stopping the DC/DC operations. It may be used in combination with FAUX and STBY pins to perform operational modes as described in *Table 4*. Use a resistor voltage divider from the auxiliary voltage to AGND to connect this 5V voltage rating pin: typical value for the threshold is 1.25V. Connect this pin to AGND if not used.
12, 15, 16	IN12	Input for the signals connected to "Tx and Rx" pairs. This signal, along with IN36 signals, is used to feed the 1st internal bridge.

Table 2. Pin description (continued)

Pin#	Name	Function
13, 14	GND12	System low potential; it is the return of the first active bridge and it is connected to the Source of the IN12 low-side MOSFET. It must be connected to the system AGND, together with the other bridges' grounds.
17, 18, 29, 38, 39	VOB	System high potential; it is the positive potential of the active bridges and it is connected to the drain of the internal bridge, high-side MOSFETs. Protect the rectified voltage with a TVS and a 100nF X7R 100V rated ceramic capacitor as per IEEE802.3 standard.
19, 20, 23	IN36	Input for the signals connected to "Tx and Rx" pairs. This signal along with IN12 signals is used to feed the 1st internal bridge.
21,22	GND36	System low potential; it is the return of the first active bridge and it is connected to the Source of the IN36 low-side MOSFET. It must be connected to the system AGND, together with the other bridges' grounds.
24	CTRL	Protected replica of the internal gate driver for an external hot swap MOSFET. To slow down the rising edge of this signal a small value ceramic capacitor may be added between this pin and GND.
25	PGD	High-voltage rating, open drain output signal to be used as Enable for a DC/DC converter feed with VOUT voltage. It is pulled down until the PoE voltage is below UVLO, or FAUX is asserted, and the hot swap MOSFET is completely closed. A 85ms delay typ. is required when receiving power from a PSE before this signal is asserted. PGD is also asserted as soon as an RAUX configuration is set.
26	NC	High-voltage rating spare pin. At the moment its function is undefined.
27, 28	VOUT	Source of the high side, hot swap MOSFET. This voltage can be used as input voltage for a DC/DC converter.
30	VDD	High-voltage rating pin, it is the supply voltage input for the PM8805 controller. It must be connected to VOB.
31	DET	Detection resistor, high-voltage rating pin. Connect the signature resistance between DET pin and VOB. Current flows through the resistor only during the detection phase; a typical value for it is 26.1KΩ. This pin has negligible resistance with respect to the external resistance.
32	VCP	High-voltage rating pin, output of the internal charge pump. Connect a 0.5A fast switching diode and a 10nF, 50V X7R ceramic capacitor between this pin and VDD to filter this pin.
33, 36, 37	IN45	Input for the signals connected to "Spare" pairs. This signal along with IN78 signals is used to feed the 2nd internal bridge.

Table 2. Pin description (continued)

Pin#	Name	Function
34, 35	GND45	System low potential; it is the return of the second active bridge and it is connected to the Source of the IN45 low-side MOSFET. It must be connected to the system AGND, together with the other bridges' grounds.
42, 43	GND78	System low potential; it is the return of the second active bridge and it is connected to the Source of the IN78 low-side MOSFET. It must be connected to the system AGND, together with the other bridges' grounds.
EP1	EP1	Exposed pad Connect the pad to a PCB copper plane to improve heat dissipation; it must be electrically connected to the IN78 signal. Internally the pad is connected with the drains of the lower side MOSFETs used in the 2nd bridge.
EP2	EP2	Exposed pad Connect the pad to a PCB copper plane to improve heat dissipation; it must be electrically connected to the IN45 signal. Internally the pad is connected with the drains of the lower side MOSFETs used in the 2nd bridge.
EP3	EP3	Exposed pad Connect the pad to a PCB copper plane to improve heat dissipation; it must be electrically connected to the IN36 signal. Internally the pad is connected with the drains of the lower side MOSFETs used in the 1st bridge.
EP4	EP4	Exposed pad Connect the pad to a PCB copper plane to improve heat dissipation; it must be electrically connected to the IN12 signal. Internally the pad is connected with the drains of the lower side MOSFETs used in the 1st bridge.
EP5	EP5	Main exposed pad Connect this pad to a PCB copper plane to improve heat dissipation; it must be electrically connected to VOB. Internally this pad is connected with the drain of the upper side MOSFETs used in the bridges.
EP6	EP6	Exposed pad Connect the pad to a PCB copper plane to improve heat dissipation; it must be electrically connected to the VOB signal. Internally the pad is connected with EP5, the drain of the high-side MOSFET used in the hot swap section.

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings(1)

Parameter	Value	Unit
V(BR)DSS	100	V
VOB, VDD to AGND (2)	-0.3 to 85	V
VCP to VOB	-0.3 to 10	V
VCP to AGND	-0.3 to 95	V
IN12, IN36, IN45, IN78 to AGND	-0.7 to 85	V
IN12, IN36, IN45, IN78 to VOB	-85 to 0.7	V
IN12, IN36, IN45, IN78 max. input continuous current	2.0	A
GND12, GND36, GND45, GND78 to AGND(2)	-0.3 to 0.3	V
VOUT to AGND	-0.3 to 85	V
VOUT to VOB	-85 to 0.7	V
Max. VOUT output continuous current	3.0	A
CTRL to AGND	-0.3 to 95	V
CTRL to VOB	-85 to 10	V
CTRL to VCP	-95 to 0.3	V
VB to AGND	-0.3 to 6	V
VB to VOB	-85 to 0.3	V
Max VB output current	10	mA
DET, PGD to AGND	-0.3 to 85	V
DET, PGD to VOB	-85 to 0.3	V
PGD to VOUT	-85 to 0.3	V
CLS1, CLS2 to AGND	-0.3 to 3.6	V
FAUX, RAUX, STBY to AGND	-0.3 to 6	V
T0, T1, T2 to AGND	-0.3 to 6	V
T0, T1, T2 to VB	-6 to 0.3	V
ESD HBM	2	kV
ESD CDM	500	V
Maximum operating junction temperature (3)	-40 to 150	°C
Storage temperature	-40 to 150	°C

1. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. VDD must be connected to VOB. GND12, GND36, GND45, GND78 must be connected to AGND.

3. Internally limited to 160°C typ. with internal overtemperature protection circuit.

3.2 Recommended operating conditions

Table 4. Recommended operating conditions

Parameter	Min.	Max.	Unit
PoE input voltage range VOB to AGND	36(1)	57(1)	V
Front AUX Input voltage range to AGND	15	57	V
Rear AUX Input voltage range to AGND	9	57	V
Output current from VOUT signal pins		2	A
Input current for each INxx signal		1	A

1. Those are the limits of the input voltage as specified in the IEEE PoE standard valid for all PD systems.

3.3 Thermal data

Table 5. Thermal data

Symbol	Parameter	Max. value	Unit
R_{THJA}	Thermal resistance junction to ambient(1)	30	°C/W
R_{THJB}	Thermal resistance junction to board(1)	15	°C/W
Pd max	Maximum power dissipation of device(2)	1.3	W
T_A	Operative ambient temperature range(3)	-40 to 85	°C

1. Device mounted on a 4" x 4" wide, 4-layer board (2 signal + 2 power), Cu thickness 35 micron, with:

- 4 small exposed pad (EP1-4) copper areas connected to two power planes plus an external layer of 0.12"x0.12" inches minimum size; those areas are connected together with a minimum of 2x3 via holes.

- a large central exposed pad (EP5) and hot swap exposed pad (EP6) copper area connected to two power planes of 1"x1" inches plus two layers with "minimum pad size shape": those areas are connected with a minimum of 3 times 2x3 via holes placed close the dissipating zone of the device.

See *Section 7* for more details.

2. Device mounted on the board as described in Note 1 and Tambient = 85°C.

   The indicated maximum power dissipation for the device has been calculated as: (TJmax -TAmax) / R_{THJA}.

   The estimated worst case device power dissipation in 4P application is:

   Bridge+ HotSwap+ Controller=4 x 0.15Ω x $1A^2$ + 0.15Ω x 2 A^2 + 0.1W = **1.3W**.

3. Heat sink is needed in order to not reach device thermal limitation.

3.4 Electrical characteristics

(VDD=VOB=48 V, 1 nF from VCP to VDD, 100 nF on VB, TA = -40°C to 85°C unless otherwise specified[a].)

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Undervoltage UVLO						
Vuvlo_rising	UVLO release	Measured between PoE inputs[1] VDD rising	38.0		41.5	V
Vuvlo_falling	UVLO lock-out	Measured between PoE inputs VDD[1] falling	30.5		33.5	V
Vuvlo_hyst	UVLO hysteresis	VDD falling		7.5		V
Tduvlo_falling	UVLO lock-out delay	VDD falling		100		µs
Input bridges						
Rdson_br	MOSFET Ron	30.5< VDD<57V, I=1A		90	150	mΩ
Vbron	Bridge ON max. voltage drop	30.5< VDD<57V, I=1A		180	300	mV
Vbroff	Bridge OFF max. voltage drop	VDD<23V, I=44mA		1.4	1.8	V
Unbal	Bridge to Bridge resistance unbalance	30.5< VDD<57V, I=1A, bridges ON			30	%
Vbfd	Backfeed voltage	100kΩ resistance between unpowered PoE inputs[1], VDD=57V			2.7	V
Ileak	Leakage current	VDD=57V, current drawn by any bridge input[1]			25	µA
ZCD_HS_thr	High-side MOSFET comparator threshold	Measured between any bridge input[1] and VDD		-25		mV
ZCD_LS_thr	Low-side MOSFET comparator threshold	Measured between any bridge input and relevant ground[1]		10		mV
ZCD_hyst	Comparators hysteresis			10		mV
Td_ZCD	Comparators delay		5		15	µs
Charge pump[2]						
Vcp	Charge pump voltage	Measured wrt VDD 30.5< VDD<57V 10nF on VCP pin	6.8		9.8	V
Icp	Capacitor charging current	VCP = VDD+7V		50		µA
Detection and classification						
Von_det	Signature enable	Measured between PoE inputs[1] VDD rising			2.5	V
Voff_det	Signature disable	Measured between PoE inputs[1] VDD rising	10.5		13.0	V

a. Minimum and Maximum limits are guaranteed by test, design, or statistical correlation. Typical values represent the most likely parametric norm at TA =25 °C, and are provided for reference only.

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Ron_det	Signature pull-down resistance	Within signature range		100	200	Ω
IDD_ det	VDD supply current during detection	VDD=8V		15	25	µA
Von_class	Classification enable	Measured between PoE inputs(1) VDD rising	12.5		14.5	V
Voff_class	Classification turn-off	Measured between PoE inputs(1) VDD rising	21.6		24.6	V
Vmark_th	Mark event threshold	Measured between PoE inputs(1) VDD falling	10.1		12.1	V
Vrst_cls	Classification reset threshold	Measured between PoE inputs(1) VDD falling	4	5.2	6.4	V
Td_cls	Delay on classification event current	VDD rising	3.0	3.3	3.7	ms
Vcls	CLSx voltage	Within classification range with 44mA load	1.38	1.4	1.42	V
Icls	CLSx max. current capability	Within classification range with CLS	47		90	mA
Autoclass						
Autoclass_thr	STBY Autoclass enable threshold	VOB within classification range	0.4	0.5	0.6	V
Tcls_typ3	Timer on first cls finger		76	81	86	ms
MPS						
Imps2P	MPS current per 2pair	Total input VDD current	10	11.5	13	mA
Imps4P	MPS current per 4pair	Total input VDD current	18	20	22	mA
Ton_mps3	MPS ON time (3% duty)		8	10	12	ms
Toff_mps3	MPS OFF time (3% duty)		250	275	300	ms
Ton_mps27	MPS ON time (27% duty)		75	85	95	ms
Toff_mps27	MPS OFF time (27% duty)		200	220	240	ms
Bias current VDD						
IDD_cls	VDD supply current during classification	VDD=20V, CLSx pins open		600	1500	µA
IDD_mark	VDD supply current during mark event	VDD=8V	250	600	1000	µA
Hot swap MOSFET						
Rdson_hs	MOSFET resistance			90	150	mΩ
Ictrls	CTRL current	Sourced by CTRL pin when VOB-VOUT<1V		10		µA
Iinrush_low	Inrush current low value	Sourced by VOUT when VOB-VOUT=55V	18		40	mA

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Iinrush_high	Inrush current high value	Sourced by VOUT when VOB-VOUT=7V	95	125	155	mA
Iinrush_ave	Average inrush current	VOUT=0V to 57V		75		mA
Inrush_delay	Iinrush startup delay	From UVLO release		1		ms
Iload_inrush	Load current capability during inrush	VOUT=0V to VOB, PGD=0			10	mA
VDS good	PGD assertion condition	VOB - VOUT (VOUT rising)	0.5		0.7	V
VDS good delay	PGD assertion delay	VOB - VOUT (VOUT rising)		0.4		ms
VGS good	PGD assertion condition	CTRL - VOUT (CTRL rising)	3		6	V
VDS fail	PGD de-assertion condition	VOB - VOUT (VOUT falling)	12		18	V
VDS fail delay	PGD de-assertion delay	VOB - VOUT (VOUT falling) hot swap open		0.4		ms
VDS fail delay	PGD de-assertion delay	VOB - VOUT (VOUT falling) hot swap closed		10	15	us
Idc_OC1	VOUT OC1 protection	VOUT>3V	2.0		3.0	A
Td_OC1	OC1 PGD de-assertion delay	OC1 PGD de-assertion delay	0.9	1	1.1	ms
Idc_OC2	VOUT OC2 protection		4.0		6.0	A
Td_OC2	OC2 PGD de-assertion delay	OC2 PGD de-assertion delay		10	15	us
Tretry		After PGD de-assertion	9	10	11	ms
STBY, FAUX, RAUX signals						
FAUX_thr, RAUX_thr, STBY_thr	Threshold	Signal rising, measured between VOB and AGND	1.20	1.25	1.30	V
FAUX_hyst, RAUX_hyst, STBY_hyst	Hysteresis	Signal falling, measured between VOB and AGND		250		mV
RAUX_del	RAUX delay rising	From RAUX = 1 to device acceptance		3.3		ms
RAUX_del	RAUX delay falling	From RAUX = 0 to device acceptance		65		us
FAUX_del	FAUX delay	From FAUX = 1 to device acceptance		1		ms
RAUX_res	RAUX input resistance	Measured from pin to AGND	250	400		kΩ
RAUX_det_thr	Threshold in detection range	VDD=VOB=9V	1.0		2.0	V
Sleep/Wkup_del	Sleep/Wkup delay	Input setup to sleep/wakeup delay		3.3		ms
Shdn_del	Shutdown delay	Input setup to shutdown delay		3.3		ms

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
PGD signal (open drain)						
PGD_low	Low state	Sinking 1mA		80	200	mV
PGD delay	High state	Measured from UVLO release	80	85	100	ms
T0, T1, T2 signals (open drain)						
	Pull down resistance			30	100	Ω
VB regulation(3)						
VB_def	Default value		4.75		5.25	V
VB_Ilim	Current limit		5		10	mA
Thermal shutdown(4)						
OT_thsd	Shutdown temp	Always on		160		°C
OT_hyst	Shutdown hyst			30		°C
Device current consumption						
Idd_off	VDD quiescent current	VDD>VUVLO_R, VB=5V		1.5	2.0	mA

1. Bridge inputs are IN12, IN36, IN45, IN78, and the relevant ground pins are GND21, GND36, GND45, GND78. PoE inputs are IN12 vs IN36 and IN45 vs. IN78.
2. The charge pump current Icp is intended for charging the VCP capacitor only.
3. The VB regulator is intended for internal use only as pull-up supply of PM8805 I/O signals; any additional external current has to be limited within the specified max. current limit.
4. Guaranteed by design or characterization.

4 PM8805 overview

The PM8805 integrates a dual MOSFET bridge and a PD-PoE single-signature interface, specifically designed to support high power, 4-pair (4P) applications, as being specified in the new IEEE802.3bt standard, but also capable of working with high efficiency, 2P applications.

Typically, after the data transformer a diode bridge is used to set a defined polarity to the input voltage since such polarity on the Ethernet cable may vary.

Considering the maximum power levels defined by the IEEE802.3-2015 standard (25 W for a Type2 PD) the diode bridges power losses may still be acceptable, but with new power hungry applications like UPOE, with more than 50 W at PD end, the power losses of a standard diode bridge become too high.

The same consideration is valid for standard applications that need to squeeze the maximum available power from the PSE. For example, comparing a diode bridge with Vd= 0.8 V with bridged 100 mΩ Ron MOSFETs, the gain at 0.5 A, 50 V is about 0.75 W out of 25 W, i.e. about 3% on overall efficiency.

4.1 Detection and DET pin

In Power over Ethernet (PoE) systems, the Power Sourcing Equipment (PSE) senses the Ethernet connection to detect whether a Powered Device (PD) is plugged into the cable termination physical interface (PI). This is done by applying a small voltage (2.7 V to 10 V) on one of the two couples of pairs that constitute the Ethernet cable and measuring the equivalent resistance in at least two consecutive steps.

During this phase, called Detection, the PD must present a signature resistance between 23.75 kΩ and 26.25 kΩ on each pair-set.

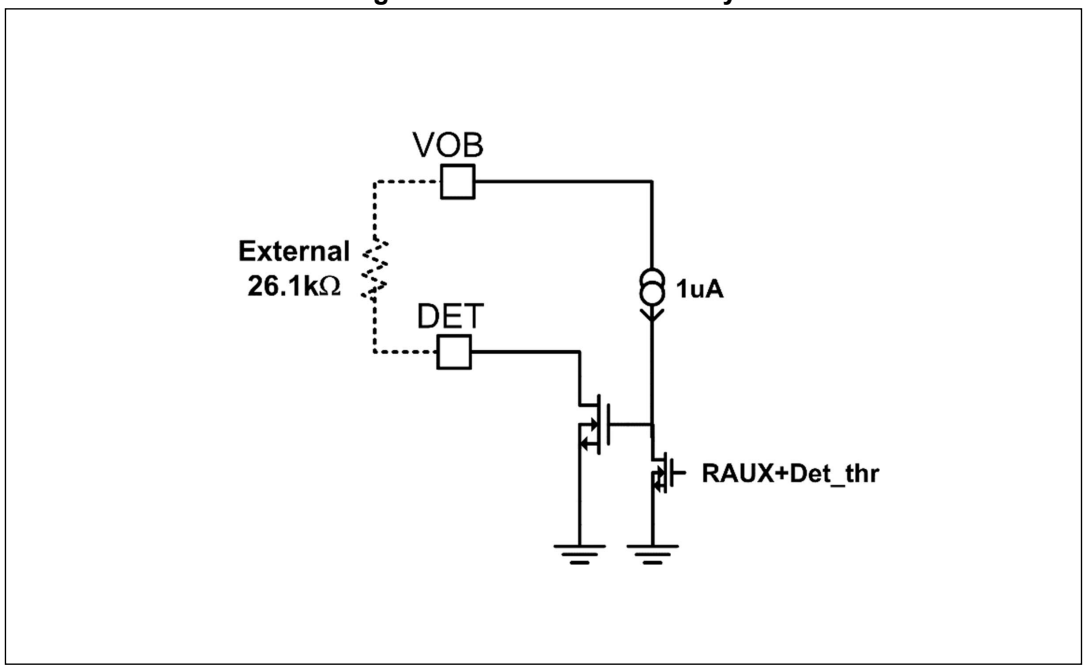
If a single PD is connected to the PI, it may share the same detection resistor for both pair-sets. Such a PD is called Single-Signature PD.

On the PM8805, the signature resistor must be connected between DET and VOB pins. This resistor is in series to a pass transistor (see *Figure 4*) enabled only during the detection phase. No current is flowing through the signature resistor for the rest of the operative phases (Classification and Power On).

The value of the detection resistance has to be selected also taking into account for the additional current flowing into any external circuitry put under the input voltage, e.g. the active bridge. For this reason the typical value that can be used in most cases is 26.1 kΩ.

During Detection, most of the circuitry inside the PM8805, as well as the active bridge, is disabled to minimize the offset current. The current drawn by the IC in this phase is typically 15 uA at 8 V with resistive behavior, so the residual offset current is much less than 10 uA.

Figure 4. DET internal circuitry



4.2 Boot and reset

When the voltage at the input rises above about Voff_det (11.5 V typ.), the PM8805 turns on its internal circuitries (bandgap reference, bias reference, regulators and control logic) and enters into the so-called mark range, waiting for the voltage entering into the Classification range.

When the voltage falls below Vrst_cls (5.2 V typ.), the PM8805 turns off its control logic and analog circuitries and turns the detection circuitry on again, resetting the results of previous classifications.

The current consumption when VDD is in the mark range (IDD_mark) acts as a pull-down of the input voltage and allows a fast reset of the control logic if the cable is disconnected.

4.3 PoE classification

The classification allows the PSE-PD mutual identification, and it is used by PSE to allocate the power to the PD. The PD also understands which type of PSE is connected, and adapts its behavior accordingly.

PM8805 complies with both IEEE802.3-2015 1-event and 2-event classification schemes, and is also capable of multiple event-classification as specified by IEEE802.3bt.

1-event classification in IEEE802.3-2015 is performed by Type1 PSEs capable of powering PDs up to 12.95 W. They can be classified into 4 classes (class 0 to class 3).

2-event classification is performed by Type2 PSEs and class 4 identifies Type2 PDs requiring up to 25.5 W.

The new 4-pair PoE standard defines two extra PD and PSE types. Type3 identifies a PSE delivering up to 60 W, and Type4 a PSE up to 99.9 W over 4-pair. The same types are defined for single-signature PDs, where the allocated power depends on the assigned class, which is the result of the Multiple-Event Classification, summarized in *Table 7*.

The assigned class may be different from the requested class for two reasons: the PSE Type is lower than the PD Type, or the PSE doesn't have enough power to allocate the PD request.

Anyway, if the PSE cannot afford the PD full power, it only issues a number of Class Events compatible with the maximum available power, and the PD has to comply with that.

To do that, the PM8805 provides the system with the indication of the number of Class Events detected through the T0, T1, T2 outputs. See *Section 4.12* for more details.

The PM8805 is capable of covering all Single-Signature PD Types and Classes. As a Type1-2 PD, the PM8805 presents a class 0-4 current within the classification range of 14.5 V to 20.5 V using the CLS1 pin during the first two Class Events. From the 3rd Class Event onwards, the CLS2 pin is activated, so it is possible to set the new classes defined for Type 3 and 4 PDs.

The detailed behavior of the controller during classification is depicted in *Figure 5*:

Above the mark range, with voltage rising above Von_class for the first time, the CLS1 buffer is turned on with a Td_cls delay (3.3 ms typ). Then a Tcls_typ3 timer (81 ms typ) starts, in order to detect the length of the first Class Event. The CLS1 buffer stays on until the input voltage falls below the mark threshold Vmark_th or rises above Voff_class.

When the voltage falls to mark range, the internal timer is stopped and stored, and a Class Event counter is increased. If the Tcls_typ3 time has expired, the first long Class Event is acknowledged, identifying that PSE is Type3 or Type4, thus allowing the PM8805 to set the MPS timings accordingly. See 4.13 for more details on MPS.

When the input voltage re-enters the class range after staying into mark, the CLS1 behavior is the same as before, while the timer is not used anymore.

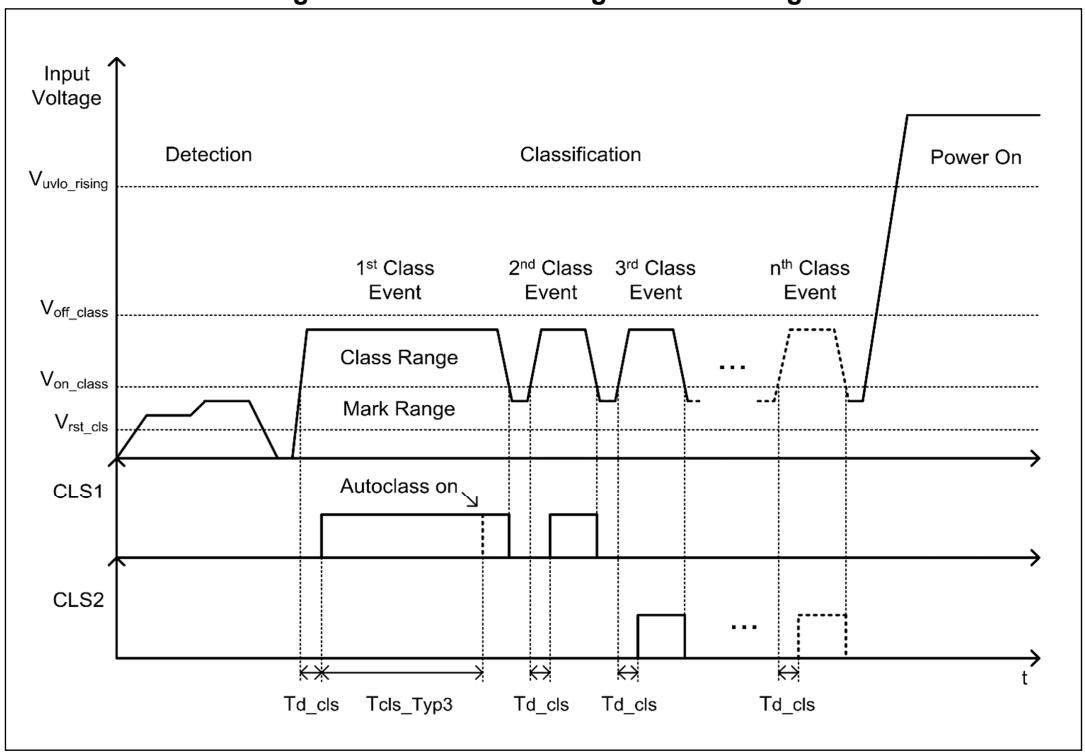
After the third transition into the mark range, entering into class, the CLS2 buffer is turned on instead of CLS1, as always after Td_cls.

The behavior in the following Mark and Class Events is always the same as the third one, regardless of the number of pulses provided by the PSE.

Both CLS1 and CLS2 are turned off if the input voltage exceeds Voff_Class (23 V typ.).

The Classification ends when the PD voltage rises above Vuvlo_rising, or falls below the reset threshold (Vrst_cls). In the first case the number of Class Events stored in the counter determines the values of the T0, T1, T2 outputs, as described in *Table 13* PM8805 Type Signals description table.

Figure 5. Classification signals and timings



Both CLS1 and CLS2 have been designed as voltage regulators, loaded by external class resistors. *Figure 6* depicts a simplified schematic of the classification circuits. During Classification the voltage of the relevant CLS pins is set to Vcls (1.4 V typ.).

In order to set the PD requested class properly, CLS1 and CLS2 pins have to be loaded with the resistors defined in *Table 7*.

Figure 6. CLS internal circuit

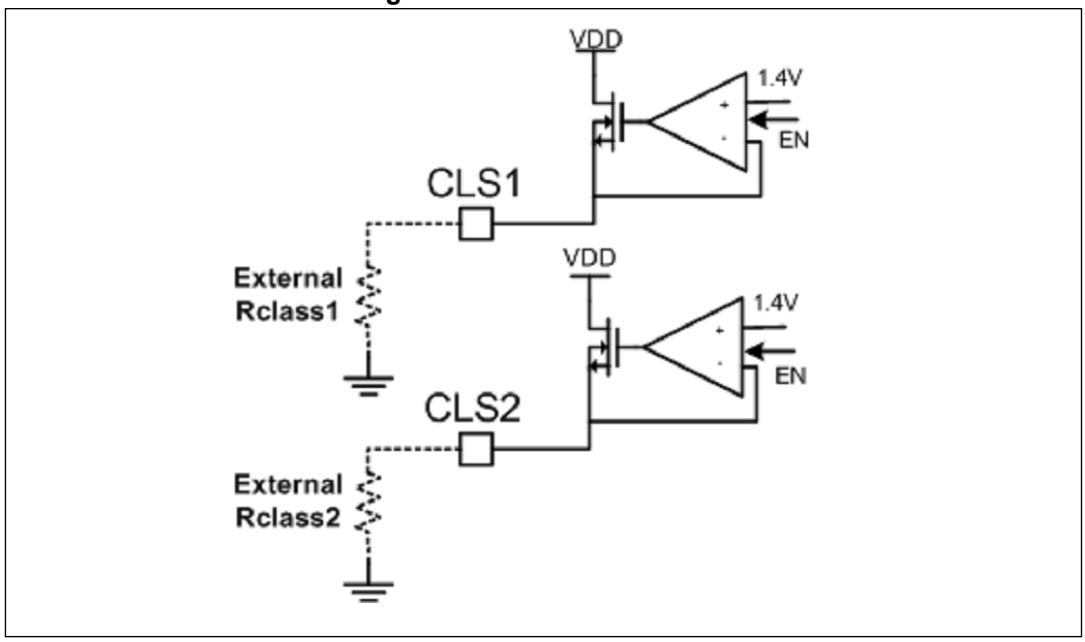


Table 7. Classification table

PSE	PD class (Requested)	CLS1 resistor (Ω)	CLS2 resistor (Ω)	Class events	PD allocated power (W)	PD class (Assigned)	T0 output	T1 output	T2 output (Note 1)
Type 1 (1-event)	0	2K	--	1	12.95	0	1	1	1
	1	150	--	1	3.84	1	1	1	1
	2	80.6	--	1	6.49	2	1	1	1
	3	51.1	--	1	12.95	3	1	1	1
Type 2 (2-events)	4	36.5	--	**2**	**25.5**	4	0	1	1
			--	1	12.95	3	1	1	1
Type 3 or 4 (5-events) 1st event has a Long Pulse	1	150	--	1	3.84	1	1	1	0 or 1
	2	80.6	--	1	6.49	1	1	1	0 or 1
	3	51.1	--	1	12.95	1	1	1	0 or 1
	4	36.5	--	**2, 3**	**25.5**	4	0	1	0 or 1
				1	12.95	3	1	1	0 or 1
	5		2K	**4**	**40**	5	1	0	0
				2, 3	25.5	4	0	1	0 or 1
				1	12.95	3	1	1	0 or 1
	6		150	**4**	**51**	6	1	0	0
				2, 3	25.5	4	0	1	0 or 1
				1	12.95	3	1	1	0 or 1
	7		80.6	**5**	**62**	7	0	0	0
				4	51	6	1	0	0
				2, 3	25.5	4	0	1	0 or 1
				1	12.95	3	1	1	0 or 1
	8		51.1	**5**	**71.3**	8	0	0	0
				4	51	6	1	0	0
				2, 3	25.5	4	0	1	0 or 1
				1	12.95	3	1	1	0 or 1

Note 1. *T2 output indicates the number of used bridges. If the value is 1, only one bridge is used (2-pair), if the value is zero, both the bridges are used (4-pairs).*

The Classification phase is valid only for PoE devices, so it is not required when connected to any non-PoE power source such as a wall adapter; in that cases the CLS buffers are never turned on. See *Section 4.10* for more details on auxiliary sources. The CLS buffers are turned off in case a thermal protection occurs.

4.4 Autoclass

During the first long classification finger, if the STBY pin is pulled above Autoclass_thr (0.5 V typ.), the CLS1 buffer is turned off after Tcls_typ3 to advertise the PSE that the PD is capable of Autoclass.

The purpose of Autoclass is to allow the PSE to determine the actual maximum power drawn of the connected PD; after power-up, a PD that implements Autoclass draws its highest required power throughout a time period bounded by 1350 ms as start time and 3650 ms as end time, both times measured from when PD rises above Vport 2P min.

4.5 Charge pump and VCP pin

Above UVLO voltage, a charge pump circuit is turned on to provide the correct driving voltage to the upper side MOSFETs. Vcp is set about 8 V above the higher input voltage VDD. An external small size ceramic cap, typically a 10 nF 50 V X7R, is suggested between VDD and VCP to stabilize this voltage, as well as a fast switching protection diode with reverse current lower than 1 uA; the current capability Icp of the charge pump is limited to a 50 uA typical and for this reason no other component or circuit is allowed to be connected to VCP.

The charge pump is turned off during standby or sleep mode in order to reduce the power consumption, as well as during RAUX operations, since neither the Active Bridge nor the hot swap MOSFET are on.

See *Table 12* PM8805 Control Signals description for more details.

Note that in the case of OT protection, the charge pump is not turned off in order not to increase the power losses into the active bridge.

4.6 Input Bridges

The bridges integrated into the PM8805 are realized with N-ch MOSFETs in order to minimize the losses due to the diode forward voltage, to improve the current balancing in 4-pair PoE operations and, at the same time, to simplify the PD design allowing huge PCB area savings with respect to discrete active bridges.

The PM8805 is capable of driving the internal N-ch MOSFETs in order to simulate the behavior of the diodes: all the MOSFETs are continuously monitored to control the direction of the current, and prevent a reverse current flow to the PSE or a fast input voltage discharge due to a transient condition.

The MOSFETs are only enabled when the input voltage is greater than UVLO; this means that during detection and classification phases the pass element of the bridges are the MOSFETs body diodes, while the current consumption is reduced in order to avoid corrupting the measurement of the detection resistor and the classification current.

Above UVLO voltage, the input active bridge state machine is activated, in order to discover the polarity of the input bridges and select which bridge can be turned on.

On each high-side MOSFET of the bridges, two circuits work in parallel monitoring the drain source voltage: the first circuit is an op-amp with slow response time, which is in charge to amplify the voltage drop across the MOSFET when the current is lower 200 mA, increasing

the Rdson. The second circuit is a fast ZCD comparator, with a typical response time of 10 us (Td_ZCD), which is in charge of determining the polarity of the current.

Four ZCD comparators are also present across the low-side MOSFETs of the bridges.

The control logic checks the output of the ZCD comparators to determine which bridge to turn on/off. Starting from a default all-off condition, each bridge leg is turned on only if both the ZCD advertises a positive current flowing from PoE to the load, and at the same time the complementary ZCD comparators report a zero current condition (reverse biased diodes).

Only valid input combinations are considered valid for the bridge activation, i.e the IEEE standard ModeA (IN12 - IN36) and ModeB (IN45 - IN78) configurations.

For example, if both IN12=48 V and IN45=48 V while IN36=0 V and IN78=hi-Z, only the high-side MOSFET on IN12 and the low-side MOSFET on IN36 are turned on, while all the other MOSFETs, including the one connected to the high side of IN45, are kept off. This is the typical case when a PSE is turning on only one of the two pair-sets, while both share the same common rail on the high side. This prevents the current flowing on a pair which is not supposed to supply current.

In case any ZCD comparator reports a zero or reverse current condition, both the high-side and the low-side MOSFETs of that bridge are instantaneously turned off.

The active bridge ensures a very low unbalance between pairs, since the contribution on the unbalance is only due to the Rdson mismatch of different bridges. This is generally much lower than the unbalance due to diode bridges, where the difference in the forward voltage may cause big differences in the current flowing in the 2-pair sets. Moreover, the MOSFET channel resistance has an intrinsic ballasting effect on the current, further improving the overall balancing.

In order to comply with the IEEE802.3bt pair-to-pair current unbalance requirements, the PD must not exceed Icon_2P_unb for more than 50 ms. A design guideline is provided by the standard in order to facilitate the compliance at the maximum power levels for each PD class. It is recommended that the pair with maximum resistance (Rpair_max) does not exceed the values reported in *Table 8*.

The contribution to the pair-to-pair unbalance of the PM8805 is Unbal (30% max.) with no offset voltage contribution, typical of diode bridges. So, it should be straightforward to achieve the most stringent requirements (75% for class 8), just taking care not to introduce a large resistance difference between pairs on the application board. Consider that the only components which may introduce unbalance are the data transformer and the PCB traces, whose contribution to the unbalance just needs to be lower than 45% (worst case for class 8).

Table 8. PD unbalance specification

PD class	Icon_2P_unb (mA)	Rpair_max. (Ω)
Class 5	550	2.20*Rpair_min+0.125
Class 6	682	2.01*Rpair_min+0.105
Class 7	777	1.80*Rpair_min+0.080
Class 8	925	1.75*Rpair_min+0.080

In general, depending on the PD Type and class, the relevant PD electrical parameters are summarized in *Table 9*.

Table 9. PD main parameters table

PD type	Class	CLS1 sign.	CLS2 sign.	Pin (W)	Vin min. (V)	Vin max. (V)	Iin max. (mA)	Ppeak (W) for 50ms
1	0	0	0	13.0	37.0	57	350	14.4
	1	1	1	3.84	42.1		90	5.00
	2	2	2	6.49	40.8		160	8.36
	3	3	3	13.0	37.0		350	14.4
2	4	4	4	25.5	42.5		600	28.05
3	1	1	1	3.84	42.1		90	5.00
	2	2	2	6.49	40.8		160	8.36
	3	3	3	13.0	37.0		350	14.4
	4	4	4	25.5	42.5		600	28.05
	5	4	0	40.0	44.3		900	42
	6	4	1	51.0	42.5		1200	53.55
4	7	4	2	62.0	42.9		1440	65.10
	8	4	3	71.3	41.2		1730	74.86

4.7 Hot swap, CTRL and PGD pins

Above UVLO threshold, when the internal charge pump is turned on, an internal current source is used to charge the output capacitor (e.g. the input capacitor of the DC/DC converter) in order to control the inrush current.

The internal current source is only active during the charge phase of the output capacitance, with a 25 mA typ. current when (VOB-VOUT) = 55 V or more, which linearly increases up to 140 mA when the voltage across the hot swap MOSFET falls below 7 V.

Note that the internal current source is not capable of sustaining any extra load applied on VOUT (such as a PWM controller quiescent current), since its only purpose is the charge of Cout. The load can be applied only after the complete charge of the output capacitor (i.e. when PGD signal is asserted).

It is recommended to limit the maximum quiescent current used as a load on VOUT before PGD assertion to 10 mA (Iload_inrush). The more current used to bias output loads, the slower the inrush phase is.

A simplified formula for the current is:

Equation 1

$$I = (25mA\text{-}Iload\_inrush) + 2.4[mA/V] * [55 - (VOB - VOUT)]$$

A simplified formula for the average current is:

Equation 2

$$Iinrush = (25mA\text{-}Iload\_inrush) + 3500[mA \cdot V] / VOB$$

The charging time may be estimated with the formula:

Equation 3

$$Tinrush - Cout \frac{VOB}{Inrush}$$

As an example, assuming a 33 uF output capacitor and 54 V input voltage, the Inrush time is around 24.5 ms.

When the voltage across the hot swap MOSFET is completely closed (VOB-0.5 V) and its gate voltage is higher than 5 V above VOB, all the electrical conditions are set in order to assert the PGD signal (PGD = Hi-Z, open drain, active high) which may serve to enable an external DC/DC converter.

Actually, when powered by PoE a PGD_Delay timer (85 ms typ.) is activated between UVLO and PGD assertion, to ensure the PSE inrush phase is completed before increasing the PD current consumption, as required by the IEEE802.3 standard.

This is just a minimum time, valid if the charge of the output capacitor is faster than PGD_Delay.

It can be calculated indeed that a 110 uF capacitor takes about 84 ms to charge to 54 V; this means that 100 uF is the maximum commercial value for the output capacitance, that causes a standard delay time for PGD assertion. Larger capacitors would need more time to charge, further delaying the PGD, and the consequent DC/DC startup.

The inrush phase may be initiated also when the FAUX pin is asserted: in that case, the control logic asserts the PGD signal as soon as the hot swap MOSFET is closed, without waiting for PGD_delay. See *Section 4.11* for more details on using FAUX.

The PGD signal is the only signal exchanged with the load (e.g. DC/DC converter or LED driver) supplied with the voltage coming from the PM8805.

PGD is an open drain signal, 100 V rated, active high; it can be pulled up to the VOUT voltage, but must be verified if the load circuitry can accept such voltage at its input: in some cases a Zener diode is required to clamp the max. voltage at the converter side.

Alternatively, PGD can be pulled up to a voltage coming from the load, for example the internal start-up voltage of the DC/DC converter, typically in the range of 8-12 V.

The UVLO threshold is provided with an internal delay (100 uS typ.) that as a secondary effect reduces the value of the protection tripping depending on the applied load; the threshold is lower for higher power PDs.

A high value output capacitor allows to mitigate this effect: for instance, assuming a load of 71 W with the minimum UVLO specified at 30 V, using a 47 uF output capacitor the 100 us delay introduces an additional drop of about 5 V (71 W/30 V x 100 us /47 uF) and the real UVLO threshold is 25 V.

4.8 Hot swap protections

Fault conditions for the hot swap MOSFET can be:

- a severe hot swap MOSFET overcurrent;
- a voltage drop higher than 14 V across the hot swap MOSFET;
- a combination of the two above conditions, like a short-circuit between VOUT and GND.

Such fault conditions are internally detected monitoring the current flowing through the hot swap MOSFET, and also the voltage across it, and signaled to the control logic.

If the overcurrent condition is above the level Idc_OC1 (2.5 A typ.) but does not reach the 2nd level (Idc_OC2, 5A typ.) and last for more than the time Td_OC1 (1 ms typ.), then the gate voltage is shorted to VOUT and the PGD signal is deasserted for the time Tretry (10 ms typ.); after that a new startup attempt is performed.

In case of a severe overcurrent, the Idc_OC2 current threshold (5 A typ.) is reached, the gate voltage and the PGD signal are forced low after the time Td_OC2 (10 us typ.) and is deasserted for the time Tretry; after that a new startup attempt is performed.

In case of a voltage drop higher than VDS_fail (14 V typ.) across the hot swap MOSFET, the gate voltage is shorted to VOUT and the PGD signal is forced low after VDS fail delay (400 us typ.). If that voltage drop is combined with a 2nd level overcurrent condition, the delay is reduced to Td_OC2 (10 us typ.).

The protections implemented in the PM8805 allow to overcome the temporary faulty operating conditions and not catastrophic events like a very strong short-circuit on the Vout.

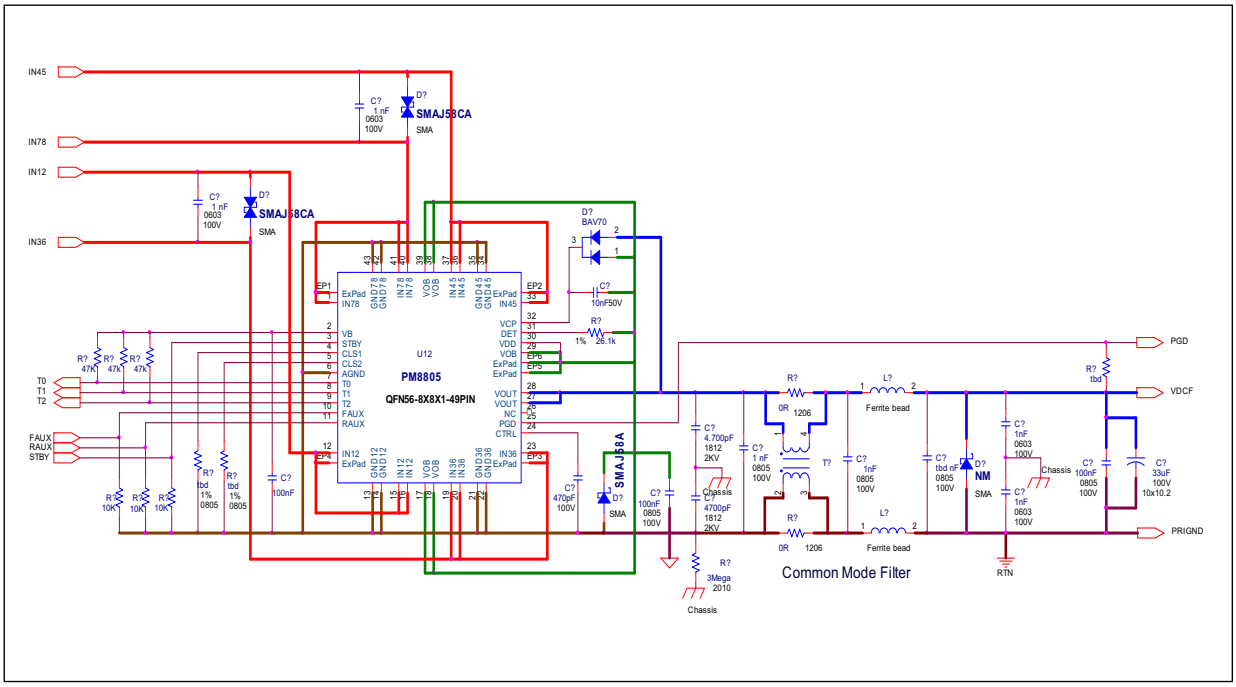
Note also that if the fault persists for a time longer than Tretry the new startup attempt fails due to the limited current available during the startup phase; the fault needs to be removed to be able to have a successful new startup attempt.

4.9 Interface with a DC/DC converter

In most of the PoE applications a common mode filter is required to allow the PoE converter to be compliant with the applicable EMI standards.

The right position where such a filter is introduced is between PM8805 and the PoE converter, as shown in *Figure 7*.

Figure 7. Simplified general schematic with PM8805 and CM filter before the DC/DC



The introduction of the CM filter separates in high frequency the ground reference of PM8805 from the ground reference of the PWM controller, but this has no effect on the behavior of the converter; in fact the only signal exchanged is PGD that can be pulled up close to the PWM controller at the internal reference voltage and, as a further precaution, can also be filtered with a small ceramic capacitor.

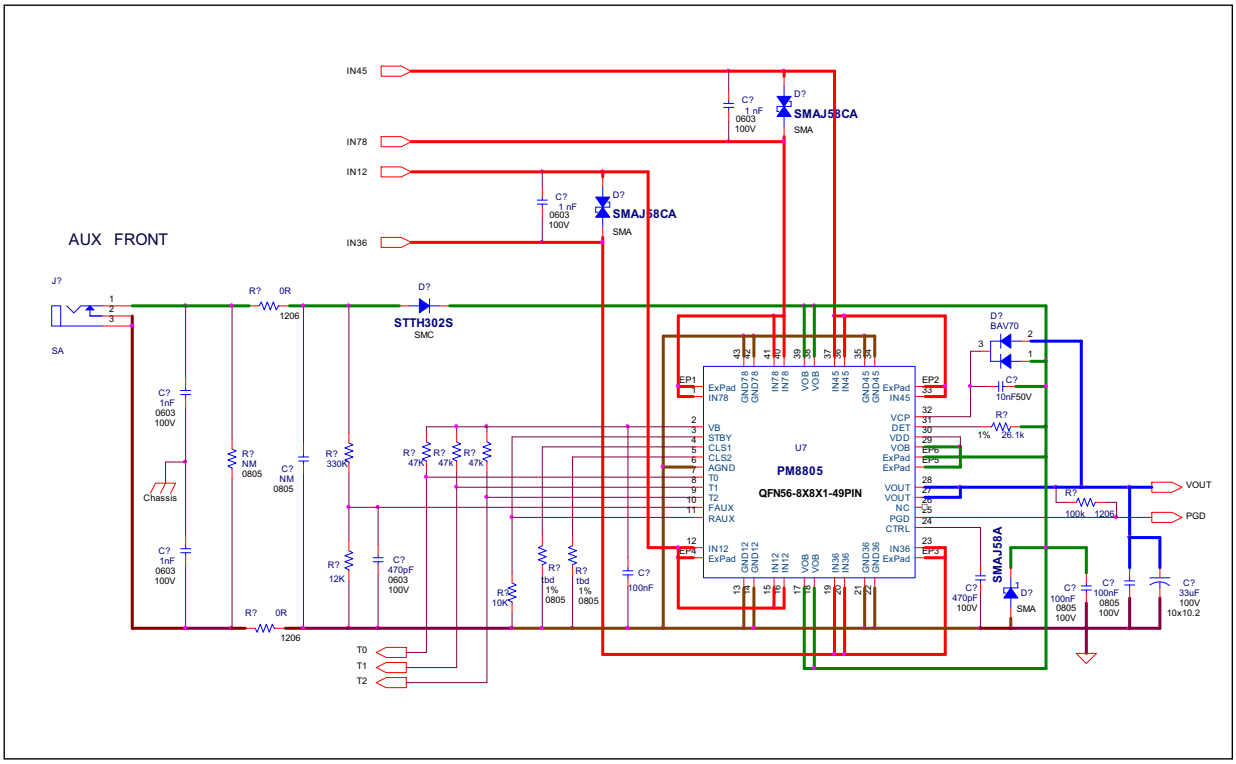
4.10 Auxiliary sources

Some Powered Devices are designed to work with power from either a PoE network or an auxiliary source such as a wall adapter. This allows PDs to be used also when the PoE is not available or when the assigned power is not sufficient.

Two different configurations are typically chosen to connect an auxiliary source to the DC/DC section of a PD device: after the bridge, but before the hot swap MOSFET or after both of those; the PM8805 is designed to facilitate the design of both configurations, allowing the coexistence with the PoE interface.

Figure 8 and *Figure 9* show simplified application schematics where auxiliary sources can be connected either prior (front) or after (rear) the internal hot swap MOSFET, making use of a resistor divider between the external source and FAUX or RAUX pins.

Figure 8. Simplified front aux connections



Connection of the auxiliary source prior to the internal hot swap MOSFET is preferred if used as an alternative (or a backup) to PoE.

The main reason for this is because the priority of the front auxiliary over PoE cannot be guaranteed in every condition, since it depends on the insertion sequence and the voltage of the PoE line with respect to the auxiliary source.

In more detail, the front auxiliary takes priority over the PoE if:

1.The front aux voltage is higher than PoE voltage, or,

2.The front aux connector is plugged when PoE is not (or not yet) present.

If a PSE is already powering the PD, and the auxiliary voltage is lower than PoE, it doesn‘t provide power until the PoE power is removed, acting as a backup power. The minimum operating voltage for the front auxiliary connection is 15 V.

The switch from PoE line to front aux is a one way operation and to back to PoE is needed to remove the front aux voltage and wait for a new detection and classification of PD on the PoE line.

Using a front aux configuration, the charge of the output capacitors is controlled by the internal current source, which is activated when the input voltage is above the UVLO_R threshold or if the voltage on the FAUX pin is above FAUX_thr (1.25 V typ.). With FAUX=1, the PGD signal is asserted - and the hot swap MOSFET activated - as soon as the inrush phase is completed (VDS_good and VGS_good conditions met) with no PGD_delay.

This configuration has the advantage of limiting the inrush current when plugging the DC jack, and the disadvantage of the power losses of the hot swap MOSFET.

For these reasons, high power systems may prefer using the Rear auxiliary connection as shown in *Figure 9*, which also has the feature of taking priority over PoE regardless of the order of connection and the voltage applied.

The simplified application schematics in *Figure 9* shows an auxiliary source connected after the internal hot swap MOSFET. This connection, together with the resistor divider on the RAUX, ensures priority of the external source with respect to the PoE. Indeed, if the voltage of this pin is above RAUX_thr (1.25 V typ.), the internal hot swap MOSFET is opened while PGD is asserted. See *Table 12* for more details on rear aux operation.

The minimum operative voltage for a rear aux operation is 9 V - which allows the use of 12 V +/-10% adapters - even though for high power systems it is recommended using high-voltage power adapters, e.g. 48 V, to facilitate the operation of DC/DC converter and to avoid voltage transients higher than VDS_fail (14 V typ.) across the hot swap MOSFET in the switchover between PoE and auxiliary source.

Depending on the value of the auxiliary source, the resistor divider on RAUX must be sized taking into account the following:

- RAUX_thr in order to provide the PGD to the system when the auxiliary voltage is good enough for a stable operation;
- The AMR of RAUX pin (6 V), which never has to be reached at the maximum auxiliary voltage;
- The RAUX command pin internally presents a 400 kΩ typ. equivalent resistance to AGND (RAUX_res) which causes a typical sink current of about 3 uA at the threshold value of 1.25 V;
- For very low RAUX voltage (12 V or lower) that still falls in the PoE detection range it is suggested to replace the resistor divider with a resistor (up) and Zener (down) network.

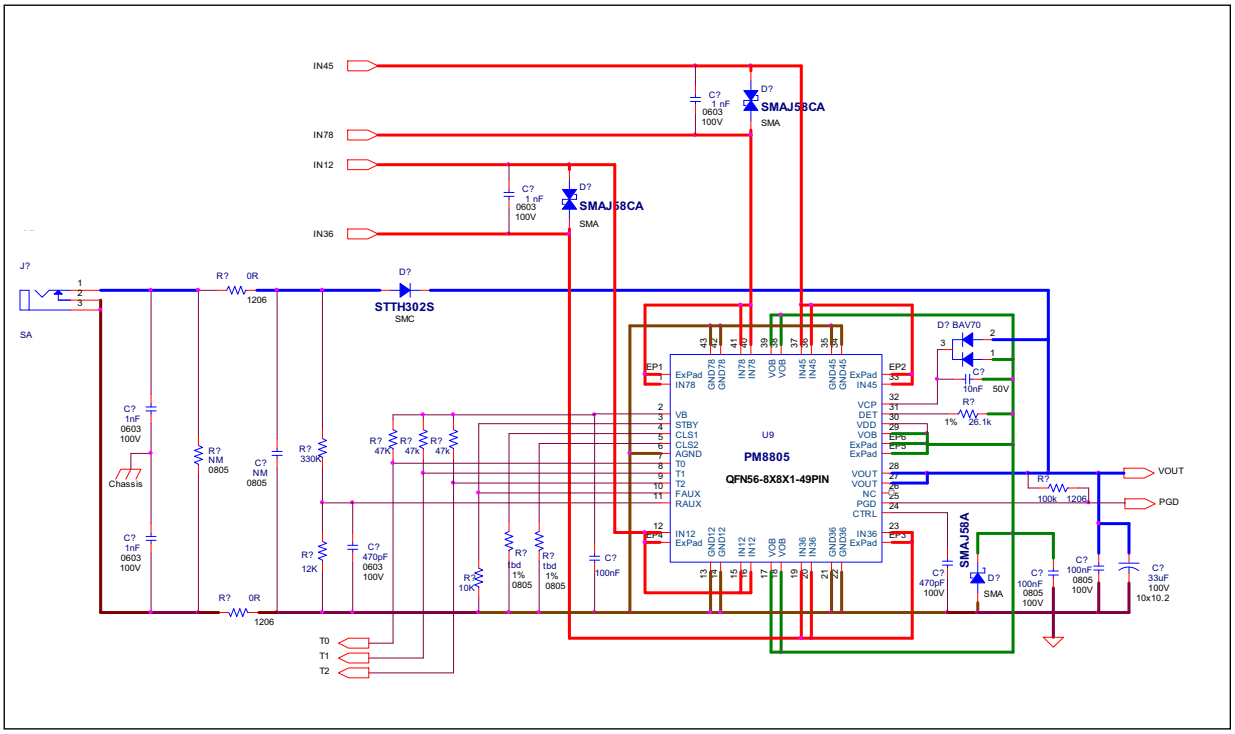
Following the above guidelines, the transition between PoE power and rear aux is typically smooth, with PGD staying asserted during the switchover.

The removal of the auxiliary source is typically followed by a system reboot instead, since the PD consumption is below the MPS limits, and the PSE typically disconnects the port while the aux source is connected. In order to keep the connection with the PSE active, it is possible to enable the MPS circuitry while a rear aux connection is operating. See *Section 4.14* for more details.

If RAUX or FAUX pin are asserted during classification, the class buffers are turned off and the Class Event counter is reset. If FAUX or RAUX are asserted after UVLO, the counter register is stored, in order to provide the classification results after the auxiliary source removal. Regardless of the classification, when FAUX or RAUX are asserted, the T0, T1, T2 are set as described in *Table 13*.

When plugging the DC jack of a rear auxiliary source, it is recommended to limit dV/dt values on VOUT (i.e > 20 V/us), which may cause large current surges. In case the dV/dt cannot be limited, a fast switching diode must be added between VOUT and VCP as a protection for the PM8805.

Figure 9. Simplified rear aux connections



4.11 Operation modes and STBY, FAUX, RAUX command signals

In the PM8805, 3 command signals are available which may be combined to obtain 7 different operation modes, as synthetically described in *Table 10*. The table describes the behavior of the PGD signal, the hot swap MOSFET, the charge pump, the active bridge and the MPS circuitry depending on the configuration on the inputs.

In order to set a "1" signal on the inputs, it is needed to drive the voltage of those pins above their threshold (1.25 V typ.). Below that threshold the configuration cannot be detected, and the system behaves as if it has a "0" input, which is the default PoE standard configuration.

Depending on the value of the voltage source used as pull-up for STBY, FAUX, RAUX, the resistor divider must be sized taking into account the voltage on the command pins above their thresholds but still below their AMR (6 V).

Table 10. PM8805 control signals description table

	Input signals			Output signals				
Standard operations	**FAUX**	**RAUX**	**STBY**	**PGD**	**Hot swap**	**Charge pump**	**Active bridge**	**MPS**
Normal POE operation	0	0	0	1 after 85ms hot swap enabled	Closes @ UVLO	On @ UVLO	Enabled	Off
Standby PoE operation	0	0	1	1 when hot swap closed	Closes @ UVLO	Off	LS enabled HS OFF	On
Front Aux operation	1	0	x	1 when hot swap closed	Closed	On	Enabled	Off
Rear Aux operation	0	1	0	1	Open	Off	Off	Off
Additional operations								
Sleep mode/ Wake Up	1	1	1	0	Open	Off	LS enabled HS OFF	On
Rear Aux with MPS	0	1	1	1	Open	Off	LS enabled HS OFF	On
Latched shutdown	1	1	0	0	Open	Off	Off	Off

4.12 Type T0, T1, T2 output signals

With 3 signals, T0, T1 and T2, 8 different Types of PSE-PD systems are advertised to the PD system:

- Type 1 and 2 as currently specified in the IEE802.3-2012 standard;
- Type 3 and 4 are the new types introduced with the new IEEE802.3bt 4PPoE standard;
- Legacy 4-pair are PSEs which perform Type1 or Type2 classification, then power up the PD over 4-pairs. They may also be new Type3 PSEs limited to Type1 or Type2 power levels. To properly detect 4-pair legacy applications PM8805 embeds a 4P detection circuit which monitors how many bridges are powered.
- Auxiliary power source such as wall adapter.

All the output configurations are described in *Table 11*, and are activated when the VDD voltage exceeds Vuvlo_rising, or an auxiliary source configuration is detected.

The 3 signals are open drain, with 6 V rating, and in most of the cases can be pulled up to VB reference voltage with a resistor in the range of 47 k to 100 kOhms.

Depending on the information needed by the system, it is possible to combine the outputs in order to minimize the number of signals transmitted. This is especially worthwhile in isolated application, where expensive optocouplers are needed to pass the information between primary and secondary side.

As an example, if a Type3 51 W PD just needs to know if the PSE allocated class matches with its requested class, it may just monitor T1. If T1 is set to 0, the PD knows that the PSE

is capable of providing all the power it needs. It is also assumed that an auxiliary source is always capable of providing the requested power.

Table 11. PM8805 type signals description table

Identification	T0	T1	T2	Bridges	Class events	Notes
Type 1 (13W)	1	1	1	1	0 or 1	Legacy PD type
Type 2 (25.5W)	0	1	1	1	2, 3	Legacy PD type
Type 3 (51W)	1	0	0	2	4	New PD type
Type 4 (71W)	0	0	0	2	≥ 5	New PD type
Type3 on 4-pair (13W), or Legacy 4-pair (Type 1 class)	1	1	0	2	0 or 1	New PD type
Type3 on 4-pair (25.5W), or Legacy 4-pair (Type 2 class)	0	1	0	2	2, 3	New PD type
Rear AUX	0	0	1	any	NA	AUX present
Front AUX				0		

See *Table 12* for the minimum information needed for confirming the requested class for each PD class.

T2 indication is directly related to the number of powered pairs, providing a low level output only when both the active bridges are on. When an auxiliary connection is present, T2 is set to 1, since both front and rear Aux connections typically bypass the active bridges.

Table 12. Minimum information needed for confirming requested class

PD requested class	Requested class confirmation
Class 0-3	Always
Class 4	(T0 or T1)=0
Class 5-6	T1=0
Class 7-8	T0 or T1)=0

4.13 Standby and MPS

When a PoE PD system goes into standby its power consumption may be very low and for this reason it may be disconnected by the PSE.

To avoid PD disconnection the PM8805 features a Maintain Power Signature (MPS) current control.

Asserting the STBY pin, the device starts drawing a current whose profile is determined by the detected PSE Power Type, the length of the first Class Event and the number of active pairs when entering STBY mode.

Table 13. MPS current profile

	First class event = long	First class event = short
2-pair power	I=11.5mA; D=3%	I=11.5mA; D=27%
4-pair power	I=20mA; D=3%	I=20mA; D=27%

If the length of the first classification finger is less than Tcls_typ3 (81 ms) the MPS current profile has a 27% duty cycle pulse with a period of Toff_mps27 + Ton_mps27 (305 ms typ.). This is the standard behavior when the PD is connected to Type1 or Type2 PSEs.

Type 3 and Type4 PSEs instead generate a long first Class Event, (longer than Tcls_typ3). In that case the PM8805 sets the MPS duty cycle to 3%, with a period of Ton_mps3+Toff_mps3 (285 ms typ.) allowing to minimize standby power consumption.

If a 4-pair PSE is detected, the MPS current pulse is set to Imps4P (20 mA typ.) instead of Imps2P (11.5 mA typ.) and is shared by the two sets of pairs.

The PM8805 standby mode does not just activate MPS current, but also configures the device in order to minimize the quiescent current consumption, and to avoid the MPS current pulses to be drawn by the capacitance connected to VOUT.

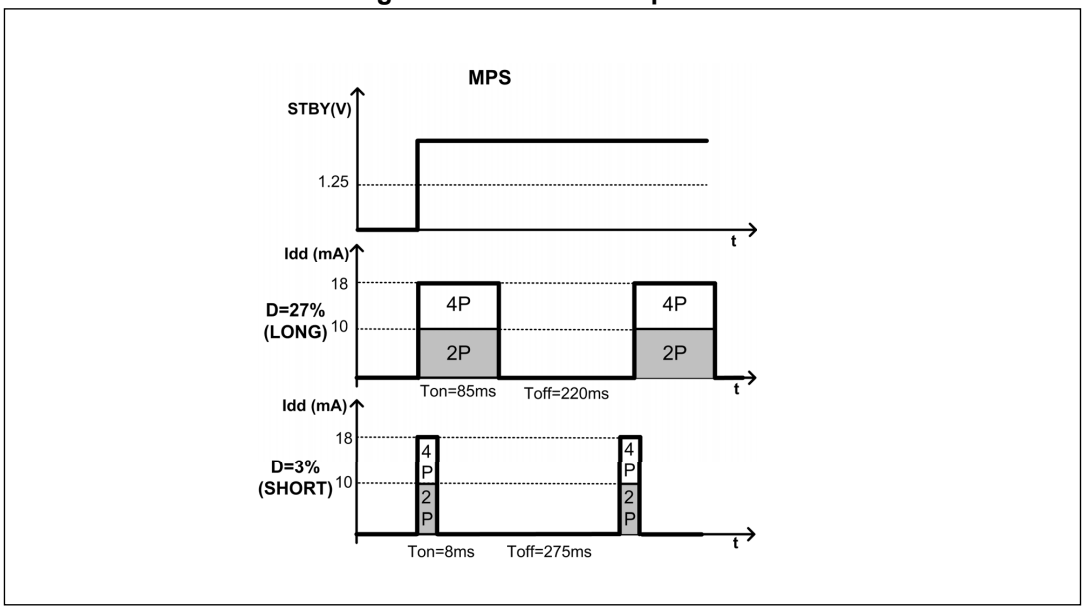
For this purpose, the high sides of the bridges are turned off, as well as the charge pump, and the hot swap MOSFET is operated in linear mode, close to saturation. This implementation introduces a drop voltage across the hot swap MOSFET of about 4 V, causing the MPS current of MPS to be drawn from the PSE instead of the DC/DC capacitors connected to VOUT, thus facilitating the PSE reading the MPS current pulses even if the pulses duty cycle is close to the lower limits defined by the standard.

This feature is very important for applications which are sensitive to the standby current consumption.

When the PM8805 is powered by an auxiliary source, typically the MPS current is not activated, unless it is required to maintain the PoE line alive even if the internal bridge is open: see the following section for more details.

In case of thermal shutdown, MPS current is turned off to ensure that the current consumption is below the minimum threshold, thus allowing the PSE to disconnect the PD.

Figure 10. MPS current profile



4.14 Special operation modes

Beyond the standard operation modes, the combination of the input commands described in *Table 12* activate three special operation modes that can be useful in certain cases; all the special modes have as a basic assumption that the PD system has been successfully detected and classified; in other words, the PD system has already been powered by a PSE.

Rear Aux with MPS

This operation mode allows the PD to maintain an active connection with the PSE even if a wall adapter is connected in rear configuration.

The behavior of the system is similar to a rear aux mode described in *Section 4.10*, but as the MPS pulses are active, the PD load is powered by the auxiliary supply while the PoE line is maintained active with the sole MPS current consumption.

This operation mode occurs under certain conditions:

the auxiliary source voltage is **lower than** / **but close to** the PoE voltage (12 V max. in order to avoid activation of VDS_fail protection: for example, PoE at 54 V and Aux at 48 V). A smooth transition to PoE power is also possible when removing the auxiliary source, while the PoE to rear aux smooth transition is always guaranteed if the following conditions are satisfied:

a) the Cout, which must provide enough energy to the load for all the time period between the Aux removal and the closure of the hot swap MOSFET: as a general rule of thumb use 1 uF for each watt on the load;

b) the inrush current must be lower than the OC2 threshold; a proper selection of the capacitor on the CTRL pin permits to control the peak current at the closure of the hot swap MOSFET: as a general rule of thumb a value between 1 and 2.2 nF covers most of the applications.

If the auxiliary source voltage is **higher** than the PoE voltage (for example, PoE at 42 V and Aux at 48 V), even if rear aux with MPS mode is selected, the PoE to rear aux transition implies the loss of the link with the PSE, basically because the MPS current is drawn from the auxiliary (through the body diode of the hot swap MOSFET) instead of the PSE (through the input bridges).

Latched shutdown

Pulling both FAUX and RAUX input pins high at the same time, the PM8805 goes into a Latched Shutdown condition as described in *Table 12*, with a filter of 3.3 ms before command actuation.

In this condition, the PM8805 goes into a very low consumption mode where the hot swap MOSFET is opened with the PGD de-asserted, the MPS current is turned off, and the active bridges are also off. The overall current consumption stays below Idd_off (2 mA max.), so a PSE monitoring DC MPS removes and recycle power.

Note that while Type1 and Type2 PSEs may monitor AC MPS, DC MPS or both, Type3 and Type 4 PSEs are required to monitor only DC MPS, so power recycle is always assured when the PD is powered by Type3 and Type 4 PSEs.

After power recycle the system reboots completely, performing a new PoE Detection, Classification and Power On.

Sleep / Wake up

Pulling RAUX, FAUX, STBY pins high together, after a 3.3 ms filter delay, the PM8805 toggles between SLEEP and WAKE UP modes.

The sleep mode, as described in *Table 12*, puts the PM8805 hot swap MOSFET in off mode, the PGD signal goes low, while the MPS circuitry is turned on. So, the PD is able to maintain active the connection with the PSE even if the system is turned off and the overall current consumption is much lower than 10 mA.

While the system is in sleep mode, if the same input pins are pulled high again for more than 3.3 ms, the hot swap MOSFET is closed raising the output voltage, then the PGD signal is asserted in order to re-boot the system afterwards.

This operational mode allows the system to go into a deep sleep mode while the PoE line is maintained active and therefore with a WAKE UP the PD system starts sooner than waiting for new Detection and Classification cycles.

The main difference with the standby mode is the absence of output voltage, which may be needed in some cases to further minimize the current consumption of the PD system in this operational mode.

5 Thermal aspects

5.1 Power dissipation

In this paragraph some worst case calculations are performed in order to show the thermal behavior of the PM8805 in 2-pair and 4-pair PoE operation modes.

Assumptions:

- Worst case current on the 4 MOSFETs at the 4 corner of package: 1A
- MOSFET Ron at 25C 90 mΩ, 1.6x at 125C = 150mΩ
- Worst case current on the hot swap MOSFET: 1A per each 2-pairs
- PoE input voltage= 54 V
- Controller quiescent current consumption= 2 mA

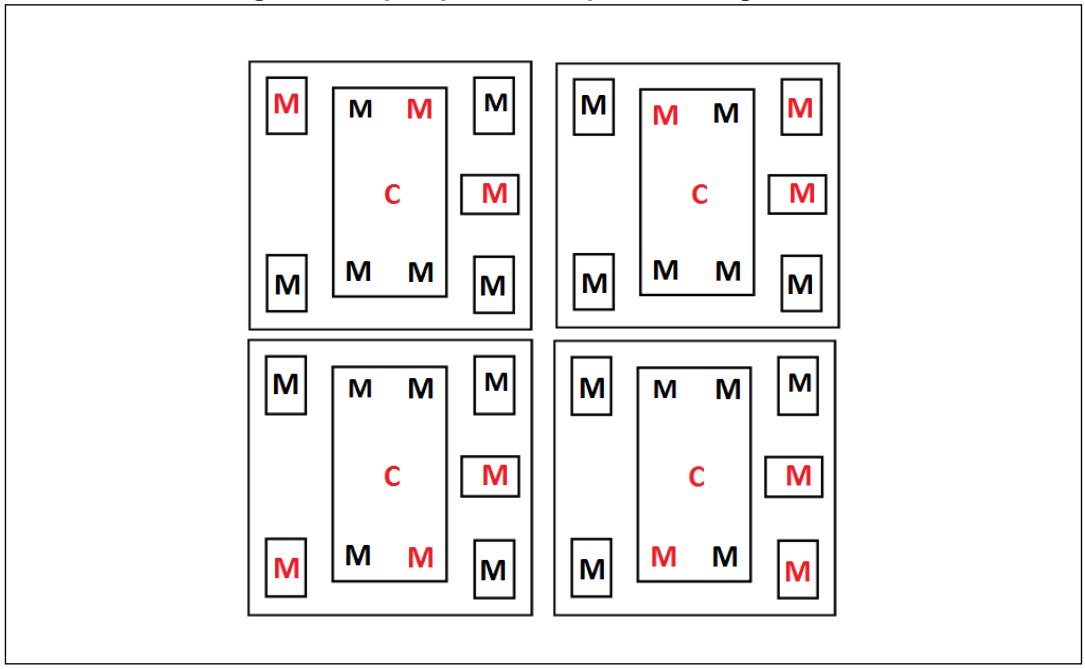
Figure 11 shows four possible 2-pair configurations depending on the polarity and the Alternative by the PSE.

The max. total power dissipated on each of the 2-pair cases is:

Equation 4

$$Ptot\_2P = 2x\ ((1A)^2\ x\ 0.15Ohm) + ((1A)^2\ x\ 0.15Ohm) + (54V\ x\ 2mA)$$
$$= 0.3W + 0.15W + 0.11W = 0.56W$$

Figure 11. 2-pair power dissipation configurations



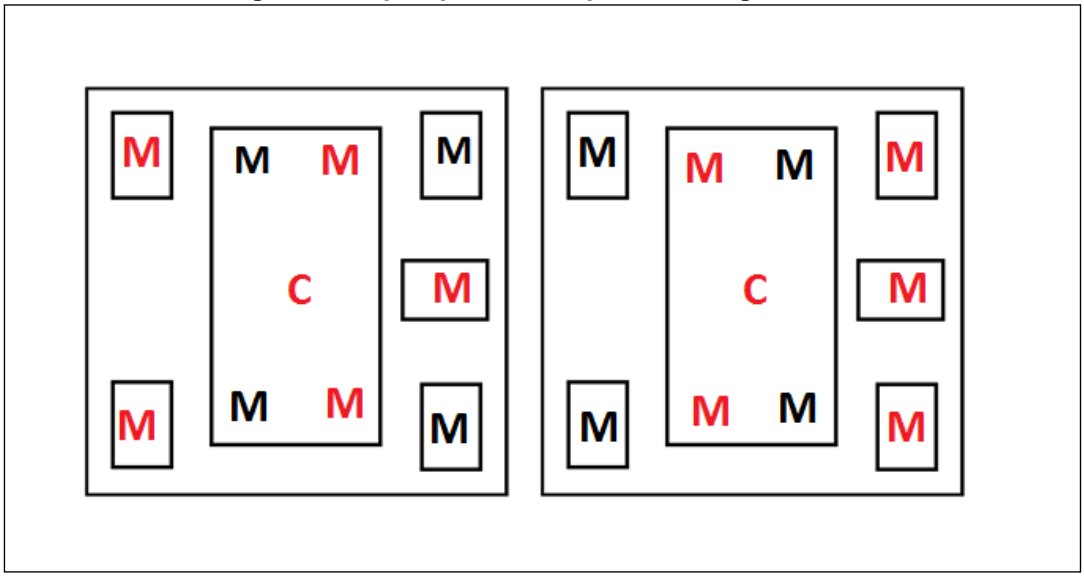
The wide central pad has a total thermal load of 0.11+0.15=0.26 W, but it is connected to a wide copper plane of the PCB (VOUT signal) and not considered critical.

The hot swap is estimated to dissipate about 0.15 W, and can be considered the most critical point of the device together with the one powered corner pad, also having a thermal

load of about 150 mW, considering that the size of those exposed pads is smaller than the central one.

However, the hot swap pad is internally electrically and physically connected to the central pad, so the most critical pads are the 4 pads at device corner. *Figure 12* shows two possible 2-pair configurations depending on the polarity of the PSE.

Figure 12. 4-pair power dissipation configurations



The max. total power dissipated on each of the 4-pair configurations is:

Equation 5

$$Ptot\_4P = 4\ x\ ((1A)^2\ x\ 0.15Ohm) + ((2A)^2\ x\ 0.15Ohm) + (54V\ x\ 2mA)$$
$$= 0.6W + 0.6W + 0.11W = 1.31W$$

In this case the central exposed pad and the hot swap MOSFET dissipate much more power than the 2-pair cases: 1.01 W, while two corner pads dissipate 0.15 W each as in the 2P cases.

In the assumption to require Tj=125°C max. at Ta=85°C, the package soldered on a PCB is needed to show a global Rja of:

Equation 6

$$Rja = 40°C/1.3W = 30.5°C/W$$

This value is comparable with the Rja of a standard VFQFPN 8x8mm with a single exposed pad.

See *Section 6* for a detailed description on the minimum layout that must be implemented on the PCB in order to reach such value of global thermal resistance.

5.2 Overtemperature protection

If OTP occurs, the Classification buffers or the hot swap MOSFET are turned off. The PGD signal is reset (low) and the MPS current is forced off. The VB regulator is also turned off.

The charge pump is kept on, and the control logic of the input bridge is kept active, so that the conducting MOSFETs are kept on.

When the junction temperature goes below about 130 °C, the converter starts automatically, without recycling the input voltage and with the internal state stored before OT protection.

6 Layout guidelines

Here follows a list of recommended procedures to be considered during the routing of a board layout.

The basic assumption is using a 4 layer, 35 um Cu thickness board layout.

The top layer should be used for the exposed pads and for most of the signal routing.

The bottom layer is used mainly for replicated, enlarged copper areas of top exp pads and for remaining signal not routed on top.

Inner layers is for GND copper plane and for routing of VOB and VOUT signals.

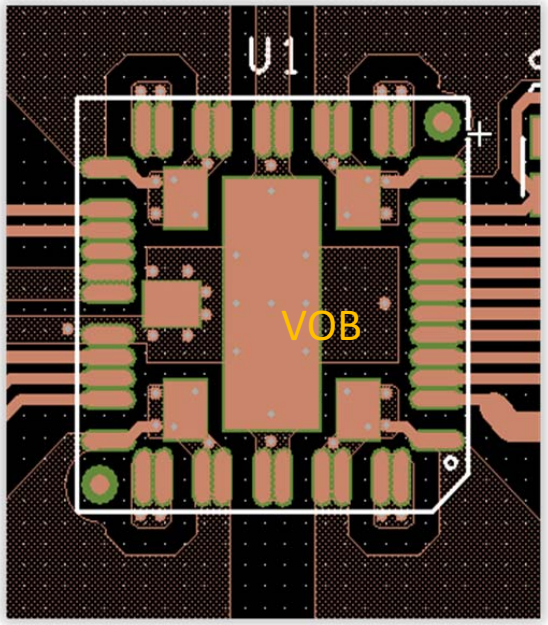
In more detail:

The layout must comply with the minimum creepage distance of 0.7 mm between high-voltage pins and adjacent low-voltage pins. Take into account that this requirement is valid for top and bottom layers where the copper areas and/or traces are exposed (uncoated PCB), while for inner layers the creepage distance can be reduced to about 0.2 mm.

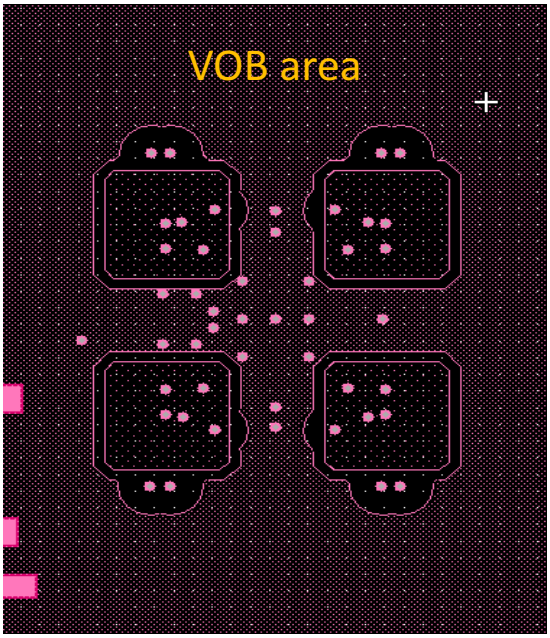
1. Use short traces of at least 30 mils to connect the data transformer to the signals: IN12, IN36, IN45 and IN78; those signals may carry up to 1 A each trace. The trace of those signals may have an impact on the current unbalance at PD interface: try to route those signals with the same trace width and same length. Route those signals in inner layers and replicate exposed pad copper area on the bottom layers, connecting them with 4 - 6 vias for a strong electrical and thermal path: the equivalent copper area for each signal should be around 0.12"x0.12" minimum (3 x 3 mm repeated at least 3 times); better results are obtained with copper areas of 0.2"x0.2" (5x5 mm).
2. The 4 copper areas at each corner of the package is connected to the other layers with the same copper area using multiple vias, at least 4-6 for each area on top layer. AGND signal must be connected to GND copper plane with a short trace of 20 mils minimum.
3. VOB large exp pad must be connected with the exp pad of the hot swap MOSFET and both connected to a large VOB copper area in an inner layer and on the bottom layer with 4 - 6 vias close to each MOSFET die position for a strong electrical and thermal path: the equivalent copper area for VOB signal should be around 0.6"x0.8" (15 x 20 mm repeated at least 2 times plus the min. pad shape repeated again two times).
4. VOUT signal may carry up to 2 A; it is connected to an inner copper plane with short trace and at least 4-6 vias. In case it is routed with a short trace to the load, use a trace width of 60 mils.
5. 5.Remaining signals is routed on top and bottom layer, with no special care except wtth respect to the creepage distances toward the other signals.

Figure 13 shows an example of a real layout done on a 4 layer PCB.

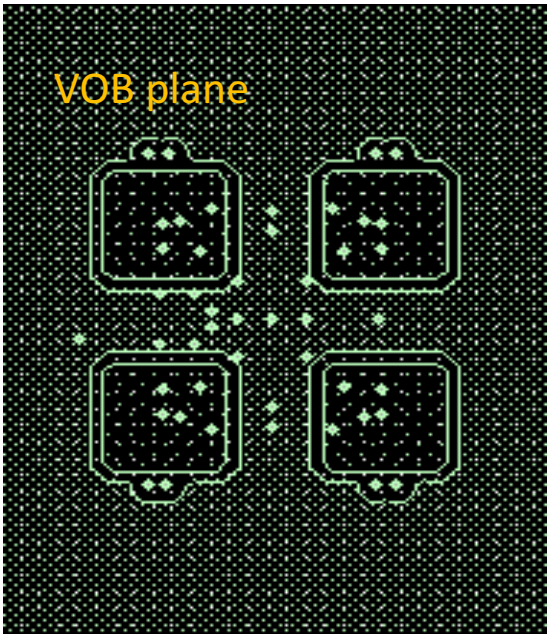
Figure 13. Example of layout for PM8805



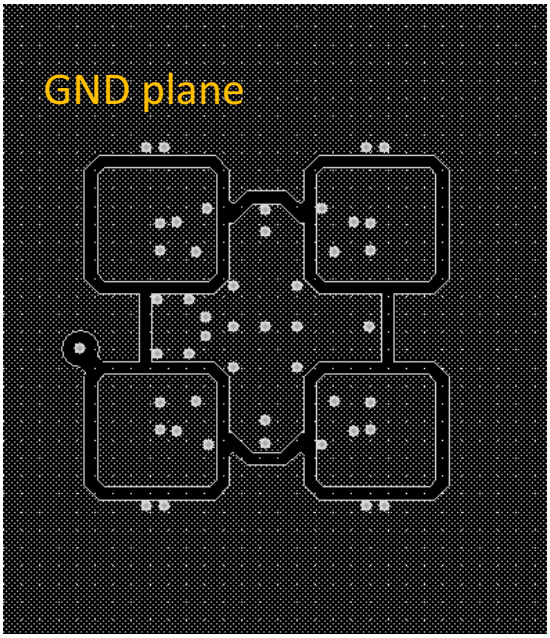
Layer TOP : note the minimum VOB pad shape



Layer BOTTOM



Inner Layer VOB



Inner Layer GND: note the minimum VOB shape

7 VFQFPN43 package mechanical data

7.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

The VFQFPN43L is a custom version of the standard VFQFPN56L 8x8 package, where the large exposed pad is replaced with 6 exp pads: 4 pads at each corner of the body are electrically connected to the 4-pair inputs:

EP4 is internally connected with IN12 signal (drain of low-side MOSFET related to pair 1-2 of 1st bridge)

EP3 is internally connected with IN36 signal (drain of low-side MOSFET related to pair 3-6 of 1st bridge)

EP2 is internally connected with IN45 signal (drain of low-side MOSFET related to pair 4-5 of 2nd bridge)

EP1 is internally connected with IN78 signal (drain of low-side MOSFET related to pair 7-8 of 2nd bridge)

while a large, central exp pad is connected to VOB as well as the last exp pad, relevant to the hot swap circuit:

EP5 is internally connected with VOB signal (drain of 4 high-side MOSFETs of both bridges, common positive output voltage)

EP6 is internally connected with VOB signal (drain of the hot swap MOSFET)

The VFQFPN43L package is designed in order to guarantee the creepage distance between signals at different voltage.

Figure 14. VFQFPN43 8x8mm 43 lead 0.5mm pitch (8x8x1.0mm) mechanical data

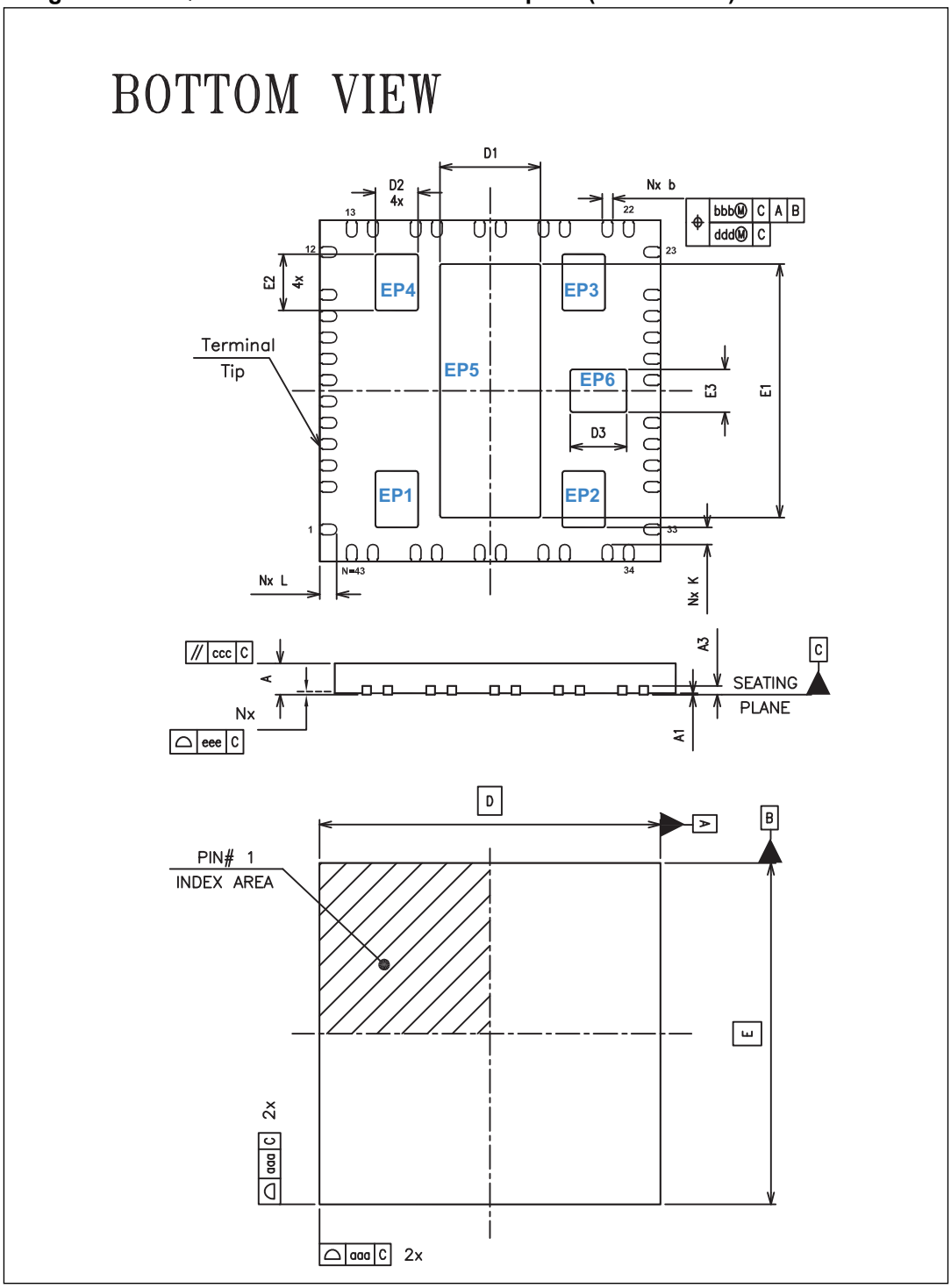
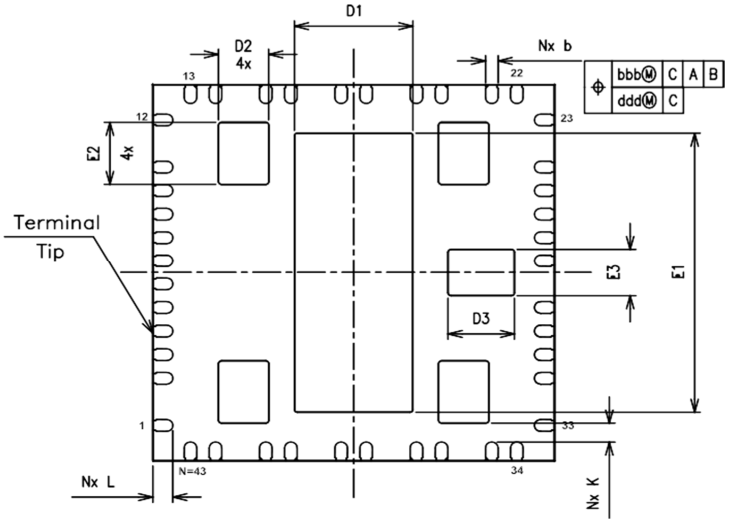


Figure 15. VFQFPN43 8x8mm 43 lead 0.5mm pitch (8x8x1.0 mm) mechanical data 2



PACKAGE DIMENSIONS

DATABOOK				
SYMBOL	MIN.	NOM.	MAX.	NOTE
A	0.8	0.9	1.00	
A1	0.00	0.02	0.05	
A3		0.20 ref		
b	0.23	0.28	0.33	
D		8.00 BSC		
E		8.00 BSC		
D1	2.205	2.355	2.455	
E1	5.790	5.940	6.040	
D2	0.85	1.00	1.10	
E2	1.17	1.32	1.42	
D3	1.17	1.32	1.42	
E3	0.85	1.00	1.10	
K	0.2	---------	----------	
L	0.30	0.40	0.50	
N		43		3
NOTES		1,2		
LF P/N		443431		

SYMBOL	TOLERANCE OF FORM AND POSITION	
	DATABOOK	
aaa	0.10	
bbb	0.10	
ccc	0.10	
ddd	0.05	
NOTE	0.08	
REF		

8 Revision history

Table 14. Document revision history

Date	Revision	Changes
19-Dec-2018	1	Initial release