NTE74174
Integrated Circuit
TTL – Hex D–Type Flip–Flop with Clear

Description:

The NTE74174 is a monolithic, positive–edge–triggered flip–flop in a 16–Lead plastic DIP type package that utilizes TTL circuitry to implement D–type flip–flop logic. Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive–going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive–going pulse. When the clock input is at either the high or low level, the D input signal ha no effect at the output.

Features:

● Contains Six Flip–Flops with Single Rail Outputs
● Buffered Clock and Direct Clear Inputs
● Individual Data Input to Each Flip–Flop

Applications:

● Buffer/Storage Register
● Shift Register
● Pattern Generator

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V

DC Input Voltage, V_{IN} 5.5V

Power Dissipation 38mW

Operating Temperature Range, T_A . . . . 0°C to +70°C

Storage Temperature Range, T_{stg} . . . . −65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High−Level Output Current	I_{OH}	–	–	−800	µA
Low−Level Output Current	I_{OL}	–	–	16	mA
Clock Frequency	f_{clock}	0	–	25	MHz
Width of Clock or Clear Pulse	t_w	20	–	–	ns
Setup Time	t_{su}				
Data Input		20	–	–	ns
Clear Inactive State		25	–	–	ns
Data Hold Time	t_h	5	–	–	ns
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High−Level Input Voltage	V_{IH}		2	–	–	V
Low−Level Input Voltage	V_{IL}		–	–	0.8	V
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −12mA	–	–	−1.5	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −800µA	2.4	3.4	–	V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA	–	0.2	0.4	V
Input Current	I_I	V_{CC} = MAX, V_I = 5.5V	–	–	1	mA
High Level Input Current	I_{IH}	V_{CC} = MAX, V_I = 2.7V	–	–	20	µA
Low Level Input Current	I_{IL}	V_{CC} = MAX, V_I = 0.4V	–	–	−1.6	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 4	−18	–	−57	mA
Supply Current	I_{CC}	V_{CC} = MAX, Note 5	–	45	65	mA

Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under "Recommended Operation Conditions".

Note 3. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 4. Not more than one output should be shorted at a time.

Note 5. With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V is applied to clock.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Clock Frequency	f_{max}	R_L = 400Ω, C_L = 15pF	25	35	–	MHz
Propagation Delay Time, from Clear Input	t_{PLH}		–	16	25	ns
	t_{PHL}		–	23	35	ns
Propagation Delay Time, from Clock Input	t_{PLH}		–	20	30	ns
	t_{PHL}		–	24	35	ns

Function Table (Each Flip−Flop):

Inputs			Output
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_o

H = HIGH Level (Steady State)
L = LOW Level (Steady State)
X = Irrelevant
↑ = Transition from LOW to HIGH Level
Q_0 = The level of Q before the indicated steady
state input conditions were established

Pin Connection Diagram

$\overline{CLR}$	1	16	V_{CC}
1Q	2	15	6Q
1D	3	14	6D
2D	4	13	5D
2Q	5	12	5Q
3D	6	11	4D
3Q	7	10	4Q
GND	8	9	CLK

16   9

1   8

.870 (22.0) Max

.260 (6.6) Max

.200 (5.08) Max

.100 (2.54)

.099 (2.5) Min

.700 (17.78)