



PSMN029-100HL

N-channel 100 V, 29 mOhm, logic level MOSFET in LPAK56D using TrenchMOS technology

26 September 2022

Product data sheet

1. General description

Dual logic level N-channel MOSFET in an LPAK56D (Dual Power-SO8) package using TrenchMOS technology.

2. Features and benefits

- High peak drain current I_{DM}
- Copper clip and flexible Leads
- High operating junction temperature $T_j = 175\text{ °C}$
- Superior reliability
- Low body diode reverse recovery charge Q_r

3. Applications

- Synchronous rectifier
- Forward and flyback converter
- Industrial drive
- Power management system
- Uninterruptible Power Supply (UPS)

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	100	V
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	-	30	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	68	W
T_j	junction temperature		-55	-	175	°C
Static characteristics FET1 and FET2						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 5\text{ A}$; $T_j = 25\text{ °C}$; Fig. 12	-	25.1	29	mΩ
		$V_{GS} = 5\text{ V}$; $I_D = 5\text{ A}$; $T_j = 175\text{ °C}$; Fig. 12 ; Fig. 13	-	68	80	mΩ
Dynamic characteristics FET1 and FET2						
Q_{GD}	gate-drain charge	$I_D = 10\text{ A}$; $V_{DS} = 80\text{ V}$; $V_{GS} = 5\text{ V}$; $T_j = 25\text{ °C}$; Fig. 14 ; Fig. 15	-	10.9	-	nC
$Q_{G(tot)}$	total gate charge		-	29.6	-	nC
Avalanche ruggedness FET1 and FET2						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 30\text{ A}$; $V_{sup} \leq 100\text{ V}$; $V_{GS} = 5\text{ V}$; $T_{j(init)} = 25\text{ °C}$; Fig. 4	[1] [2]	-	83	mJ

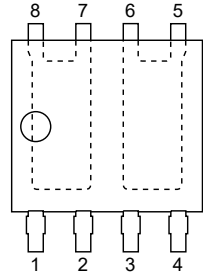
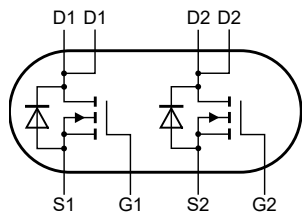
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode FET1 and FET2						
Q_r	recovered charge	$I_S = 10\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$	-	50.1	-	nC

- [1] Refer to application note AN10273 for further information
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 <p>LPAK56D; Dual LPAK (SOT1205)</p>	 <p>mbk725</p>
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PSMN029-100HL	LPAK56D; Dual LPAK	plastic, single ended surface mounted package (LPAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN029-100HL	29RL10H

8. Limiting values

Table 5. Limiting values

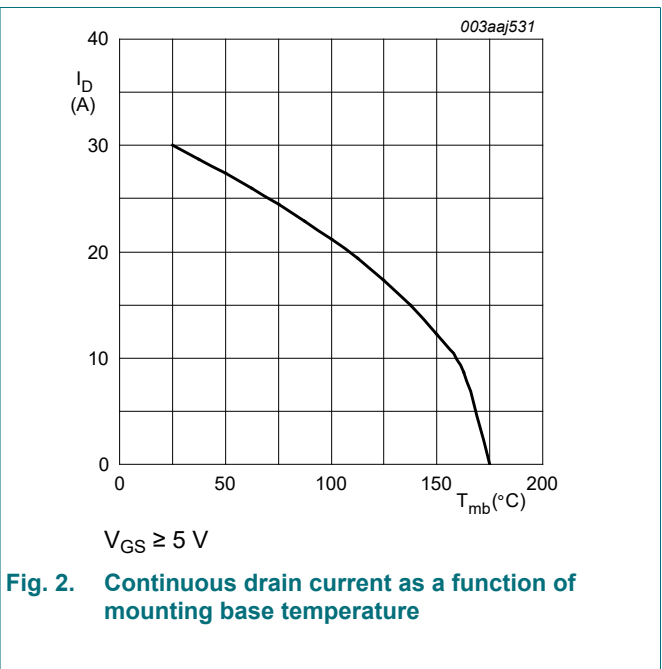
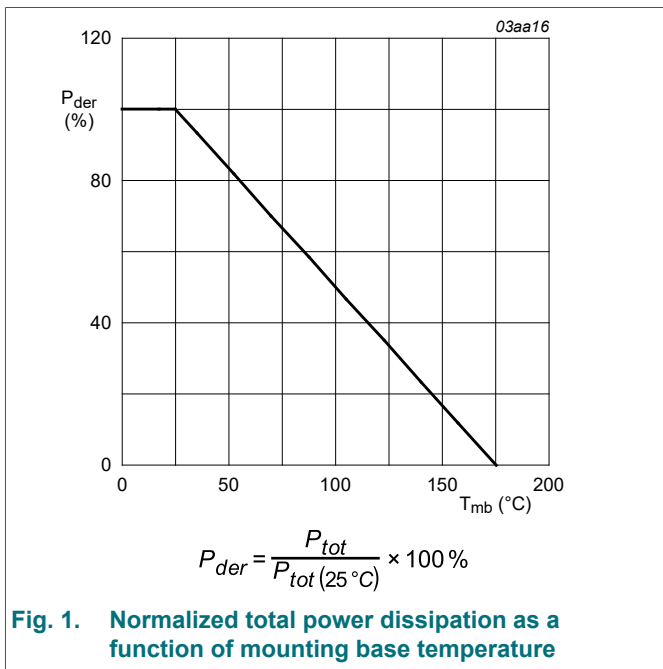
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ }^\circ\text{C} \leq T_j \leq 175\text{ }^\circ\text{C}$	-	100	V
V_{DGR}	drain-gate voltage	$25\text{ }^\circ\text{C} \leq T_j \leq 175\text{ }^\circ\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage	DC; $T_j \leq 175\text{ }^\circ\text{C}$	-10	10	V
		Pulsed; $T_j \leq 175\text{ }^\circ\text{C}$	[1] [2]	-15	15
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 1	-	68	W

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Symbol	Parameter	Conditions	Min	Max	Unit
I _D	drain current	V _{GS} = 5 V; T _{mb} = 25 °C; Fig. 2	-	30	A
		V _{GS} = 5 V; T _{mb} = 100 °C; Fig. 2	-	21	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3	-	118	A
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
T _{slid(M)}	peak soldering temperature		-	260	°C
Source-drain diode FET1 and FET2					
I _S	source current	T _{mb} = 25 °C	-	30	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	118	A
Avalanche ruggedness FET1 and FET2					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 30 A; V _{sup} ≤ 100 V; V _{GS} = 5 V; T _{j(init)} = 25 °C; Fig. 4	[3] [4]	-	83 mJ

- [1] Accumulated Pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering T_j and or V_{GS}.
- [3] Refer to application note AN10273 for further information
- [4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C



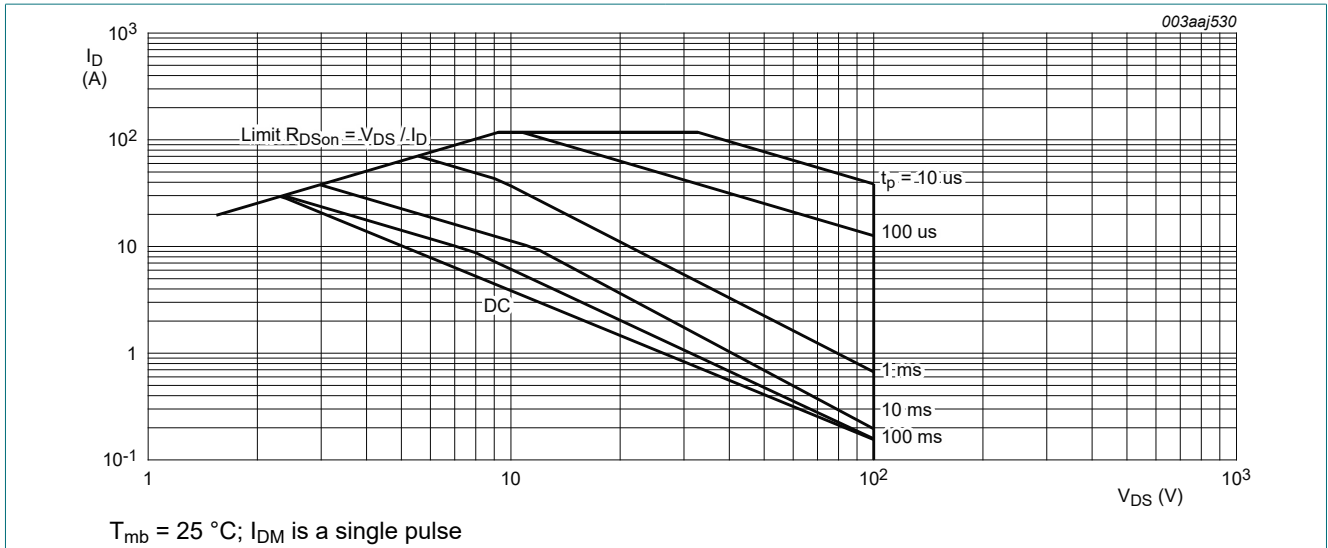


Fig. 3. Safe operating area; continuous and peak drain current as a function of drain-source voltage

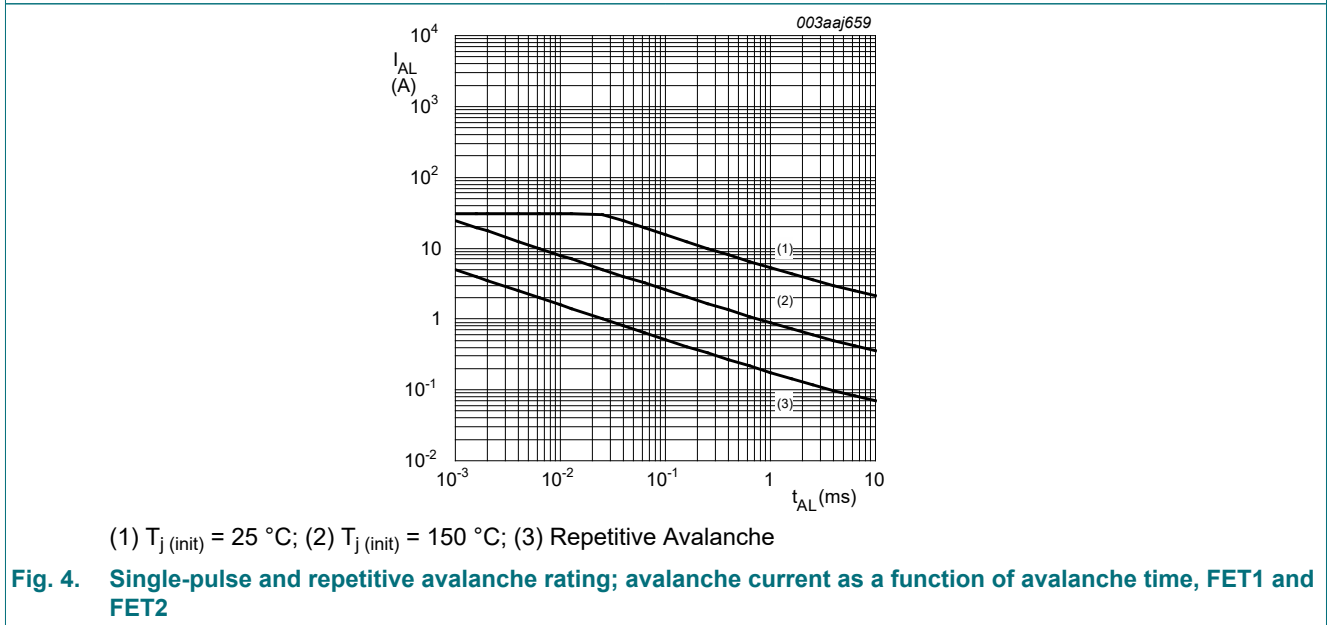


Fig. 4. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time, FET1 and FET2

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	2.21	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W

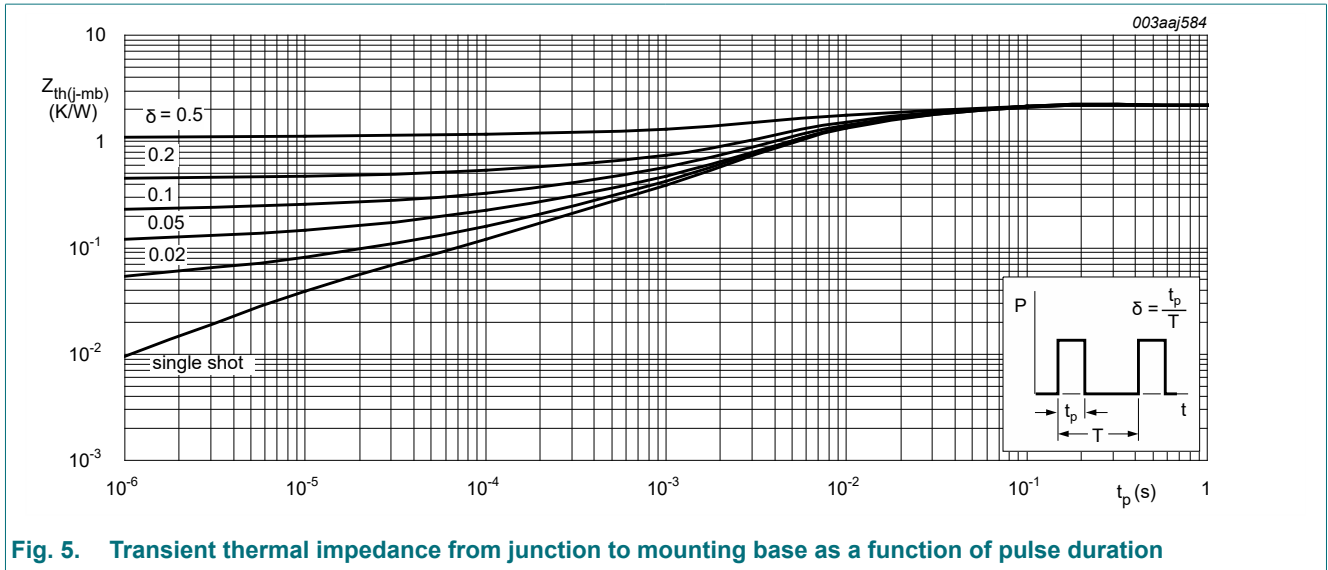


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

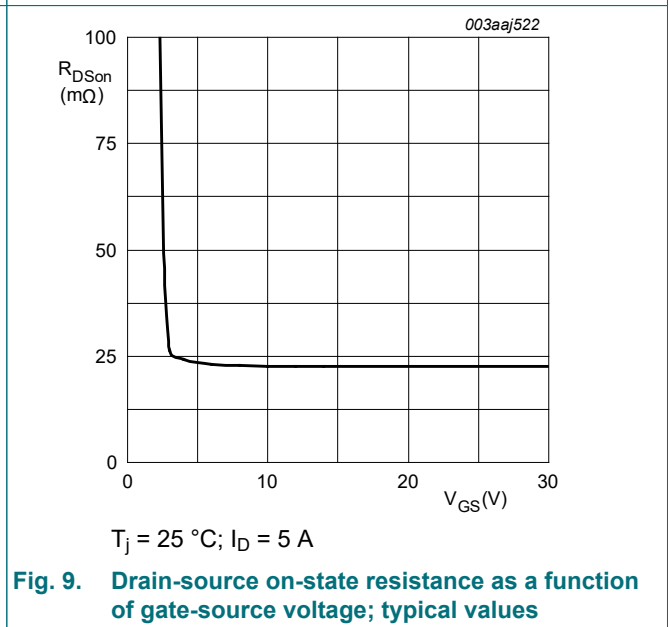
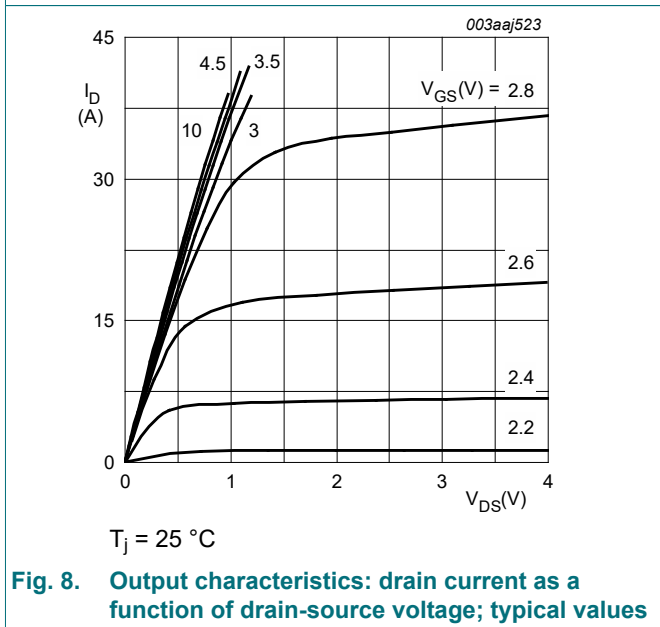
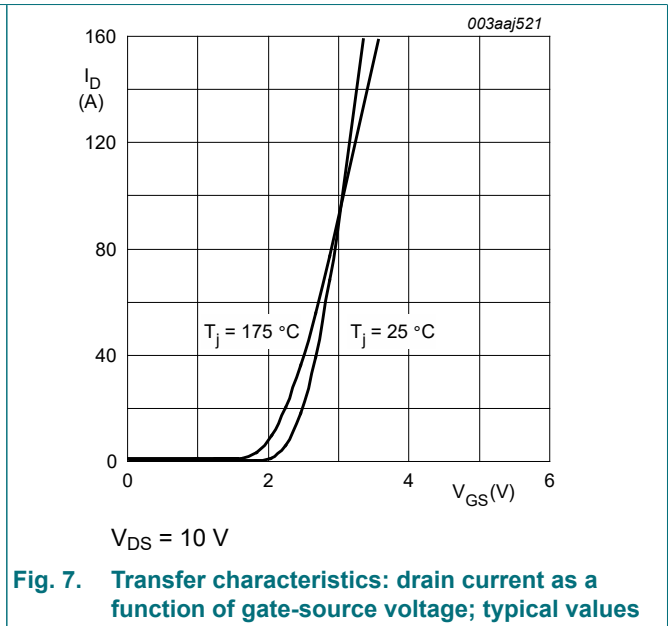
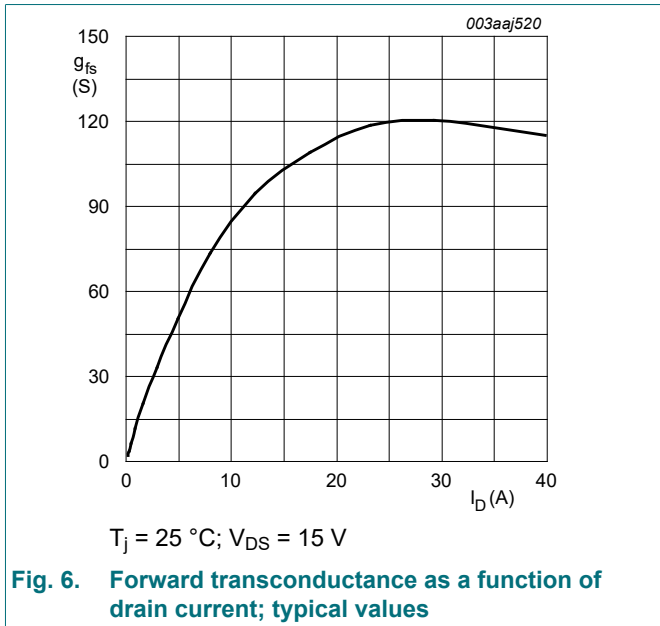
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics FET1 and FET2						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	90	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C$; Fig. 10 ; Fig. 11	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C$; Fig. 10 ; Fig. 11	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C$; Fig. 10 ; Fig. 11	-	-	2.45	V
I_{DSS}	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.02	1	μA
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ C$; Fig. 12	-	25.1	29	m Ω
		$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 175 \text{ }^\circ C$; Fig. 13	-	68	80	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ C$; Fig. 12	-	22.7	27	m Ω
Dynamic characteristics FET1 and FET2						
$Q_{G(tot)}$	total gate charge	$I_D = 10 \text{ A}; V_{DS} = 80 \text{ V}; V_{GS} = 5 \text{ V}; T_j = 25 \text{ }^\circ C$; Fig. 14 ; Fig. 15	-	29.6	-	nC
Q_{GS}	gate-source charge		-	5.6	-	nC
Q_{GD}	gate-drain charge		-	10.9	-	nC
C_{iss}	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$; Fig. 16	-	2727	3637	pF
C_{oss}	output capacitance		-	169	203	pF
C_{rss}	reverse transfer capacitance		-	106	145	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 80 \text{ V}; R_L = 8 \text{ } \Omega; V_{GS} = 5 \text{ V}; R_{G(ext)} = 5 \text{ } \Omega; T_j = 25 \text{ }^\circ C$	-	13.4	-	ns
t_r	rise time		-	18.7	-	ns

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(off)}$	turn-off delay time		-	48	-	ns
t_f	fall time		-	36	-	ns
Source-drain diode FET1 and FET2						
V_{SD}	source-drain voltage	$I_S = 15\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 17}$	-	0.78	1.2	V
t_{rr}	reverse recovery time	$I_S = 10\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$	-	32.7	-	ns
Q_r	recovered charge	$V_{DS} = 50\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	50.1	-	nC



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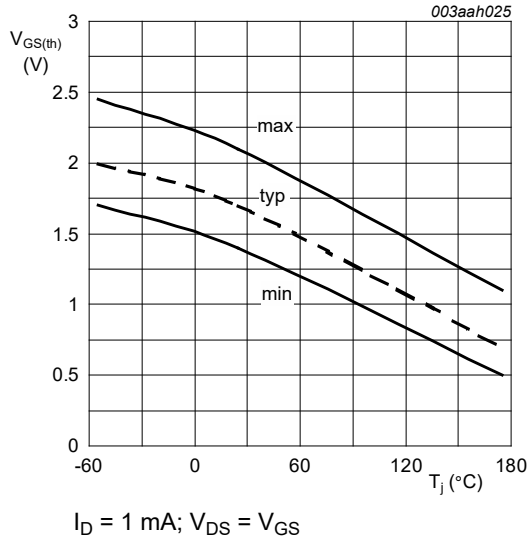


Fig. 10. Gate-source threshold voltage as a function of junction temperature

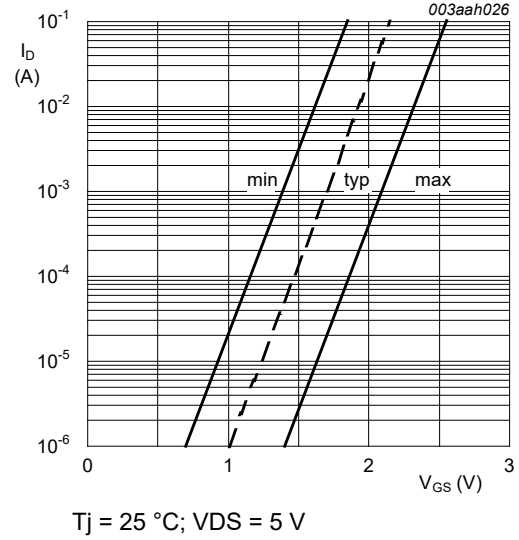


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

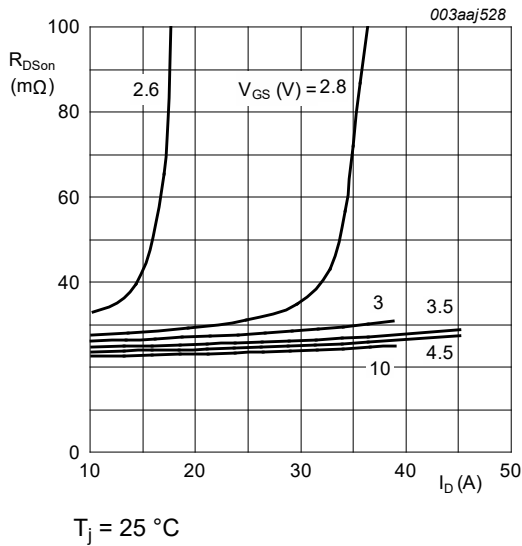


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

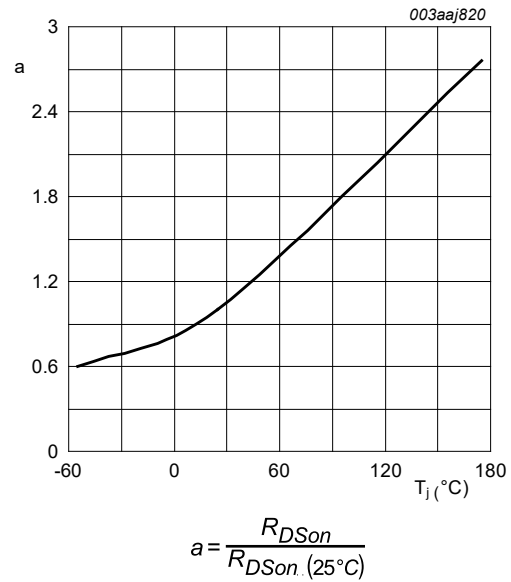


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

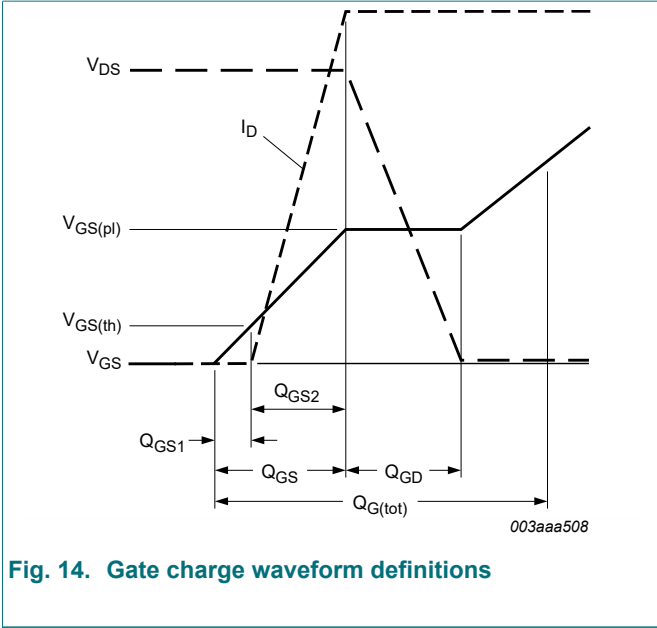


Fig. 14. Gate charge waveform definitions

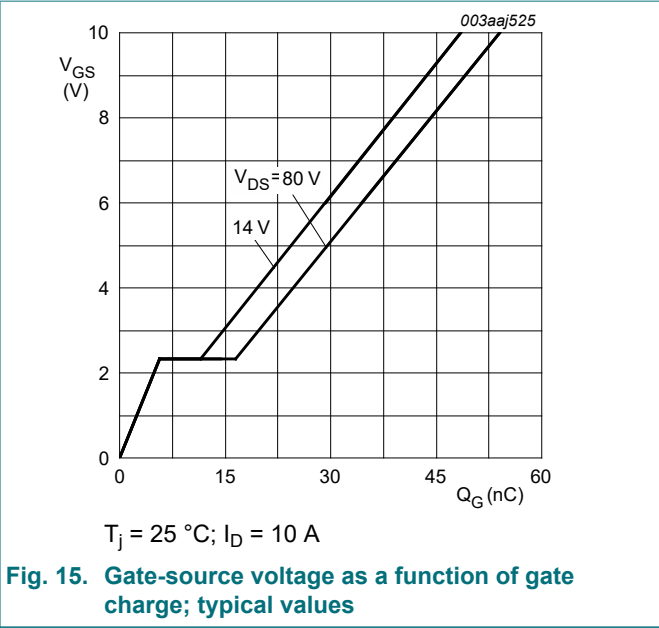


Fig. 15. Gate-source voltage as a function of gate charge; typical values

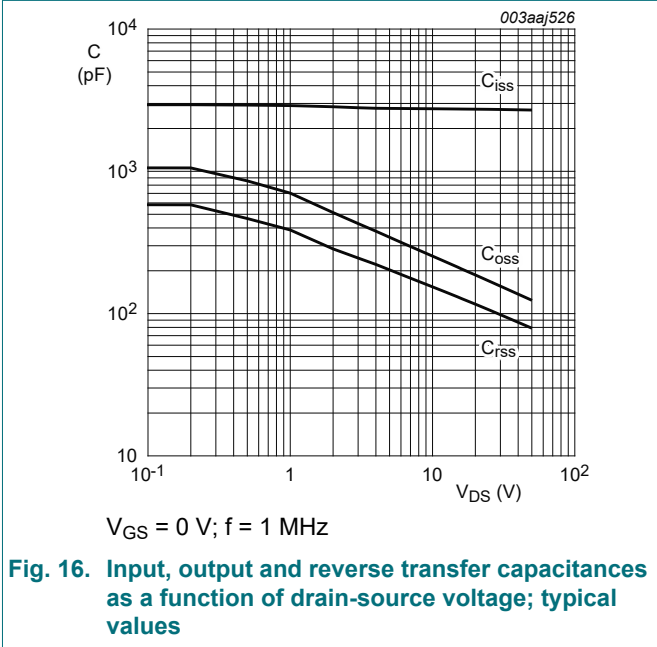


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

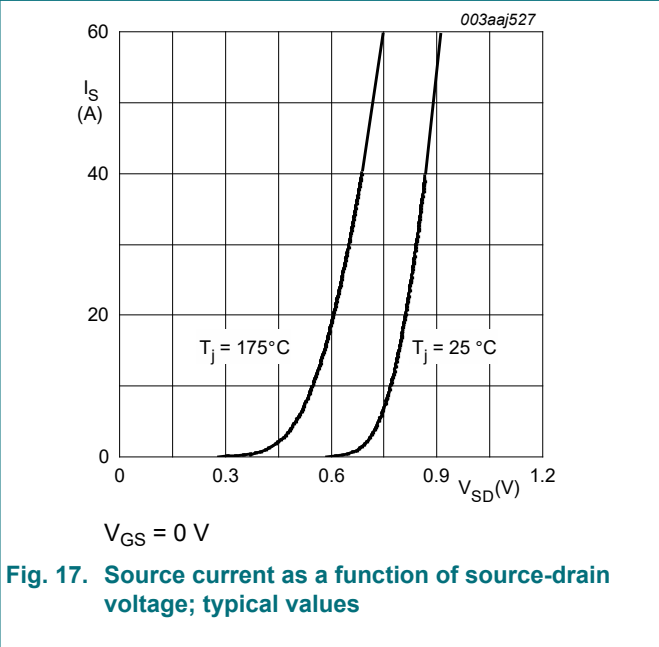


Fig. 17. Source current as a function of source-drain voltage; typical values

11. Package outline

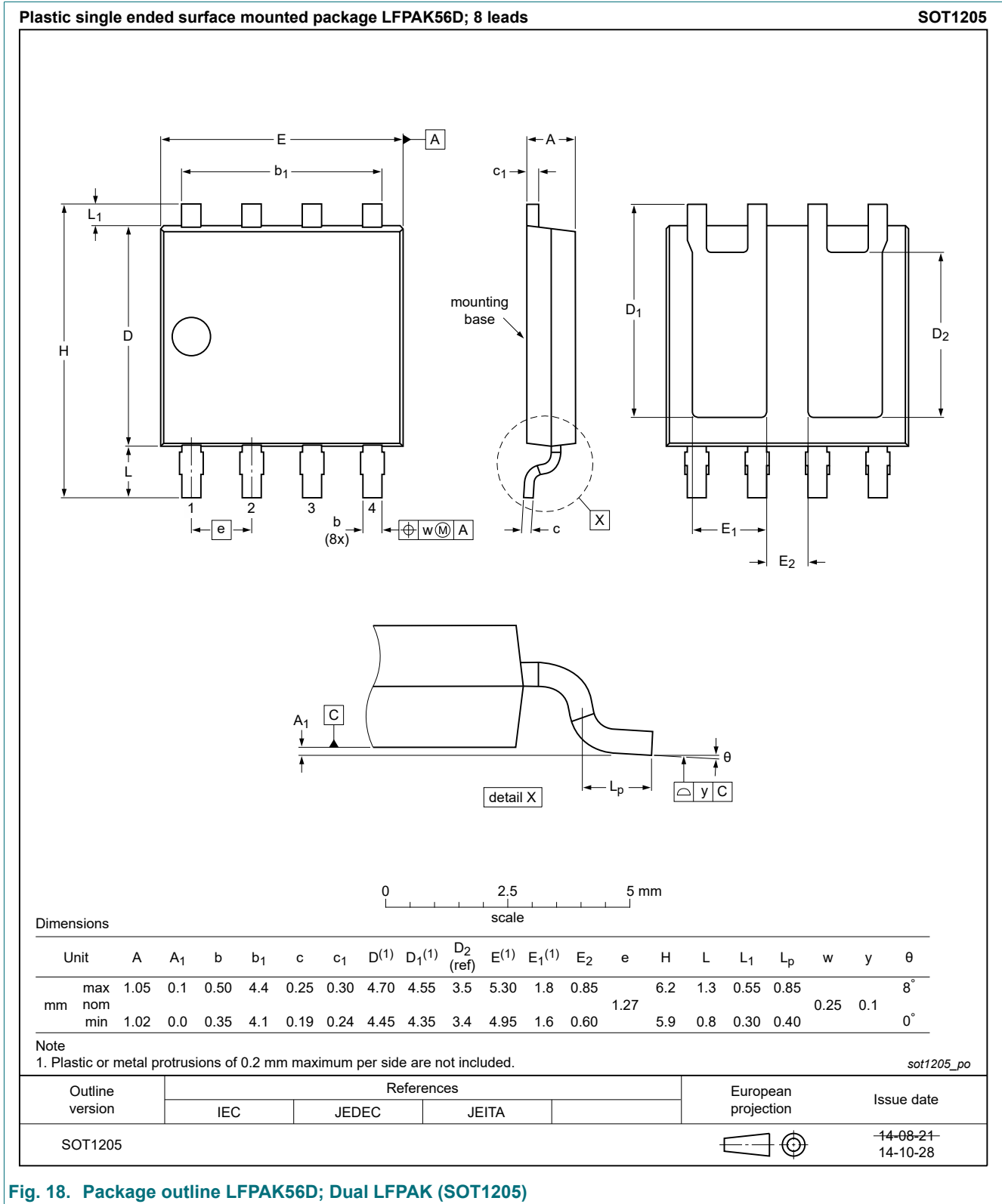


Fig. 18. Package outline LPAK56D; Dual LPAK (SOT1205)

12. Soldering

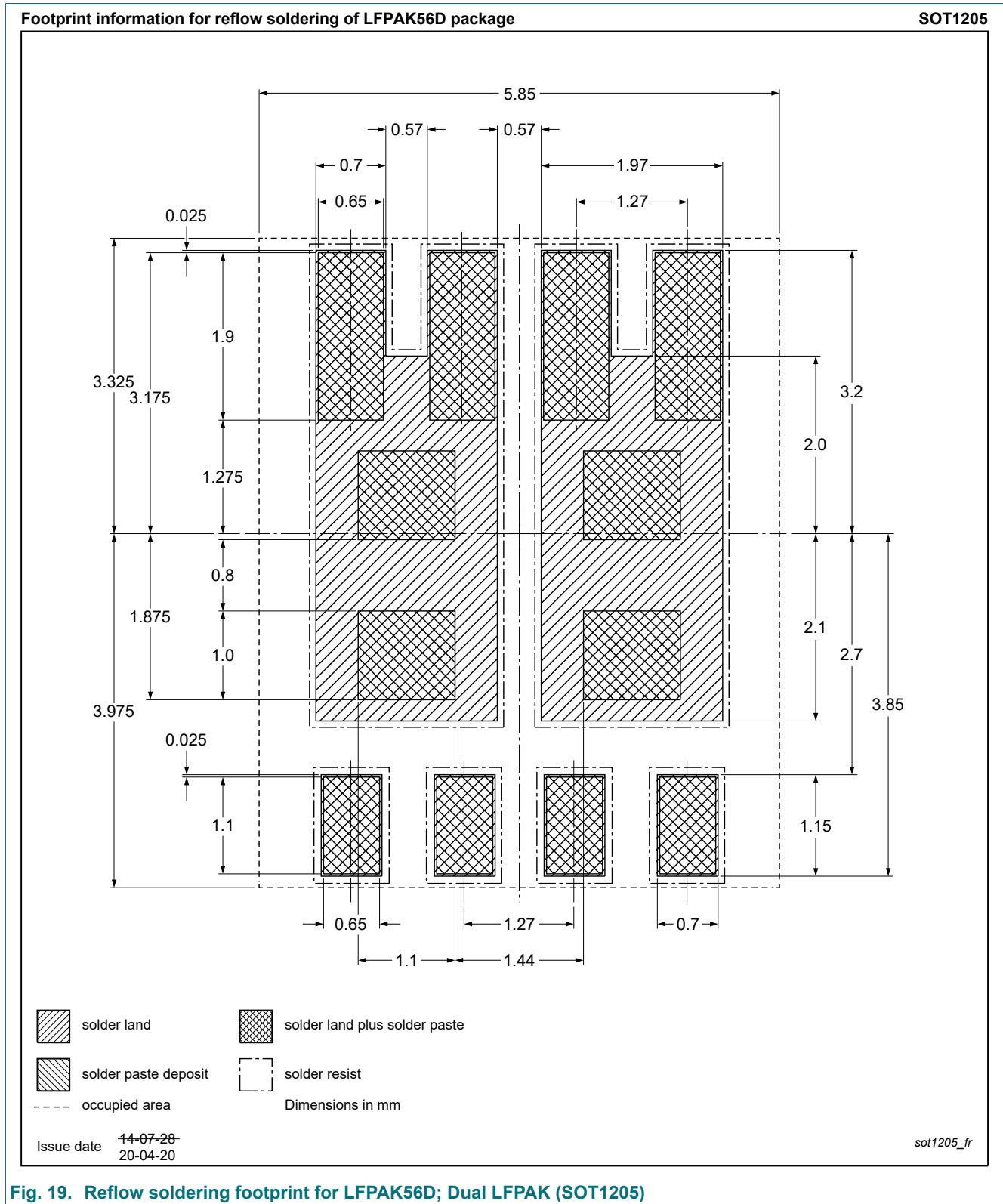


Fig. 19. Reflow soldering footprint for LPAK56D; Dual LPAK (SOT1205)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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