NTE7403
Integrated Circuit
TTL – Quad 2–Input Positive NAND Gate
with Open Collector Outputs

Description:

The NTE7403 contains four independent 2–Input NAND gates in a 14–Lead plastic DIP type package. The open collector outputs require pull–up resistors to perform correctly. They may be connected to other open collector outputs to implement active–low wired–OR or active–high wired–AND functions. Open collector devices are often used to generate higher V_{OH} levels.

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V

DC Input Voltage, V_{IN} 5.5V

Operating Temperature Range, T_A . . . . 0°C to +70°C

Storage Temperature Range, T_{stg} . . . . −65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High–Level Input Voltage	V_{IH}	2.0	–	–	V
Low–Level Input Voltage	V_{IL}	–	–	0.8	V
High–Level Output Voltage	V_{OH}	–	–	5.5	V
Low–Level Output Current	I_{OL}	–	–	16	mA
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −12mA	–	–	−1.5	V
High Level Output Current	I_{OH}	V_{CC} = MIN, V_{IL} =0.8V, V_{OH} = 5.5V	–	–	0.25	mA
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, I_{OL} = 16mA	–	0.2	0.4	V
Input Current	I_I	V_{CC} = MAX, V_I = 5.5V	–	–	0.1	mA

Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under "Recommended Operation Conditions".

Note 3. All typical values are at V_{CC} = 5V, T_A = +25°C.

Electrical Characteristics (Cont'd): (Note 2, Note 3)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High Level Input Current	I_{IH}	V_{CC} = MAX, V_I = 2.4V	–	–	40	μA
Low Level Input Current	I_{IL}	V_{CC} = MAX, V_I = 0.4V	–	–	–1.6	mA
High Level Supply Current	I_{CCH}	V_{CC} = MAX, V_I = 0	–	4	8	mA
Low Level Supply Current	I_{CCL}	V_{CC} = MAX, V_I = 4.5V	–	12	22	mA

Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under "Recommended Operation Conditions".

Note 3. All typical values are at V_{CC} = 5V, T_A = +25°C.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time From A or B Input to Y Output)	t_{PLH}	R_L = 4kΩ, C_L = 15pF	–	35	45	ns
	t_{PHL}	R_L = 400Ω, C_L = 15pF	–	8	15	ns

Truth Table (Each Gate):

Inputs		Output
A	**B**	**Y**
H	H	L
L	X	H
X	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Logic Diagram

A1 — 1
B1 — 2
3 — Y1

A2 — 4
B2 — 5
6 — Y2

$Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$

A3 — 9
B3 — 10
8 — Y3

A4 — 12
B4 — 13
11 — Y4
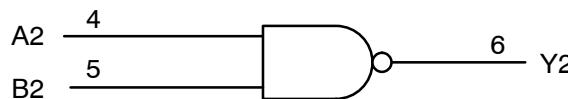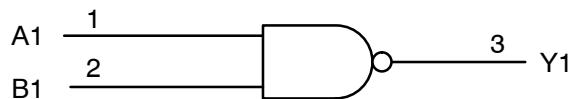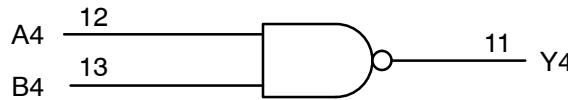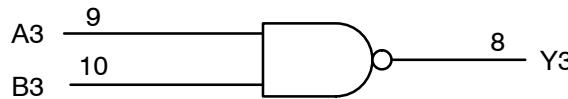
Pin14 = V_{CC}
Pin7 = GND

Pin Connection Diagram

1A	**1**		**14**	V$_{CC}$
1B	**2**		**13**	4B
1Y	**3**		**12**	4A
2A	**4**		**11**	4Y
2B	**5**		**10**	3B
2Y	**6**		**9**	3A
GND	**7**		**8**	3Y

14   8

1   7

.785 (19.95) Max

.200 (5.08) Max

.300 (7.62)

.100 (2.45)

.099 (2.5) Min

.600 (15.24)