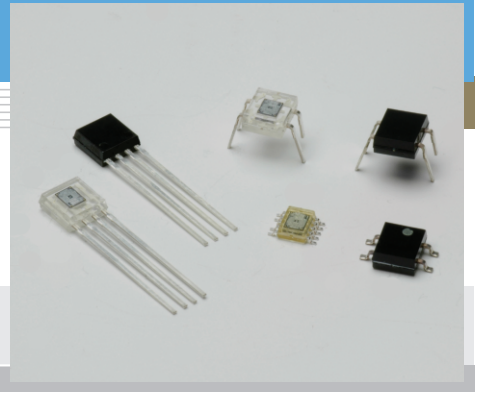


Light modulation photo IC

S4282-51, S6809, S6846, S6986, S7136/-10, S10053



Fewer detection errors even under disturbance background light

These light modulation photo ICs were developed for optical synchronous detection under disturbance background light. A photodiode, preamplifier, comparator, oscillator, LED driver and signal processing circuit, etc. are all integrated on a monolithic photo IC chip. Optical synchronous type photoreflectors and photointerrupters, which less susceptible to disturbance background light, can be easily configured by just connecting an external LED to this photo IC. Our unique circuit design achieves an allowable background light level of 10000 lx Typ. (S4282-51, S6986, S10053) and a minimum detection level of 0.2 μW/mm² Typ. (S6809, S6846, S7136/-10).

Features

- Large allowable background light level
S4282-51, S6986, S10053: 10000 lx Typ.
S6809, S6846, S7136/-10 : 3000 lx Typ.
- Minimum detection level
S4282-51, S6986, S10053: 0.7 μW/mm² Typ.
S6809, S6846, S7136/-10 : 0.2 μW/mm² Typ.
- Digital output (Output appears "L" by light input.)
- Small hysteresis (S6809)
- Small SMD package (S10053)

Applications

- Paper detection in office machine (copiers, fax machines, etc.)
- Optical switch

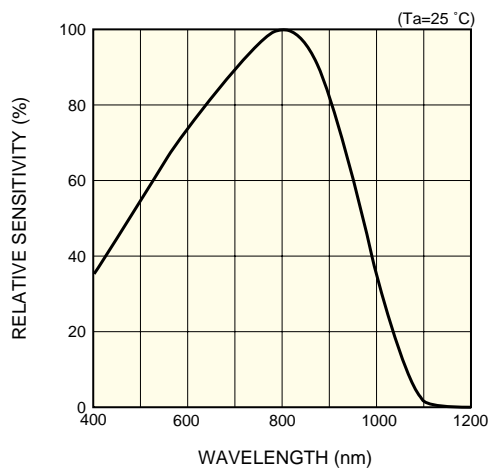
Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	S4282-51, S6986, S10053	S6809, S6846, S7136/-10	Unit
Supply voltage	Vcc	-0.5 to +16		V
Output voltage	Vo	-0.5 to +16		V
Output current	Io	50		mA
Cathode output voltage	Vcath	-0.5 to +16		V
Cathode output current	Icath		70	mA
Power dissipation *1	P	250		mW
Operating temperature	Topr	-25 to +60		°C
Storage temperature	Tstg	-40 to +100		°C

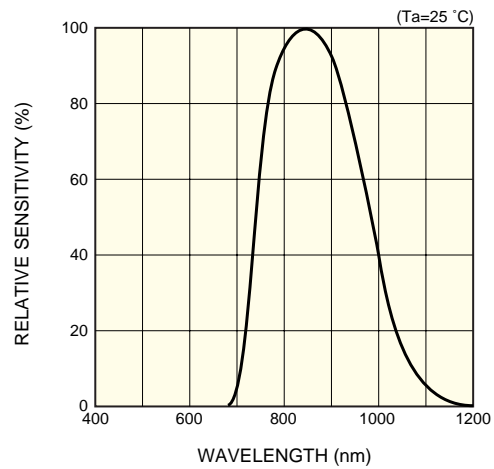
*1: Derate power dissipation at a rate of 3.3 mW/°C above Ta=25 °C

Spectral response (typical example)

S4282-51, S6986, S10053

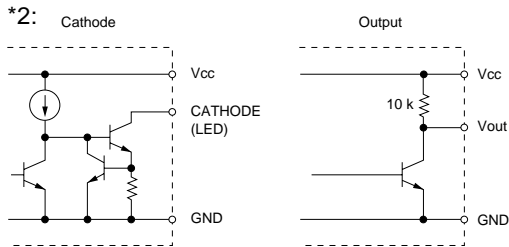


S6809, S6846, S7136/-10

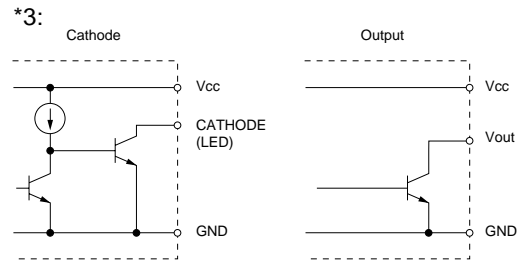


■ Electrical and optical characteristics (Ta=25 °C, Vcc=5 V)

Parameter	Symbol	Condition	S4282-51, S6986, S10053			S6809, S6846, S7136 /-10			Unit
			Output: built-in pull-up resistor *2			Output: open collector *3			
			Cathode: constant current drive			Cathode: open collector drive			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply voltage	Vcc		4.5	-	16	4.5	-	16	V
Current consumption	Icc	Vo, LED terminals open	-	4	11	-	4	11	mA
Output	Low level output voltage	VoL IOL=16 mA	-	0.2	0.4	-	0.2	0.4	V
	High level output voltage	VoH 4.7 kΩ between Vcc and Vo	4.9	-	-	/			V
Cathode	Low level output voltage	Vcath Icath=40 mA	/						4.9
	Low level output current	Icath Vcath=1.2 V				15	35	60	/
	Pulse cycle	Tp	65	130	220	65	130	220	
	Pulse width	Tw	4	8	13.7	4	8	13.7	μs
H→L Threshold light level	EHL	λ=940 nm No background light	-	0.7	2	-	0.2	1.0	μW/mm ²
Hysteresis	-		0.45	0.65	0.95	0.45 (S6809)	0.65 (S6809)	0.95 (S6809)	-
Frequency response	f		0.5	1.25	-	0.5	1.25	-	kHz
Allowable background light level	Ex	Signal light: 5 μW / m ² λp=940 nm Background light: "A" light source	5000	10000	-	2000	3000	-	lx

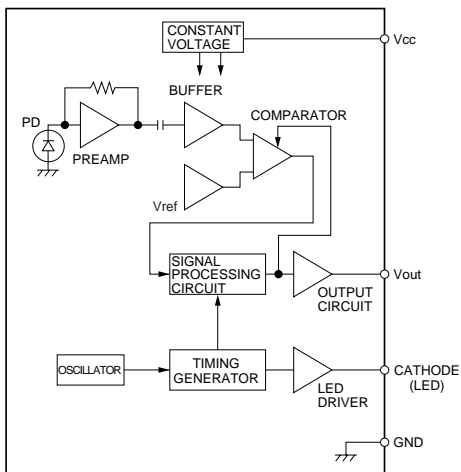


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■ Block diagram and internal functions



TRUTH TABLE

INPUT	OUTPUT LEVEL
LIGHT ON	LOW
LIGHT OFF	HIGH

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(a) Oscillator and timing signal generator

The oscillator produces a reference oscillation output by charging and discharging the built-in capacitor with constant current. The oscillation output is fed to the timing signal generator, which then creates LED drive pulses and various timing pulses for digital signal processing.

(b) LED driver circuit

This circuit drives an external LED using the LED drive pulses created by the timing signal generator. The duty cycle is 1/16.

(c) Photodiode and preamplifier circuit

The photodiode is formed on the same monolithic chip. A photocurrent generated in the photodiode is converted to a voltage by a preamplifier circuit. The preamplifier circuit uses an AC amplifier to expand the dynamic range versus DC or low-frequency background light, without impairing signal detection sensitivity.

(d) Capacitive coupling, buffer amplifier and reference voltage generator

Capacitive coupling removes low-frequency noise and also cancels the DC offset in the preamplifier. The buffer amplifier boosts the signal up to the comparator level, and the reference voltage generator produces a comparator level voltage.

(e) Comparator circuit

The comparator circuit has a hysteresis function to prevent chattering caused by small fluctuations in the input light.

(f) Signal processing circuit

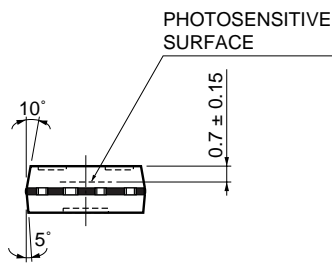
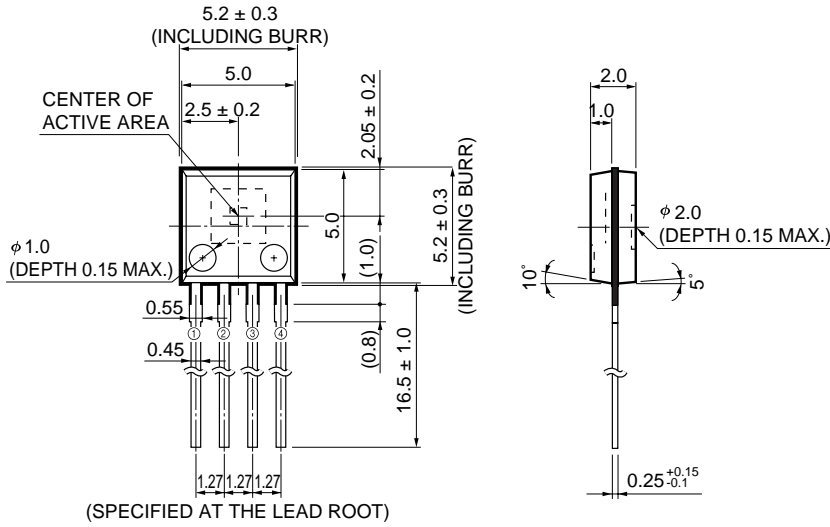
The signal processing circuit consists of a gate circuit and digital integrator circuit. The gate circuit discriminates input pulses during synchronous detection, to prevent operational errors caused by asynchronous background light. Background light which is synchronized with the signal detection timing cannot be eliminated by the gate circuit, but is canceled out by the digital integrator circuit at the latter stage.

(g) Output circuit

This circuit serves as an output buffer for the signal processing circuit and outputs the signal to an external circuit.

■ Dimensional outlines (unit: mm)

S6809, S6846, S6986

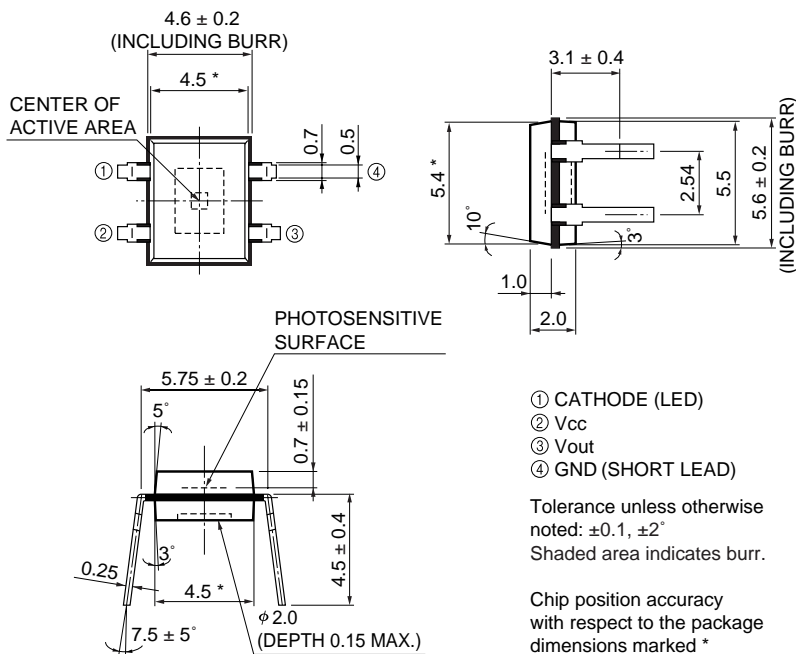


- ① Vout
- ② GND
- ③ CATHODE (LED)
- ④ Vcc

Tolerance unless otherwise noted: ± 0.1 , $\pm 2^\circ$
 Shaded area indicates burr.
 Values in parentheses are not guaranteed, but for reference.

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S4282-51, S7136



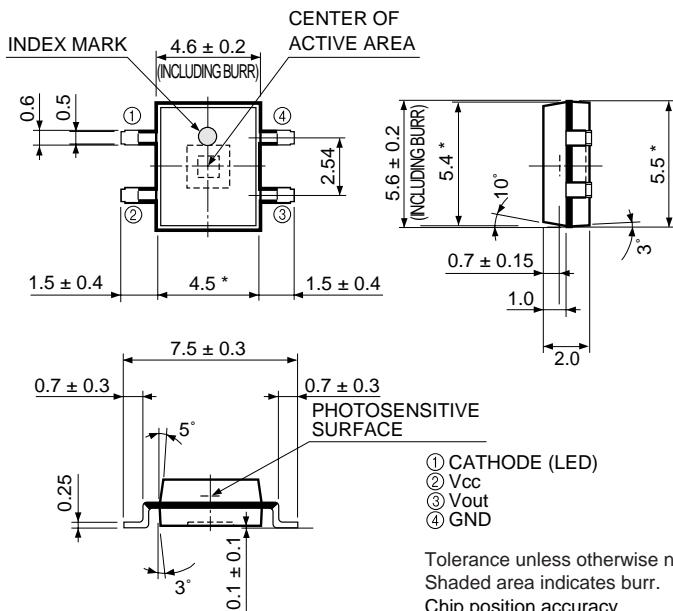
- ① CATHODE (LED)
- ② Vcc
- ③ Vout
- ④ GND (SHORT LEAD)

Tolerance unless otherwise noted: ± 0.1 , $\pm 2^\circ$
 Shaded area indicates burr.

Chip position accuracy with respect to the package dimensions marked *
 $X \leq \pm 0.2$
 $Y \leq \pm 0.2$

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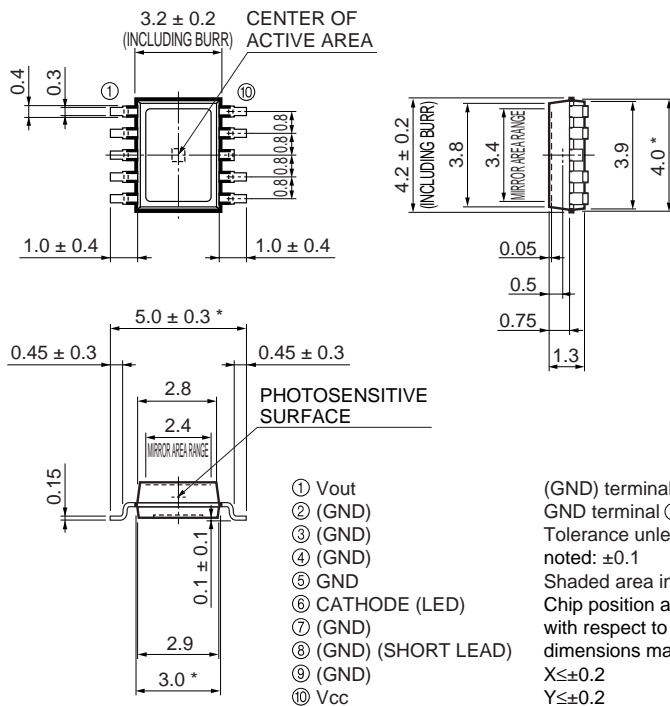
S7136-10



Tolerance unless otherwise noted: ±0.1, ±2°
 Shaded area indicates burr.
 Chip position accuracy with respect to package dimensions marked *
 X ≤ ±0.2
 Y ≤ ±0.2

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S10053



(GND) terminals should be connected to GND terminal ⑤ on board.
 Tolerance unless otherwise noted: ±0.1
 Shaded area indicates burr.
 Chip position accuracy with respect to the package dimensions marked *
 X ≤ ±0.2
 Y ≤ ±0.2

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