# TDA38740/25 OptiMOS iPOL

## 40/25A Single-voltage Synchronous Buck Regulator with PMBus

## Quality Requirement Category: Industrial

## Features

- Single 4.5 V to 17 V application or Wide Input Voltage Range from 3.0 V to 17 V with external Vcc
- Output Voltage Range: 0.25 V to 5 V based on Output Feedback Divider Network
- Enhanced Fast COT Engine Stable with Ceramic output Capacitors without External Compensation
- Pin programmable Output Voltage, Switching Frequency/mode selection with 16 unique selectable settings
- Programmable Switching Frequency from 400 kHz - 2 MHz in steps of 200 kHz, excluding 1600 kHz
- Monotonic Start-Up with Selectable Soft-Start Time through PMBus & Pre-Bias Start-Up
- Thermally Compensated Internal Over Current Protection with Eight Unique Selectable Settings
- Enable input with Voltage Monitoring Capability & Power Good Output
- PMBus system interface for reporting of Temperature, Voltage, Current & Power telemetry
- Multiple Time Programming (MTP) with up to 24 writes for the USER section
- Digitally programmable load-line without any external components
- Thermal Shut Down
- Operating junction temp: -40 °C < Tj < 125 °C
- Small Size: 5 mm x 6 mm PQFN
- Lead-free, Halogen-free and RoHS2 Compliant with Exemption 7a

## Applications

- Server Applications
- Storage Applications
- Telecom & Datacom Applications
- Distributed Point of Load Power Architectures

## Description

The TDA38740/725 is an easy-to-use, fully integrated and highly efficient dc-dc regulator. The onboard PWM controller and OptiMOS™ FETs with integrated bootstrap diode make TDA38740/725 a small footprint solution, providing high-efficiency power delivery. Furthermore, it uses a fast Constant On-Time (COT) control scheme, which simplifies the design efforts and achieves fast transient response.

TDA38740/725 is a versatile regulator, operating with wide input and output voltage ranges, offering programmable switching frequency from 400 kHz to 2 MHz, and providing eight unique selectable current limits. It features a programmable dc loadline, which provides an additional tool to manage the transient response.

It also features important protection functions, such as pre-bias start-up, thermally compensated current limit, over voltage and under voltage protection, and thermal shutdown to give required system level security in the event of fault conditions. The device configuration can be easily defined using Infineon's XDP Designer GUI and is stored in the on-chip memory. The controller requires the fewest possible external components and results in a simplified Bill of Materials (BOM).

# Contents

# 1 Ordering Information

**Table 1 Ordering Information**

| Base Part Number | Package Type | Standard Pack Form and Qty | | Orderable Part Number |
|---|---|---|---|---|
| TDA38740 | QFN 5 mm x 6 mm | Tape and Reel | 5000 | TDA38740aabbAUMA1 |
| TDA38725 | QFN 5 mm x 6 mm | Tape and Reel | 5000 | TDA38725aabbAUMA1 |

TDA38740-aabb
- Configuration File Identifier
- Customer Identifier

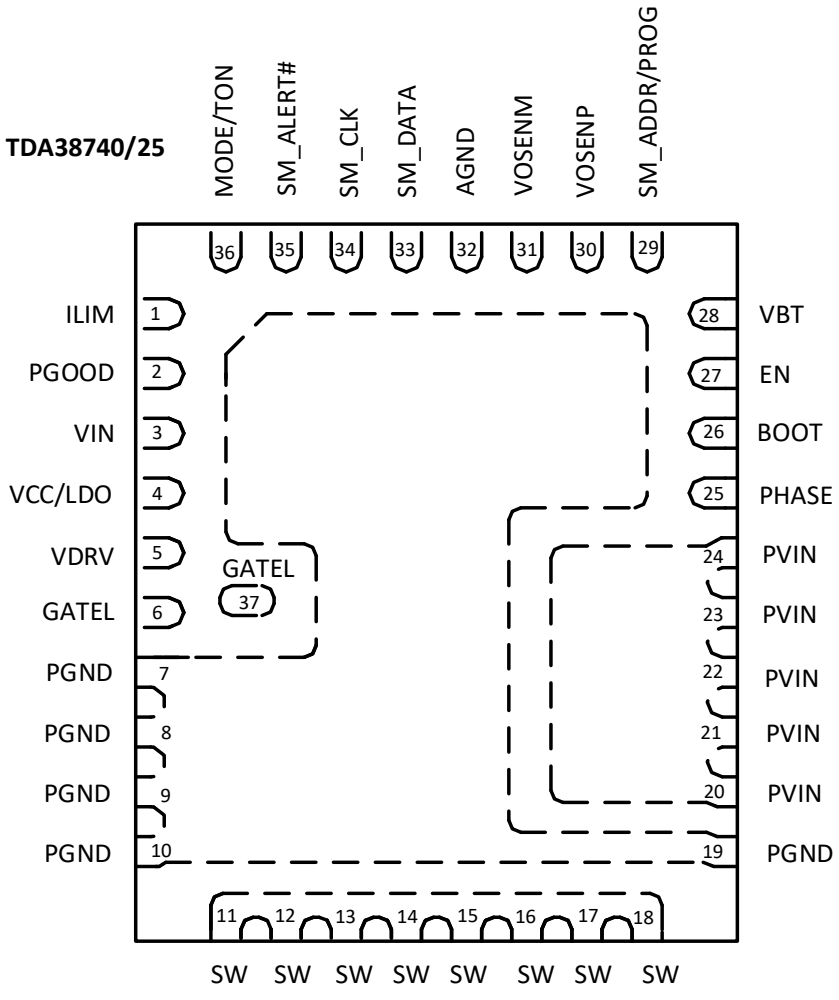



**Figure 1 Package Top View**

# 2 Functional Block Diagram

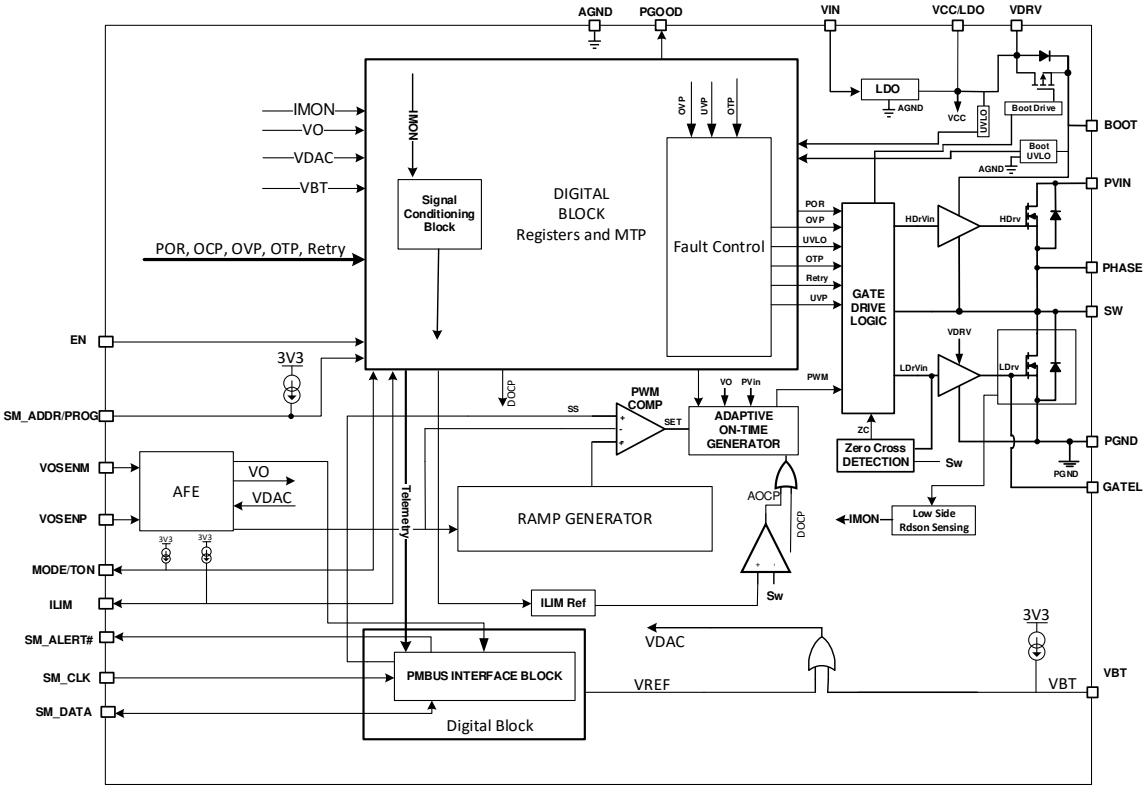



**Figure 2 Block Diagram**

# 3 Typical Application Diagram

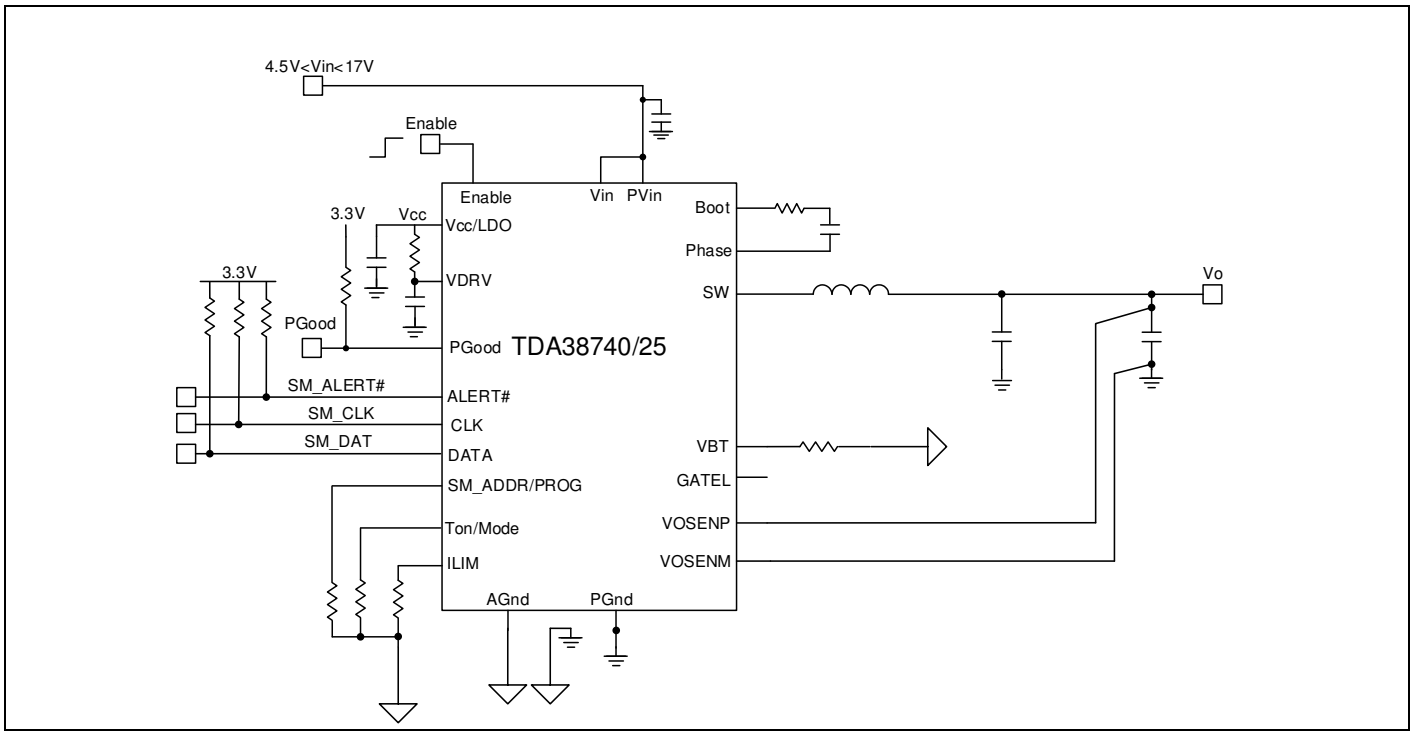



**Figure 3 TDA38740/725 application circuit for Vout< 2.5 V**

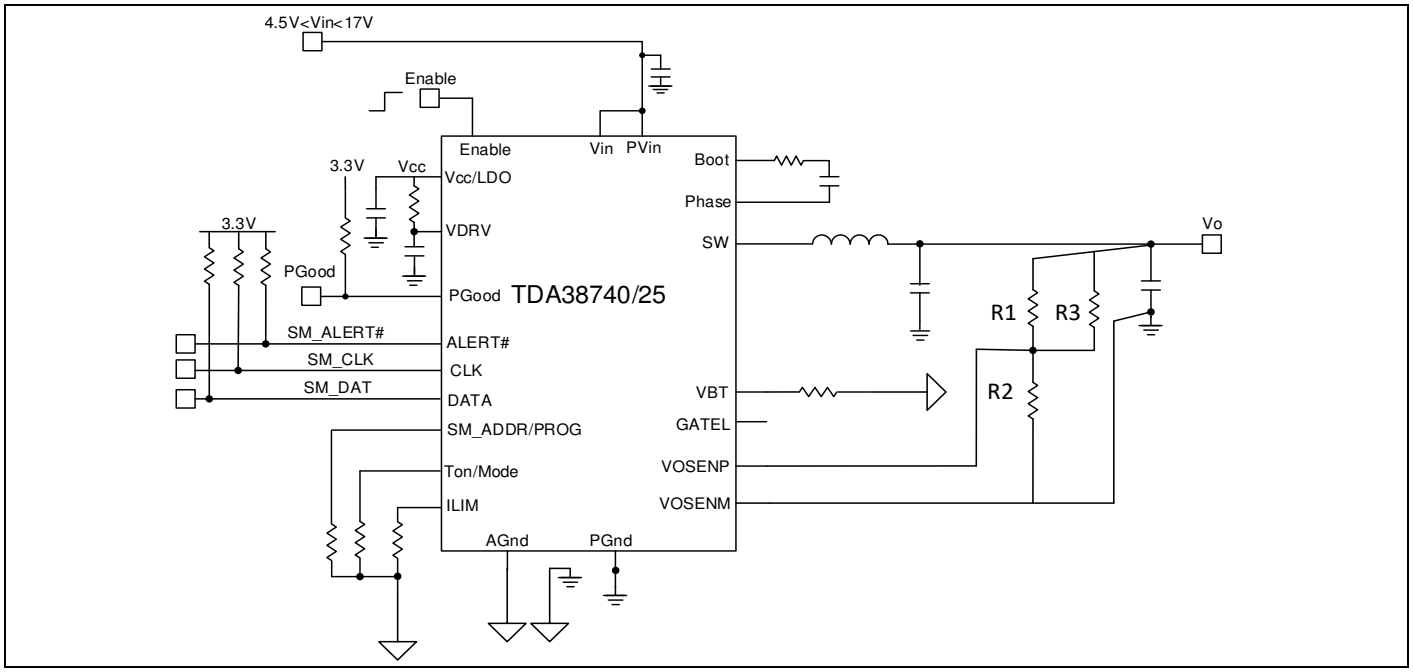



**Figure 4 TDA38740/725 application circuit for Vout> 2.5 V**

# 4 Pin Descriptions

**Table 2 Pin Descriptions**

| Pin# | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 1 | ILIM | A[I] | Connect a resistor to ground to set Over Current Protection (OCP) limit. Eight user selectable OCP limits are available. |
| 2 | PGood | D[O] | Power Good status output pin is open drain. Connect a pull up resistor from this pin to an external bias voltage. |
| 3 | VIN | A[I] | Input voltage for an Internal LDO. A 4.7 uF capacitor should be connected between this pin and PGND. If an external supply is connected to theVcc/LDO pin, this pin should be shorted to the Vcc/LDO pin and a 2.2 uF ceramic capacitor can be shared with Vin and Vcc/LDO. |
| 4 | Vcc/LDO | A[P] | Input bias for an external Vcc voltage /Output of the internal LDO. A 2.2 uF ceramic capacitor is recommended to use between Vcc, VDRV and the Power ground (PGND). An optional decoupling capacitor can be placed between Vcc/LDO and AGND. Connect to external supply when internal LDO not being used. |
| 5 | VDRV | A[P] | VDRV should be shorted to the Vcc/LDO pin on the PCB. A 2.2 uF ceramic capacitor is recommended to use between VDRV, Vcc/LDO and the Power ground (PGND). Connect to external supply when internal LDO not being used. |
| 6, 37 | GATEL | A [O] | Gate of Low-side FET. The signal on this pin should be used for test purposes only and should not have external components connected to it. Leave it opened if not used. |
| 7, 8, 9, 10, 19 | PGND | - | Power Ground. Should be connected to the system's power ground plane. PGND and AGND are internally connected via the lead frame. |
| 11, 12, 13, 14, 15, 16, 17, 18 | SW | A [O] | Switch Node. Connect these pins to an output inductor. |
| 20, 21, 22, 23, 24 | PVin | A [P] | Input supply for the power stage. |
| 25 | Phase | A [O] | Source of High-side FET. Connect a bootstrap capacitor between this pin and the Boot pin. A high temperature (X7R) 0.1 uF or greater value ceramic capacitor is recommended. |
| 26 | Boot | A [I] | Supply voltage for the high side driver. Connect this pin to the Phase pin of the regulator through a bootstrap capacitor. |
| 27 | EN | A [I] | Enable pin to turn the IC on and off. Leave it open or ground it when not used |
| 28 | VBT | A[I] | A resistor from this pin to ground defines the default boot voltage that the part will boot up in. |
| 29 | SM_ADDR/PROG | D[I] | PMBus Slave Address and PROG pin. A resistor to ground on this pin points to one of the unique sixteen PMBus slave devices which needs to be addressed on the board. The same address also defines the specific configuration file that will be loaded into the OTP during power-up. |

## Pin Descriptions

| Pin# | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 30 | VOSENP | A [I] | Output voltage feedback pin. Connect this pin to the output of the regulator to regulate the output voltage. |
| 31 | VOSENM | A [I] | The pin provides the return path for the remote voltage sensing. It is used as a reference for the Analog Front End (AFE) |
| 32 | AGND | - | Signal ground for the internal circuitry. AGND to be connected to PGND on the PCB. |
| 33 | SM_DATA | D [B] | Serial data line I/O. PMBus bi-directional serial data line. Leave the pin open or ground it if not being used. |
| 34 | SM_CLK | D [I] | Serial Clock Line Input. PMBus serial clock input. The interface is rated to max of 1 MHz. Leave the pin open or ground it if not being used. |
| 35 | SM_ALERT# | D [O] | SMB Active low alert line. Leave the pin open if not being used. |
| 36 | TON/Mode | D [I] | Multi-function pin. This pin can be used to select one of eight switching frequencies, and FCCM or DEM mode by connecting a resistor from this pin to ground. |

# 5 Absolute Maximum Ratings

**Table 3 Absolute Maximum Ratings**

| Description | Symbol | Values | | | Unit | Note/ Test Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Input voltage | $V_{PVIN}$ | -0.3 | - | 25 | V | Note 1, PVIN Pin |
| LDO Input voltage | $V_{IN}$ | -0.3 | - | 25 | V | Note 1, VIN Pin |
| Enable voltage | $V_{EN}$ | -0.3 | - | 25 | V | EN Pin |
| PVIN-PHASE voltage | $V_{PVIN}$ -$V_{PHASE}$ | Below -5 V for 5 ns, -0.3 V dc | - | 34 V for 1 ns, 25 V dc | V | PVIN-PHASE pin |
| VIN-PHASE voltage | $V_{VIN}$-$V_{PHASE}$ | Below -5 V for 5 ns, -0.3 V dc | - | 34 V for 1 ns, 25 V dc | V | VIN-PHASE pin |
| PVIN-Switch Node voltage | $V_{PVIN}$ -$V_{SW}$ | Below -5 V for 5 ns, -0.3 V dc | - | 34 V for 1 ns, 25 V dc | V | PVIN- SW Pin |
| Internal Driver voltage | $V_{DRV}$ | -0.3 | - | 6 | V | Note 1, VCC/VDRV Pin |
| Gate Low Pin voltage | $V_{GATEL}$ | -0.3 | - | 6 | V | GateL Pin |
| BOOT voltage | $V_{BOOT}$ | Below -0.3 V for 5 ns, -0.3 V dc | - | 29 V dc | V | BOOT Pin |
| | $V_{BOOT}$ - $V_{PHASE}$ | -0.3 | - | 7 V for 5 ns, 6 V dc | V | BOOT – PHASE Pin |
| Switch Node voltage | $V_{SW}$ | Below -5 V for 5 ns, -0.3 V dc | - | 34 V for 1 ns, 25 V dc | V | Switch Node Pin |
| Phase Node voltage | $V_{PHASE}$ | Below -5 V for 5 ns, -0.3 V dc | - | 34 V for 1 ns, 25 V dc | V | Phase Pin |
| Address/PROG voltage | $V_{SM\_ADDR/PROG}$ | -0.3 | - | 3.6 | V | Note 1, SM_ADDR/PROG Pin |
| Output Positive Sense voltage | $V_{VOSENP}$ | -0.3 | - | 3.6 | V | Note 1, VOSENP Pin |
| Output Negative Sense voltage w.r.t AGND | $V_{VOSENM}$ | -0.3 | - | 0.3 | V | Note 1, VOSENM Pin |
| Voltage Regulator Power Good | $V_{PGOOD}$ | -0.3 | - | 3.6 | V | Note 1, PGOOD Pin |
| ILIM Voltage | $V_{ILIM}$ | -0.3 | - | 3.6 | V | Note 1, ILIM Pin |
| TON/ MODE voltage | $V_{TON/MODE}$ | -0.3 | - | 3.6 | V | Note 1, TON/MODE Pin |
| VBT voltage | $V_{VBT}$ | -0.3 | - | 3.6 | V | Note 1, VBT voltage pin |
| Power GND w.r.t Analog GND voltage | $V_{PGND}$- $V_{AGND}$ | -0.3 | - | 0.3 | V | PGND – AGND Pin |
| SM CLK voltage | $V_{SM\_CLK}$ | -0.3 | - | 3.6 | V | SM_CLK Pin |
| SM Data voltage | $V_{SM\_DAT}$ | -0.3 | - | 3.6 | V | SM_DAT Pin |

## Absolute Maximum Ratings

| Description | Symbol | Values | | | Unit | Note/ Test Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| SM Alert voltage | $V_{SM\_ALERT\#}$ | -0.3 | - | 3.6 | V | SM_ALERT# Pin |
| Juntion Temperature | $T_{Jmax}$ | -40 | - | 150 | °C | - |
| Storage Temperature | $T_{STORAGE}$ | -55 | - | 150 | °C | - |

*Note:*

*1. PGND and AGND pins should be connected together on the PCB.*

***Attention: Stresses beyond these listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.***

# 6 Thermal Characteristics

**Table 4 Thermal Characteristics**

| Description | Symbol | Values | Test Conditions |
|---|---|---|---|
| Junction to Ambient Thermal Resistance | $\theta_{JA}$ | 19 °C/W | Note 2 |
| Junction to PCB Thermal Resistance | $\theta_{JC\text{-}PCB}$ | 1.1 °C/W | Note 3 |
| Junction to Case Top Termal Resistance | $\theta_{JC}$ | 24 °C/W | |

*Note:*

2. *Thermal resistance is measured with components mounted on a standard EVAL_TDA38740_1.2Vout demo board in free air*
3. *Thermal resistance is based on the board temperature near pin 22*

# 7 Electrical Specifications

**Table 5 Recommended Operating Conditions for Reliable Operation with Margin**

| Description | Min | Max | Unit | Note |
|---|---|---|---|---|
| PVin Voltage Range with External Vcc | 3 | 17 | V | Note 4, Note 5 |
| PVin Voltage Range with Internal LDO | 4.5 | 17 | V | Note 5 , Note 6 & Note 10 |
| Vcc Supply Voltage Range | 4.5 | 5.5 | V | Note 4 , Note 7 |
| Output Voltage Range | 0.25 | 5.12 | V | Note 8 |
| Continuous Output Current Range for TDA38740 | | 40 | A | Note 9 |
| Continuous Output Current Range for TDA38725 | | 25 | A | Note 9 |
| Switching Frequency (excluding 1600 kHz) | 400 | 2000 | kHz | Note 10 |
| Operating Junction Temperature | -40 | 125 | °C | |

*Note:*

4. *VCC/VDRV pin is connected to an external bias voltage when Pvin is less than 4.5 V*
5. *A common practice is to have 20% margin on the maximum SW node voltage in the design. For applications requiring PVin equal to or above 14 V, a small resistor in series with the Boot pin should be used to ensure the maximum SW node spike voltage does not exceed absolute maximum specs. Alternatively, a snubber can be used at SW node to reduce the SW node spike.*
6. *$PV_{in}$ with internal LDO is used. For single-rail applications with the internal LDO and $PV_{in}$ = 4.5 V-5.4 V, the internal LDO may enter dropout mode. AOCP limits can be reduced due to the lower VCC voltage.*
7. *The TDA38740/725 is designed to function with VCC down to 4.5 V. However, electrical specifications such as AOCP limits may be degraded.*
8. *The maximum output voltage is limited by the minimum off-time. For output voltages above 2.56 V an external feedback resistor divider is needed.*
9. *Refer to Section 15.1 for maximum output current rating at different ambient temperature and OCP threshold tolerance*
10. *The maximum LDO output current must be limited within 50 mA for operations requiring the full operating temperature range of -40 °C ≤ $T_J$ ≤ 125 °C. Thermal De-rating may be needed at an elevated ambient temperature to ensure the junction temperature remains within the recommended operating range.*

## 7.1 Electrical Characteristics

Unless otherwise specified, these specifications apply over, 4.5 V ≤ Vin = PVin ≤ 17 V, in 0 °C < $T_J$ < 125 °C. Typical values are specified at Ta = 25 °C.

**Table 6 Electrical Characteristics**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Power Stage** | | | | | | |
| Top Switch | $R_{ds(on)\_Top}$ | VBoot – Vsw= 5.0 V, Io = 35 A, Tj =25 °C | - | 2.9 | - | mΩ |
| Bottom Switch | $R_{ds(on)\_Bot}$ | Vcc = 5.0, Io= 35 A, Tj =25 °C | - | 1.00 | - | mΩ |
| Bootstrap Diode Forward Voltage | | I(Boot) = 25 mA | - | 780 | 950 | mV |
| SW Leakage Current | $I_{SW}$ | SW = 0 V, EN = 0 V | - | - | 175 | µA |
| | | SW = 0 V, EN = high, No Switching | - | - | 175 | µA |
| Dead Band Time | $T_{db}$ | SW Node rising edge, 40 A , Internal LDO, $T_j$=25 °C, Note 11 | - | 10 | - | ns |
| | | SW Node falling edge, 40 A , Internal LDO, $T_j$=25 °C, Note 11 | - | 10 | - | ns |
| **Supply Voltage** | **Vin** | | | | | |
| PVin range (using external VCC = 5V) | | | - | 3-17 | - | V |
| Vin Range (using internal LDO) | | Fsw = 600 kHz | - | 4.5 -17 | - | V |
| | | Fsw = 2000 kHz | - | 4.5 –17 | - | V |
| Vin range (when VIN=VCC) | | | 4.5 | 5 | 5.5 | V |
| **Supply Current** | **Iin** | | | | | |
| PVin Supply Current (standby)(External Vcc) | $I_{in\ (Standby)}$ | EN = Low, No Switching, Note 11 | - | 2 | - | mA |
| PVin Supply Current (dynamic)(External Vcc) | $I_{in\ (Dyn)}$ | EN = High, Fs = 800kHz, Vin=PVin=12 V, Vout =1.1 V, Note 11 | - | 15 | - | mA |
| PVin Supply Current (standby)(Internal Vcc) | $I_{in\ (Standby)}$ | EN = Low, No Switching, Note 11 | - | 12 | - | mA |
| PVin Supply Current (dynamic)(Internal Vcc) | $I_{in\ (Dyn)}$ | EN = High, Fs = 800kHz, Vin=PVin=12 V, Vout =1.1 V, Note 11 | - | 48 | - | mA |
| **Digital Inputs - LVTTL** | **SM_DAT, SM_CLK** | | | | | |

## Electrical Specifications

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input High Voltage | | | 1.35 | - | - | V |
| Input Low Voltage | | | - | - | 0.8 | V |
| Input Leakage | | | - | - | -1 | µA |
| Pin Capacitance | | See Note 11 | - | - | 4 | pF |
| **Remote Voltage Sense Inputs** | **VOSENP, VOSENM** | | | | | |
| VOSENP Input Current | | VOSENP = 3.6 V | - | - | 230 | µA |
| | | VOSENP = -0.3 V | -85 | - | - | µA |
| VOSENM Input Current | | VOSENM = 0.3 V | -155 | - | - | µA |
| | | VOSENM = -0.3 V | -200 | - | - | µA |
| Differential Input Voltage Range | | | - | - | 2.56 | V |
| VOSENM Input CM Voltage | | | - | ±300 | - | mV |
| **TON/MODE** | | | | | | |
| Output Current | | | - | 100 | - | µA |
| **VBT/ILIM/SM_ADDR** | | | | | | |
| Output Current | | | - | 15 | - | µA |
| **Open-Drain Outputs-20mA Drive** | **SM_CLK, SM_DAT, SM_ALERT#** | | | | | |
| Output Low Voltage | | I = 20 mA | - | - | 0.26 | V |
| On Resistance | | I = 20 mA | - | 7 | - | Ω |
| Tri-State Leakage | | | - | - | ±5 | µA |
| **On-Time Timer Control** | | | | | | |
| Frequency Range (programmable) | | Excluding 1600 kHz and in steps of 200 kHz | 400 | -- | 2000 | KHz |
| Minimum On-Time | | Vin=12 V, Vo=0 V, Note 11 | - | 25 | - | ns |
| Minimum Off-Time | Toff(Min) | Tj=25°C, VFB=0 V, Note 11 | - | 150 | - | ns |
| **VCC LDO Output** | **Vcc** | | | | | |
| System Accuracy 5 mV step mode voltage | Vcc | 5.5 V ≤ Vin ≤ 17 V, when Icc =50 mA, Cload = 2.2 uF | 4.7 | 5.0 | 5.3 | V |
| VCC Dropout | Vcc_drop | Vin = 4.5 V, Icc=50 mA, Cload=2.2uF | - | 650 | - | mV |
| **Under Voltage Lockout** | | | | | | |

## Electrical Specifications

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Vcc-Start Threshold | VCC_UVLO_Start | Vcc Rising Trip Level | 3.55 | 3.7 | 3.95 | V |
| Vcc-Stop Threshold | VCC_UVLO_Stop | Vcc Falling Trip Level | 3.4 | 3.6 | 3.8 | |
| Enable-Start-Threshold | Enable_UVLO_Start | Ramping up | 0.605 | 0.65 | 0.695 | V |
| Enable-Stop-Threshold | Enable_UVLO_Stop | Ramping down | 0.505 | 0.55 | 0.595 | |
| **Over Current Limit** | | | | | | |
| TDA38740 Current Limit Threshold (Valley Current) | $I_{oc}$ | Tj = 25 °C, Vcc =5.0 V, | - | 10 | - | A |
| | | | - | 15 | - | |
| | | | - | 20 | - | |
| | | | - | 25 | - | |
| | | | - | 30 | - | |
| | | | - | 40 | - | |
| | | | - | 50 | - | |
| | | | - | 60 | - | |
| TDA38725 Current Limit Threshold (Valley Current) | $I_{oc}$ | Tj = 25 °C, Vcc =5.0 V, | - | 10 | - | A |
| | | | - | 15 | - | |
| | | | - | 20 | - | |
| | | | - | 25 | - | |
| | | | - | 25 | - | |
| | | | - | 25 | - | |
| | | | - | 25 | - | |
| | | | - | 25 | - | |
| **Over Voltage Protection** | | | | | | |
| Fixed OVP Threshold (Programmable) | OVP_Vth | In VOUT_SCALE_LOOP 1:1 mode, 8 Discrete Options | - | 0.8 | - | V |
| | | | - | 1.0 | - | |
| | | | - | 1.2 | - | |
| | | | - | 1.35 | - | |
| | | | - | 1.5 | - | |
| | | | - | 1.8 | - | |
| | | | - | 2.2 | - | |
| | | | - | 2.85 | - | |
| | | In VOUT_SCALE_LOOP 1:2 mode, 8 Discrete Options. Note 11 | - | 1.6 | - | V |
| | | | - | 2.0 | - | |
| | | | - | 2.4 | - | |
| | | | - | 2.7 | - | |
| | | | - | 3.0 | - | |
| | | | - | 3.6 | - | |
| | | | - | 4.4 | - | |
| | | | - | 5.7 | - | |

## Electrical Specifications

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Fixed OVP Threshold Accuracy | | | -5 | | +5 | % |
| Relative OVP Threshold (programmable) | | Relative to Vout in steps of 50 mV in VOUT_SCALE_LOOP 1:1 mode | 50 | - | 400 | mV |
| | | Relative to Vout in steps of 50 mV VOUT_SCALE_LOOP 1:2 mode | 100 | - | 800 | mV |
| Output Relative OVP Threshold Accuracy | | VOUT_SCALE_LOOP 1:1 | - | ±100 | - | mV |
| | | VOUT_SCALE_LOOP 1:2 | - | ±200 | - | mV |
| **Under Voltage Protection** | | | | | | |
| UVP Trip Threshold | UVP_Vth | Relative to Vout in steps of 50 mV in VOUT_SCALE_LOOP 1:1 mode | 50 | - | 400 | mV |
| | | Relative to Vout in steps of 50 mV in VOUT_SCALE_LOOP 1:2 mode | 100 | - | 800 | mV |
| Output Relative UVP Threshold Accuracy | | VOUT_SCALE_LOOP 1:1 | - | ±100 | - | mV |
| | | VOUT_SCALE_LOOP 1:2 | - | ±200 | - | mV |
| **IMON Reporting Accuracy** | | | | | | |
| IMON Accuracy | Imon | Vin = 12 V, Vout = 1.2 V, Iout = 40 A | - | ±6 | - | % |
| **Power Good** | **Pgood** | | | | | |
| Pgood Sink Current | $I_{PG}$ | $V_{PG}$ = 0.5 V, Rpull-up = 500 Ω to 3.3 V | - | 5 | 6 | mA |
| Pgood Open Drain Leakage Current | | $V_{PG}$ = 3.3 V | - | - | 1 | µA |
| Pgood Low Voltage | $V_{PG}$ | Vin = Vcc = 5 V, Rpull-up = 5 kΩ to 3.3 V, I = 6 mA | - | - | 0.1 | V |
| Pgood Low Voltage | $V_{PG}$ | Vin = Vcc = 0 V, Rpull-up = 5 kΩ to 3.3 V, I = 6 mA | - | - | 0.5 | V |
| **Thermal Shutdown** | | | | | | |
| Thermal Shutdown | | Note 7 | - | 140 | - | °C |
| Hysteresis | | | - | 20 | - | |
| **PMBus Reporting** | | | - | | - | |
| Bus Speed | | Normal | - | 100 | - | kHz |
| | | Fast | - | 400 | - | kHz |

## Electrical Specifications

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | High-Speed | - | 1000 | - | kHz |
| Output Voltage Resolution | | | - | 0.244,<br>0.488,<br>0.977,<br>1.953,<br>3.906 | - | mV |
| Output Voltage Filter Rate | | | - | 8 | - | kHz |
| Output Voltage Update Rate | | | - | 379 | - | kHz |
| Highest Reported Vout | | VOUT_SCALE_LOOP=1:1 | - | - | 2.56 | V |
| | | VOUT_SCALE_LOOP=1:2 | - | - | 5.12 | V |
| Vout Reporting Accuracy | | -40 °C-125 °C (Tj),<br>4.5 V<Vcc<5.5 V,<br>Note 11 & 12 | -1 | - | 1 | % |
| Iout Resolution | | | - | 0.0625 | - | A |
| Iout Filter Rate | | | - | 8 | - | kHz |
| Iout Update Rate | | | - | 379 | - | kHz |
| Iout Digital Monitoring Range | | | - | - | 64 | A |
| Iout Accuracy (PMBus) | | 0 °C-125 °C,<br>4.5 V<Vcc<5.5 V<br>0 A ≤ Iout ≤ 40 A<br>0.25 V ≤ Vout ≤ 2.52 V | - | ±6 | - | % |
| Temperature Resolution | | | - | 1 | - | °C |
| Temperature Filter Rate | | | - | 4 | - | kHz |
| Temperature Update Rate | | | - | 189 | - | kHz |
| Temperature Monitoring Range | | | -40 | - | 125 | °C |
| Temperature Reporting Accuracy | | Note 11 | - | ±1 | - | °C |
| **PMBus Interface Timing Specifications** | | | | | | |
| Data Rising Threshold | | | 0.997 | - | 1.208 | V |
| Data Falling Threshold | | | 0.839 | - | 1.057 | V |
| Clock Rising Threshold | | | 0.996 | - | 1.201 | V |
| Clock Falling Threshold | | | 0.836 | | 1.057 | V |
| Data pulldown resistance | | | 5 | - | 13 | Ω |

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SMALERT# pulldown resistance | | | 5 | - | 20 | Ω |

*Note: .*

11. *Guaranteed by design and not tested in production*
12. *Cold temperature performance is guaranteed via correlation using statistical quality control. Not tested in production.*
13. *FOVP, ROVP and RUVP threshold accuracies for VOUT_SCALE_LOOP 1:2 are based on the use of an output divider as specified in section 13.3.*

# 8 Pin Strap Resistors Application Information

The tables and descriptions below detail different parameters that can be set using pin strap resistor.

**Table 7 TON/MODE Table**

| Bin | TON/MODE (kΩ) | Freq (kHz) | MODE |
|---|---|---|---|
| 0 | SHORT | 600 | FCCM |
| 1 | 2.49 | 1000 | |
| 2 | 3.24 | 1400 | |
| 3 | 4.02 | 2000 | |
| 4 | 4.87 | 1200 | DEM |
| 5 | 5.76 | 1400 | |
| 6 | 6.81 | 1800 | |
| 7 | 7.87 | 2000 | |
| 8 | 9.09 | 400 | |
| 9 | 10.5 | 600 | |
| 10 | 12.1 | 800 | |
| 11 | 14 | 1000 | |
| 12 | 15.8 | 400 | FCCM |
| 13 | 17.8 | 1800 | |
| 14 | 20 | 1200 | |
| 15 | FLOAT | 800 | |

When operating in the pin strap resistor mode the switching frequency and the mode can be set by connecting a resistor from MODE/TON pin to GND per table above. Switching frequency can be selected from 400kHz to 2000kHz in steps of 200kHz except the 1600kHz. Mode can be selected between Forced Continous Conduction Mode (FCCM) and Diode Emulation Mode (DEM).

**Table 8 TDA38740/725 Boot Up Voltage and OVP Limits Table for VOUT_SCALE_LOOP 1:1.**

| VBT (kΩ) | BOOT-Up Voltage (V) | Relative OVP/UVP (mV) | Fixed OVP (V) |
|---|---|---|---|
| FLOAT | 2.5 | 300 | 2.85 |
| 150 | 1.8 | 300 | 2.2 |
| 127 | 1.65 | 300 | 2.2 |
| 105 | 1.5 | 300 | 2.2 |
| 88.7 | 1.35 | 250 | 1.8 |
| 75 | 1.25 | 250 | 1.8 |
| 61.9 | 1.2 | 200 | 1.5 |
| 51.1 | 1.1 | 200 | 1.35 |
| 43.2 | 1.05 | 200 | 1.35 |
| 36.5 | 1 | 200 | 1.35 |
| 30.1 | 0.90 | 200 | 1.2 |
| 21 | 0.8 | 200 | 1.2 |
| 14 | 0.7 | 150 | 1.2 |
| 9.53 | 0.6 | 150 | 1 |
| 5.62 | 0.5 | 150 | 1 |
| SHORT | 0.4 | 150 | 0.8 |

**Table 9 TDA38740/725 Boot Up Voltage and OVP Limits Table for VOUT_SCALE_LOOP 1:2**

| VBT (kΩ) | BOOT-Up Voltage (V) | Relative OVP/UVP (mV) | Fixed OVP (V) |
|---|---|---|---|
| FLOAT | 5.0 | 300 | 5.7 |
| 150 | 3.6 | 300 | 4.4 |
| 127 | 3.3 | 300 | 4.4 |
| 105 | 3.0 | 300 | 3.6 |
| 88.7 | 2.7 | 300 | 3.6 |
| 75 | 2.5 | 300 | 3.0 |
| 61.9 | 2.4 | 300 | 3.0 |
| 51.1 | 2.2 | 300 | 2.7 |
| 43.2 | 2.1 | 300 | 2.7 |
| 36.5 | 2.0 | 300 | 2.7 |
| 30.1 | 1.8 | 300 | 2.4 |
| 21 | 1.6 | 300 | 2.4 |
| 14 | 1.4 | 300 | 2.0 |
| 9.53 | 1.2 | 200 | 1.6 |
| 5.62 | 1.0 | 200 | 1.6 |
| SHORT | 0.8 | 200 | 1.6 |

When operating in the pin strap resistor mode, the output voltage can be selected by connecting a resistor from the VBT pin to GND per the table above.

When setting the output voltage using VOUT_COMMAND, the VOUT_SCALE_LOOP 1:1 should be used for obtaining outputs in the range of 0.25 V to 2.56 V. For obtaining output voltages between 2.56 V to 5.12 V, the VOUT_SCALE_LOOP 1:2 should be used. When operating in VOUT_SCALE_LOOP 1:1 mode the full output voltage should be fed back to the VOSENP pin as shown in Figure 3. When operating in VOUT_SCALE_LOOP 1:2, half of the

output voltage is fed back to the VOSENP Pin by using a resistor divider as shown in Figure 4. The VBT pin can be used to set the output voltages in the range of 0.4 V to 2.5 V in VOUT_SCALE_LOOP 1:1 and from 0.8 V to 5 V in VOUT_SCALE_LOOP 1:2.

**Table 10 TDA38740 OCP and Internal Phase margin Zero selection**

| $R_{ILIM}$(kΩ) | Typical OCP(A) | Internal Loop-Compensation-Filter-Zero Register |
|---|---|---|
| SHORT | 15 | 0 |
| 3.32 | 60 | 4 |
| 6.98 | 20 | 2 |
| 11 | 10 | 0 |
| 15.4 | 15 | 1 |
| 20.8 | 20 | 1 |
| 26.1 | 25 | 2 |
| 31.6 | 30 | 2 |
| 43.2 | 40 | 3 |
| 51.1 | 50 | 4 |
| 64.9 | 25 | 1 |
| 78.7 | 60 | 3 |
| 95.3 | 40 | 2 |
| 113 | 50 | 3 |
| 133 | 10 | 1 |
| FLOAT | 30 | 3 |

**Table 11 TDA38725 OCP and Internal Phase margin Zero selection**

| $R_{ILIM}$(kΩ) | Typical OCP(A) | Internal Loop-Compensation-Filter-Zero Register |
|---|---|---|
| SHORT | 15 | 0 |
| 3.32 | 15 | 4 |
| 6.98 | 20 | 2 |
| 11 | 10 | 0 |
| 15.4 | 15 | 1 |
| 20.8 | 20 | 1 |
| 26.1 | 30 | 2 |
| 31.6 | 10 | 2 |
| 43.2 | 15 | 3 |
| 51.1 | 20 | 4 |
| 64.9 | 30 | 1 |
| 78.7 | 10 | 3 |
| 95.3 | 15 | 2 |

| $R_{ILIM}$(kΩ) | Typical OCP(A) | Internal Loop-Compensation-Filter-Zero Register |
|---|---|---|
| 113 | 20 | 3 |
| 133 | 10 | 1 |
| FLOAT | 30 | 3 |

When operating in the pin strap resistor mode, the OCP limit can be selected by connecting a resistor from the ILIM pin to GND per the table above. The Internal Loop-compensation-filter zero can also be set by configuration register 0x64[14:12] through PMBus.

**Table 11 SM_ADDR/PROG Pin**

| Resistor to GND (kΩ) | PROG pin | SM_ADDR pin : Offset from the base Address |
|---|---|---|
| SHORT | CONFIG0 | 0 |
| 5.62 | CONFIG1 | 1 |
| 9.53 | CONFIG2 | 2 |
| 14 | CONFIG3 | 3 |
| 21 | CONFIG4 | 4 |
| 30.1 | CONFIG5 | 5 |
| 36.5 | CONFIG6 | 6 |
| 43.2 | CONFIG7 | 7 |
| 51.1 | CONFIG8 | 8 |
| 61.9 | CONFIG9 | 9 |
| 75 | CONFIG10 | 10 |
| 88.7 | CONFIG11 | 11 |
| 105 | CONFIG12 | 12 |
| 127 | CONFIG13 | 13 |
| 150 | CONFIG14 | 14 |
| FLOAT | CONFIG15 | 15 |

When operating in the pin strap resistor mode for the SM_ADDR/PROG pin, the address and the configuration file can be selected by connecting a resistor from the SM_ADDR/PROG pin to GND per the table above.

# 9 Typical Efficiency and Power Loss Curves

## 9.1 $PV_{in} = V_{in} = 12$ V, Vout = 1.2V, $F_{sw} = 600$kHz

The test for efficiency was done at 0 LFM and the driver losses are included in the efficiency numbers. Solid lines indicate efficiency and dashed lines show power loss at 600 kHz.

**Table 12 Inductors for $PV_{in}=V_{in}=12$ V, $F_s = 600$ kHz**

| Vout (V) | Lout (nH) | P/N | DCR (mΩ) | Size (mm) |
|---|---|---|---|---|
| 1.2 | 150 | L101247A-100L | 0.125 | 10 x 6.4 x 12 |
| 3.3 | 470 | L101158A-R47MHF | 0.81 | 10 x 7 x 10 |

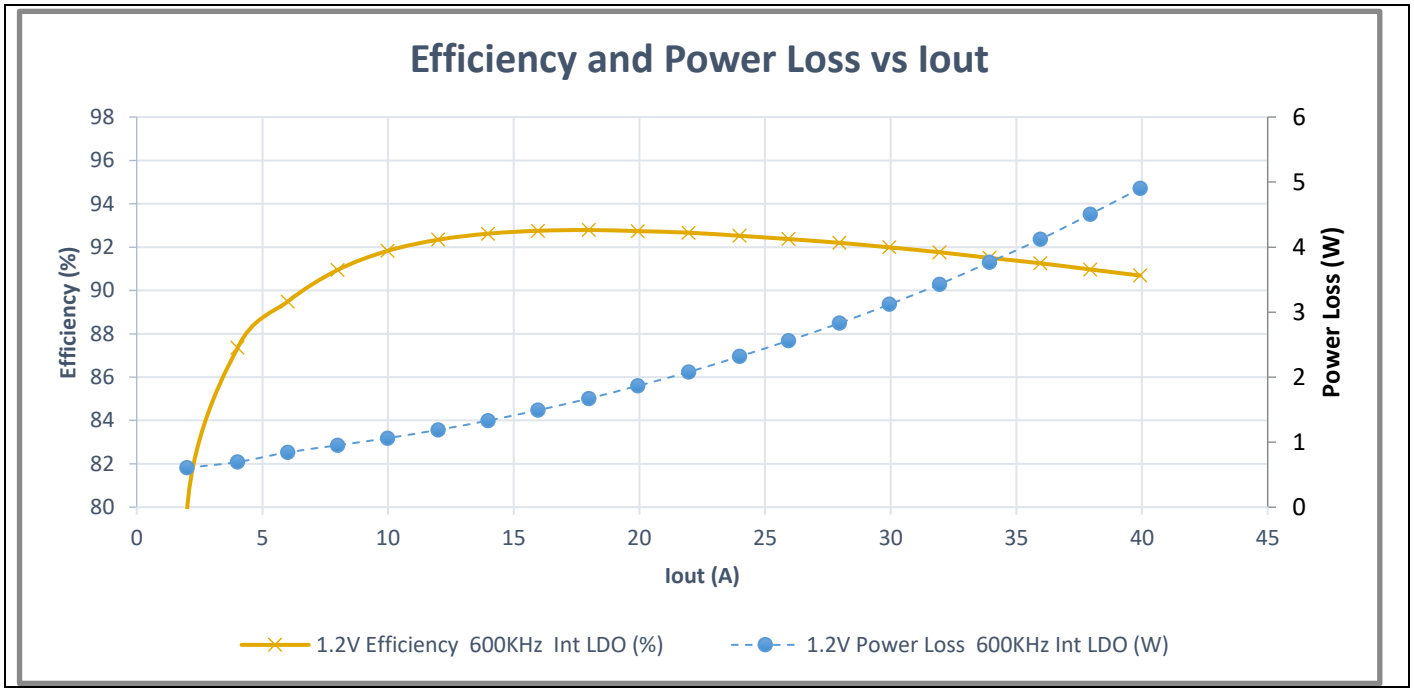



**Figure 5 Typical efficiency and power loss curves, $PV_{in} = V_{in} = 12$ V, Vout = 1.2 V, $F_{sw} = 600$ kHz**

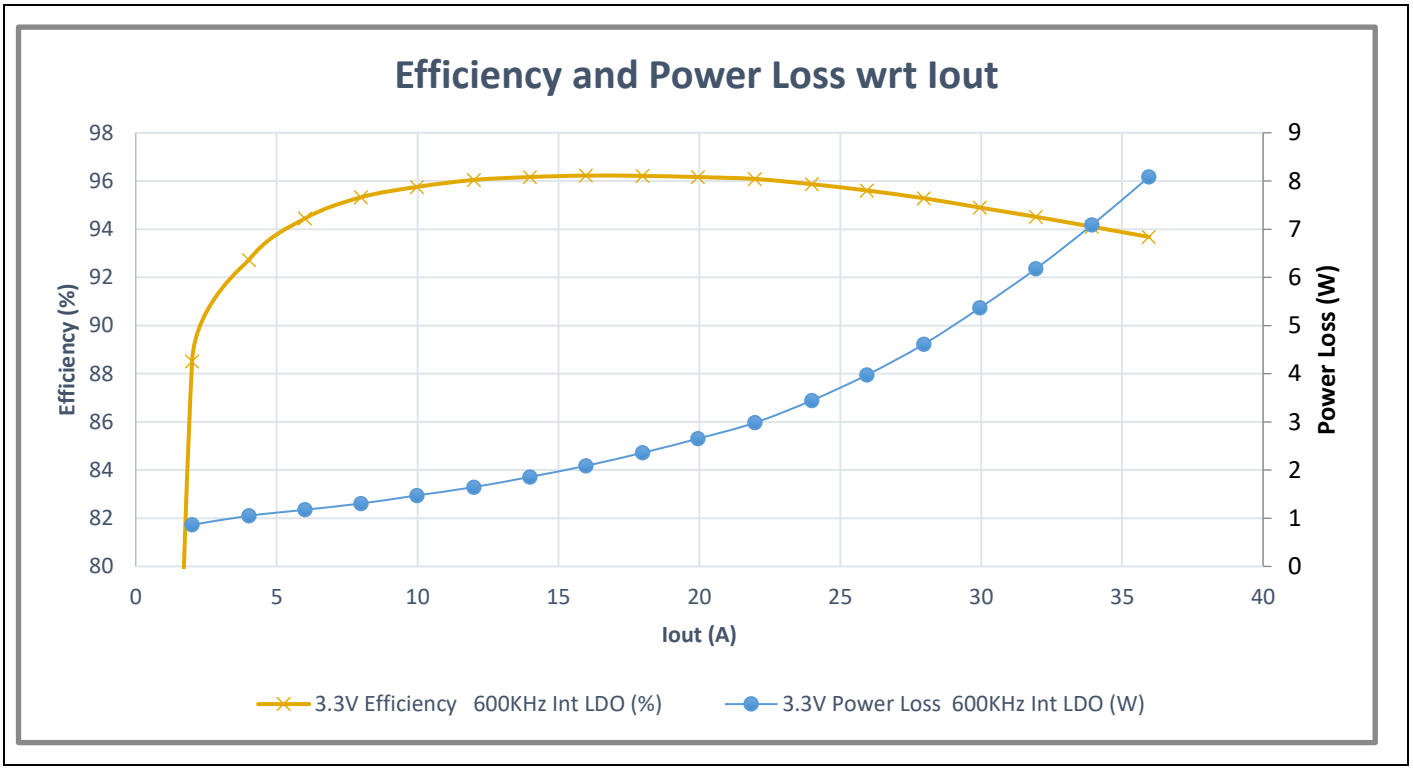



**Figure 6 Typical efficiency and power loss curves, $PV_{in}$ = $V_{in}$ = 12 V, Vout = 3.3 V, $F_{sw}$ = 600 kHz**

## 9.2 $PV_{in}$ = $V_{in}$ = 12 V, $F_{sw}$ = 800 kHz

The test for efficiency was done at 0 LFM and the driver losses are included in the efficiency numbers. Solid line indicate Efficiency and dashed lines are showing power loss at 800 kHz.

**Table 13 Inductors for $PV_{in}$=$V_{in}$=12 V, $F_{sw}$ = 800 kHz**

| Vout (V) | Lout (nH) | P/N | DCR (mΩ) | Size (mm) |
|---|---|---|---|---|
| 1.2 | 150 | L101247A-150L | 0.125 | 10 x 6.4 x 12 |
| 3.3 | 470 | L101158A-R47MHF | 0.81 | 10 x 7 x 10 |


**Figure 7 Typical efficiency and power loss curves, $PV_{in}$ = $V_{in}$ = 12 V, Vout = 1.2 V, $F_{sw}$ = 800 kHz**

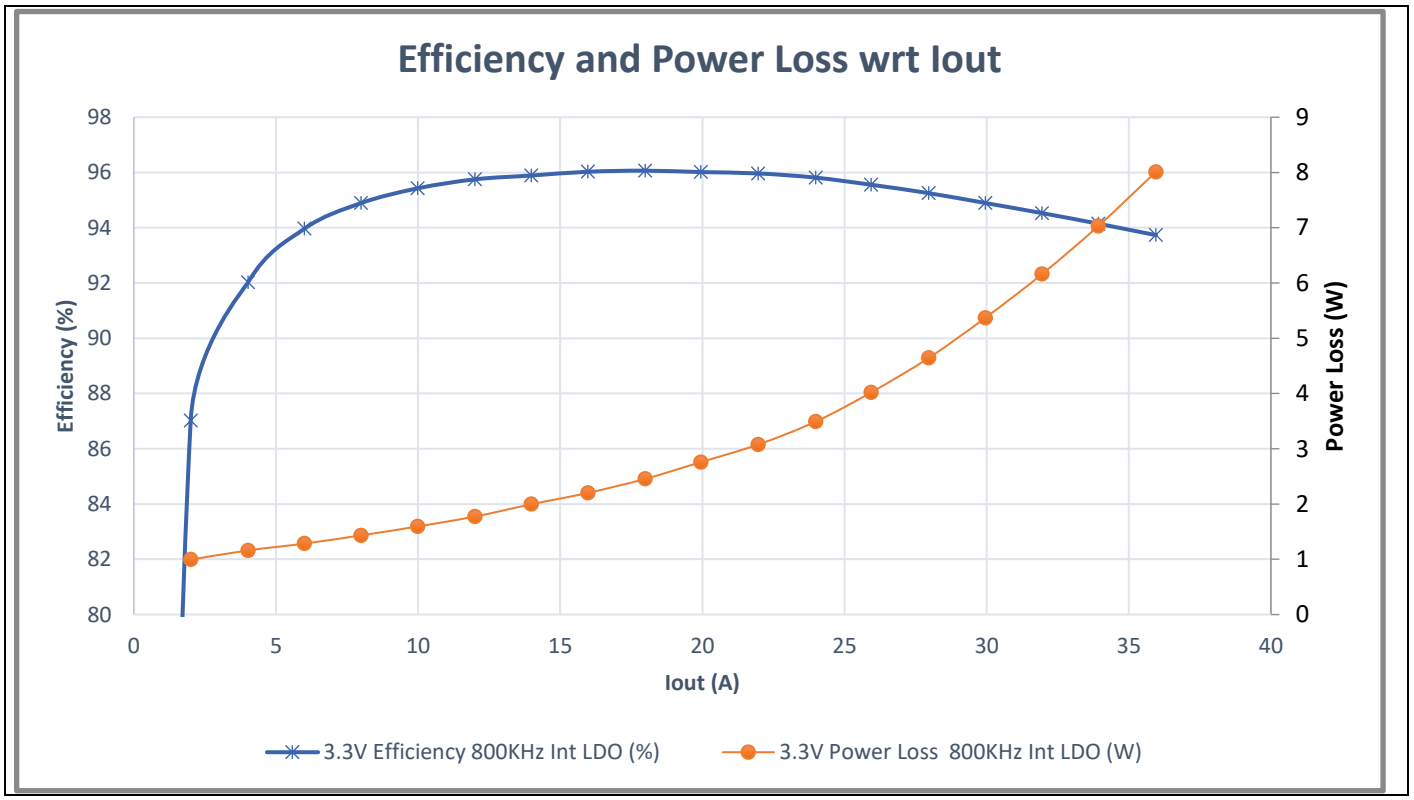



**Figure 8 Typical efficiency and power loss curves, $PV_{in}$ = $V_{in}$ = 12 V, Vout = 3.3 V, $F_{sw}$ = 800 kHz**

## 9.3 $PV_{in}$ = $V_{in}$ = 12 V, $F_{sw}$ = 1000 kHz

The test for efficiency was done at 0 LFM and the driver losses are included in the efficiency numbers. Solid lines indicate efficiency and dashed lines show power loss at 1000 kHz.

**Table 14 Inductors for $PV_{in}$=$V_{in}$=12 V, $F_{sw}$ = 1000 kHz**

| Vout (V) | Lout (nH) | P/N | DCR (mΩ) | Size (mm) |
|---|---|---|---|---|
| 1.2 | 150 | L101247A-150L | 0.125 | 10 x 6.4 x 12 |
| 3.3 | 470 | L101158A-R47MHF | 0.81 | 10 x 7 x 10 |

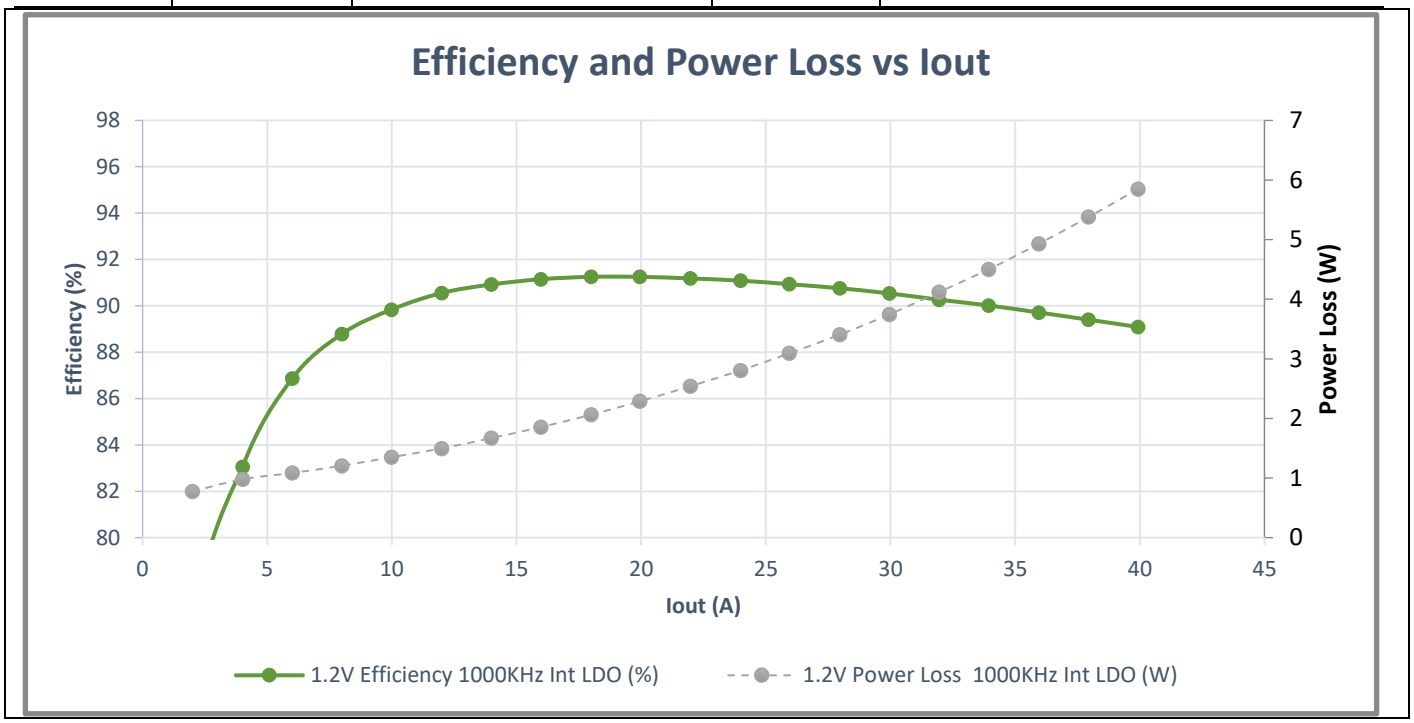



**Figure 9 Typical efficiency and power loss curves, $PV_{in}$ = $V_{in}$ = 12 V, Vout =1.2 V, $F_{sw}$ = 1000 kHz**

## Typical Efficiency and Power Loss Curves

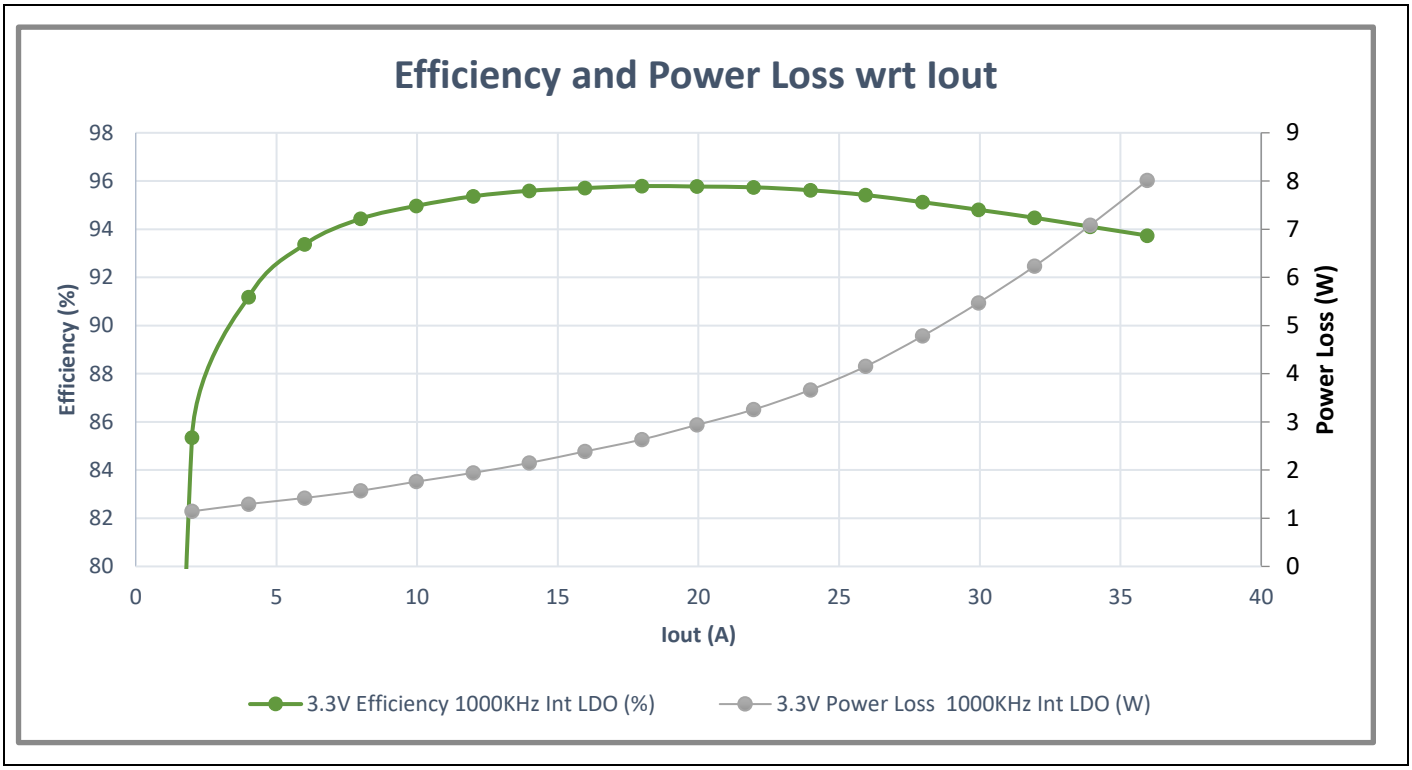



**Figure 10 Typical efficiency and power loss curves, $PV_{in}$ = $V_{in}$ = 12 V, Vout =3.3 V, $F_{sw}$ = 1000 kHz**

# 10 Thermal De-rating curves

Measurement is done on Evaluation board DB356. The PCB is an 8-layer board with 2 oz Copper for top and bottom layers and 2 oz Copper for the inner layers, FR4 material, size 5.25”x4.1”.

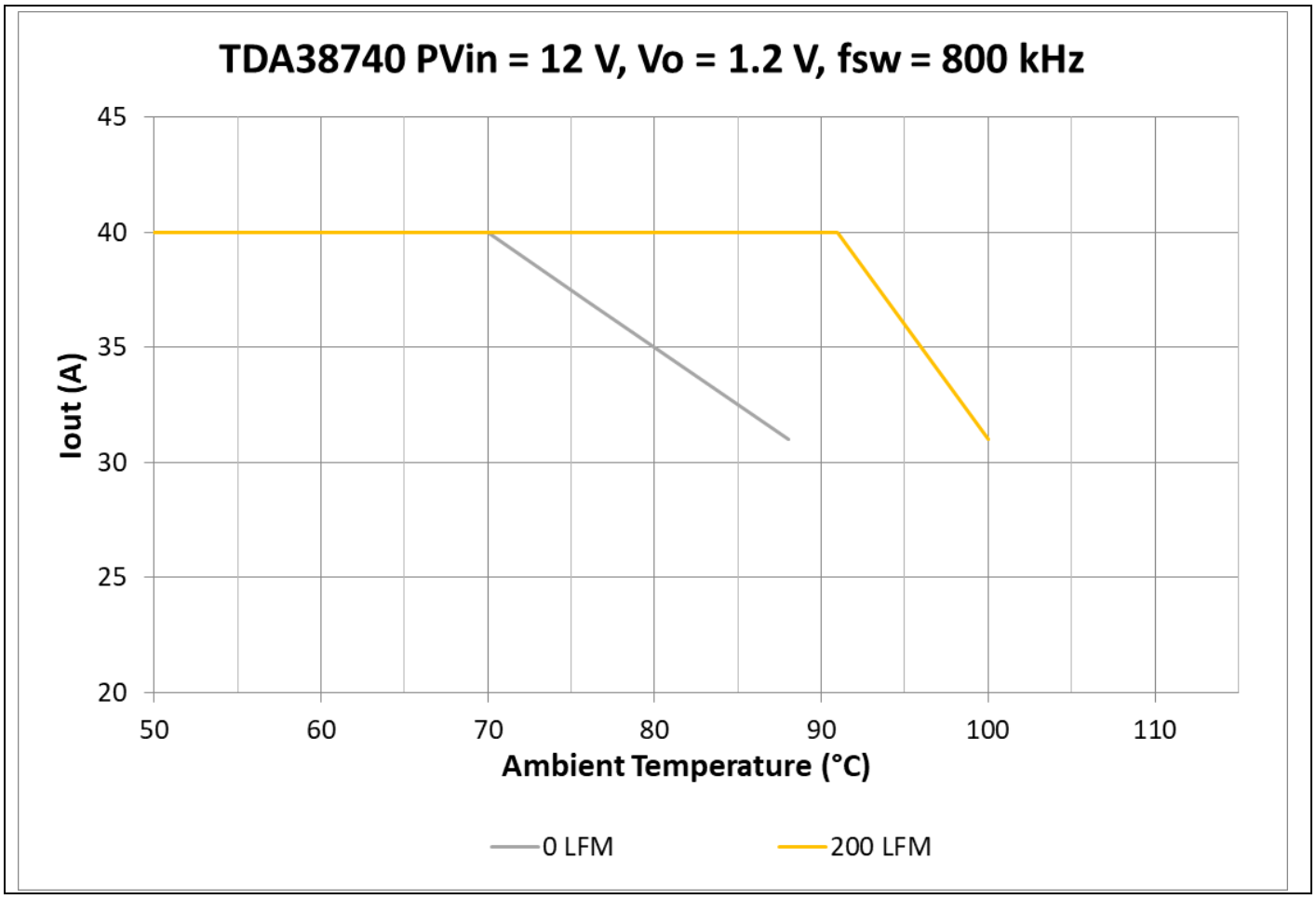



**Figure 11 Thermal de-rating curves, $PV_{in}$ = 12 V, Vout = 1.2 V, $f_{sw}$ = 800 kHz, VCC = Internal LDO**

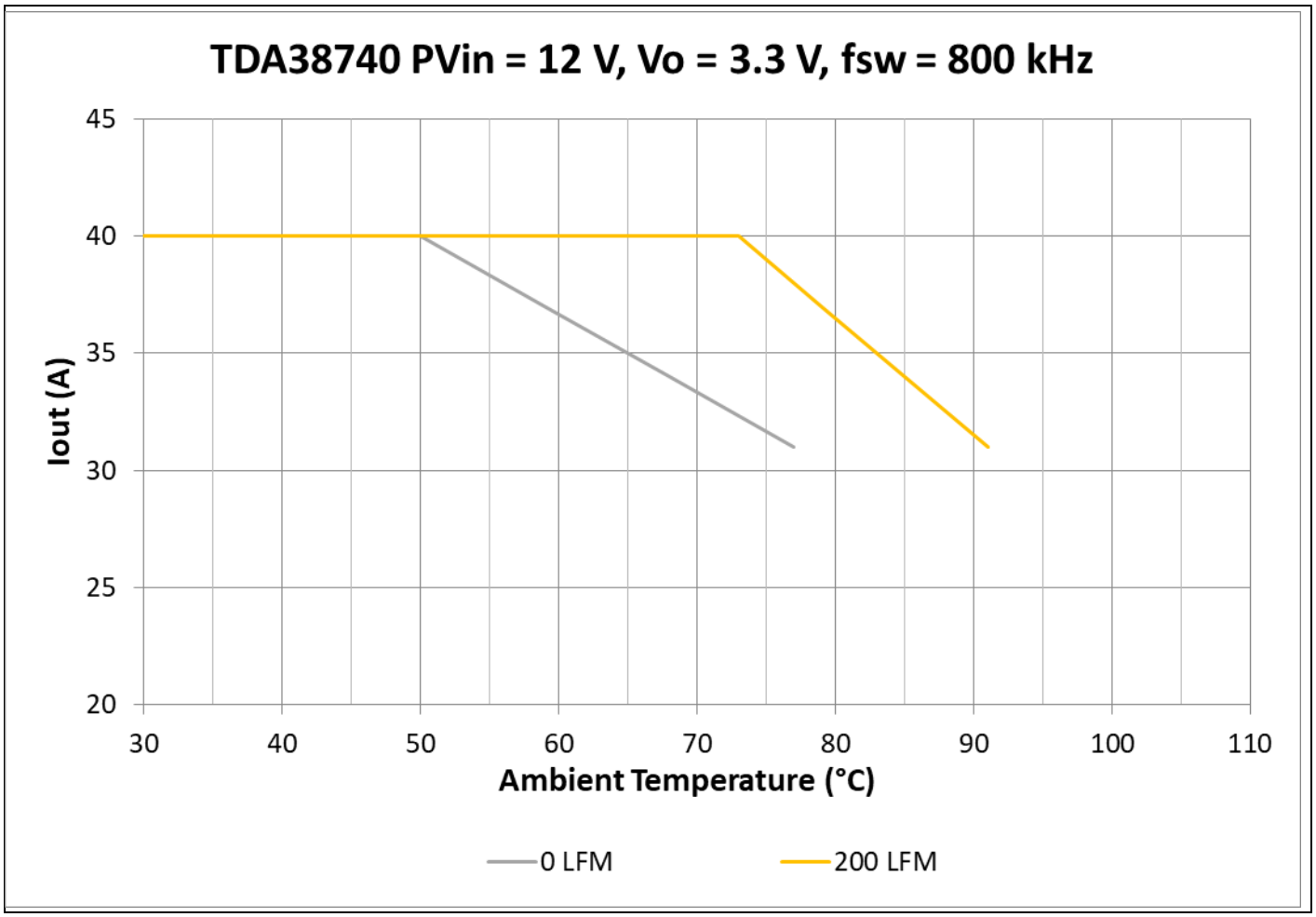



**Figure 12 Thermal de-rating curves, $PV_{in}$ = 12 V, Vout = 3.3 V, $f_{sw}$ = 800 kHz, VCC = Internal LDO**

# 11 $R_{DS(on)}$ of MOSFET Over Temperature

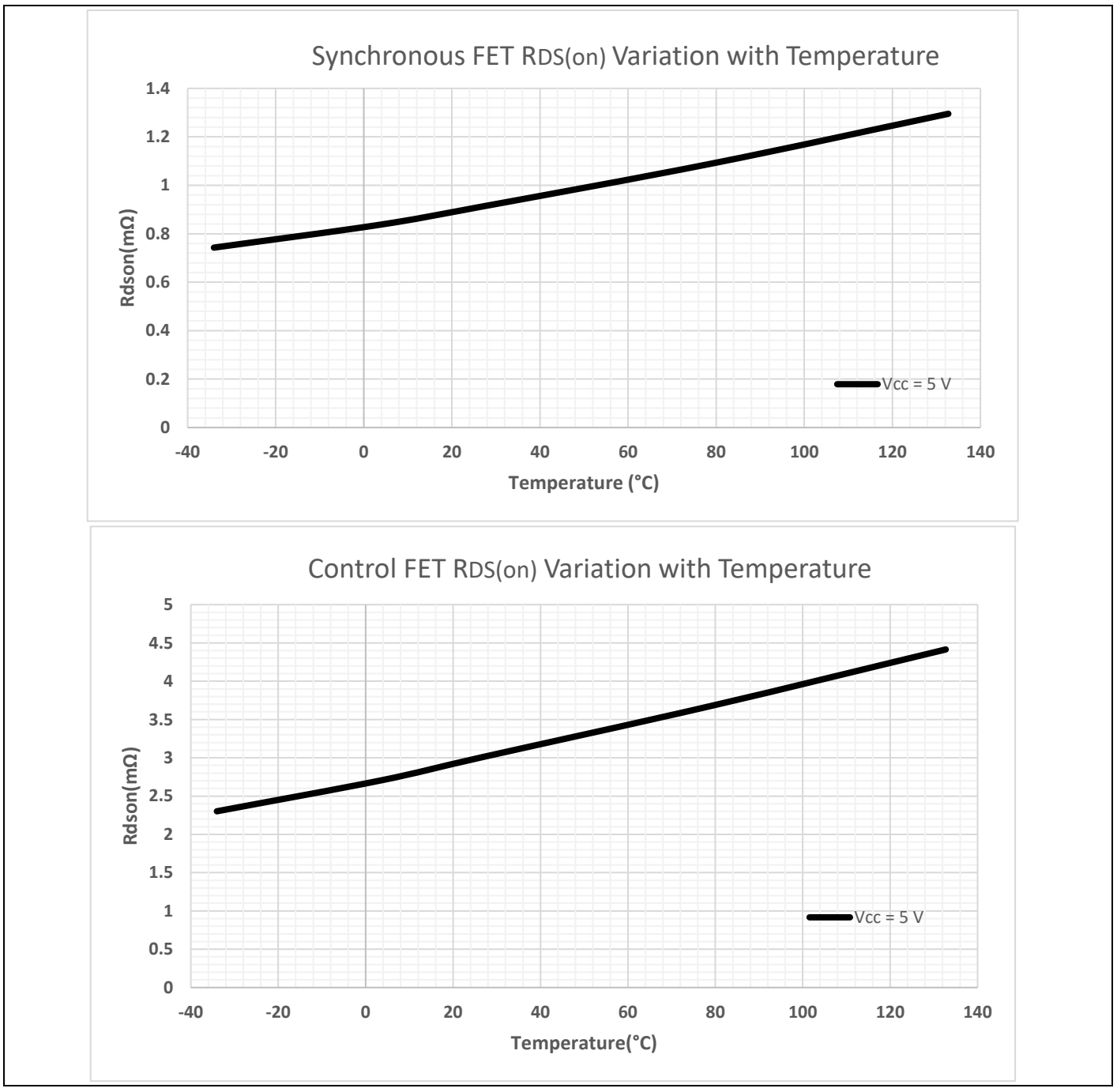



**Figure 13 RDS(on) of MOSFETs over Junction Temperature**

# 12 Typical operating characteristics (-40 °C ≤ $T_j$ ≤ +125 °C)

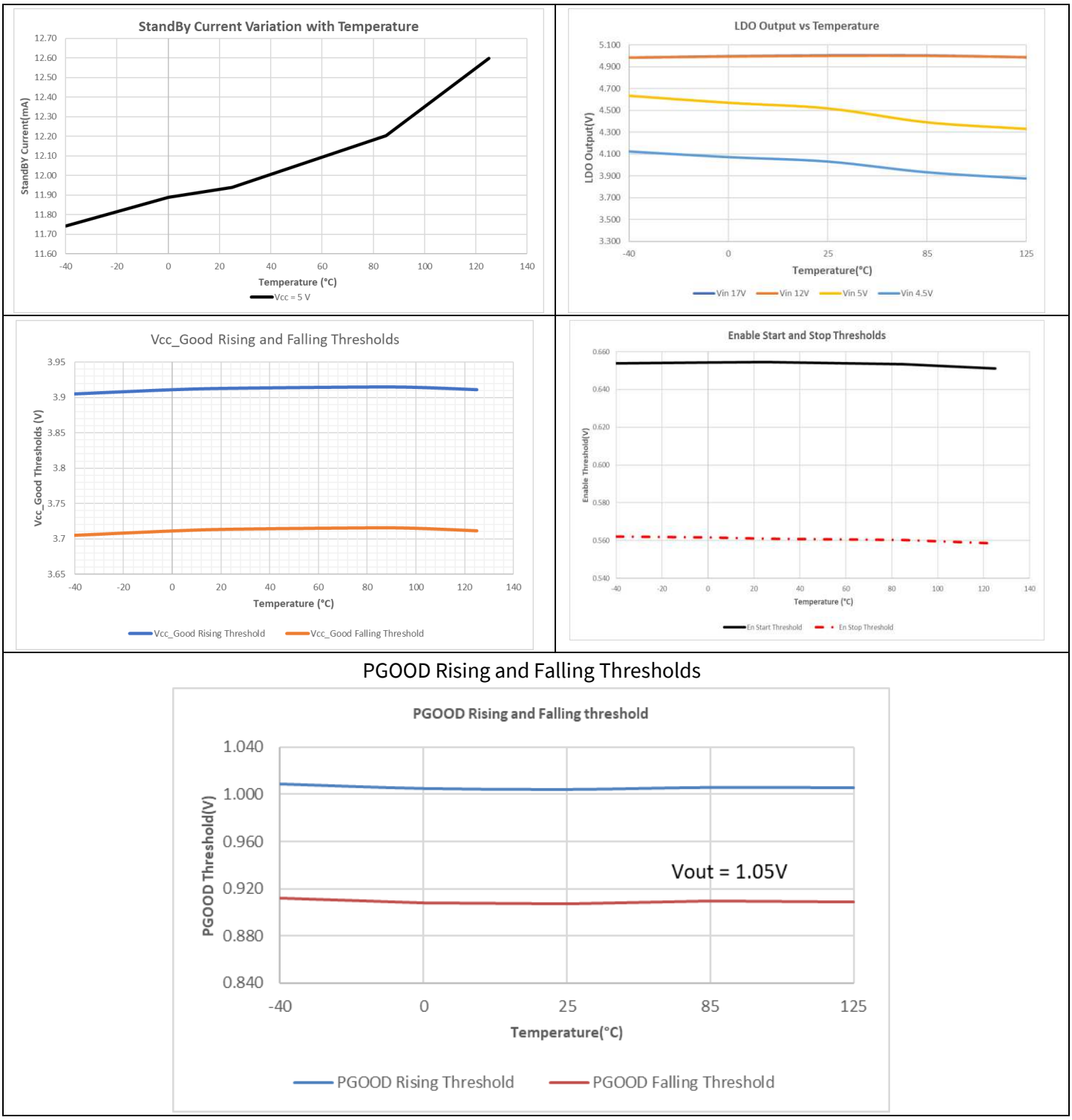
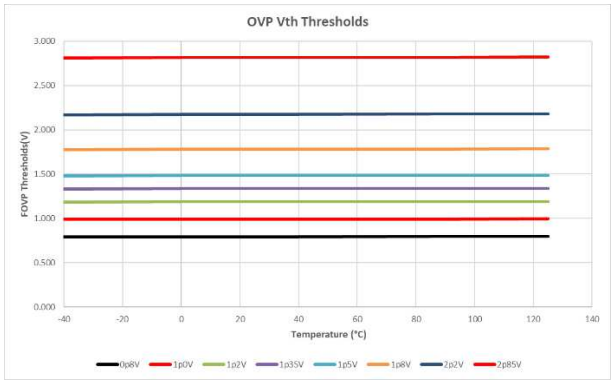


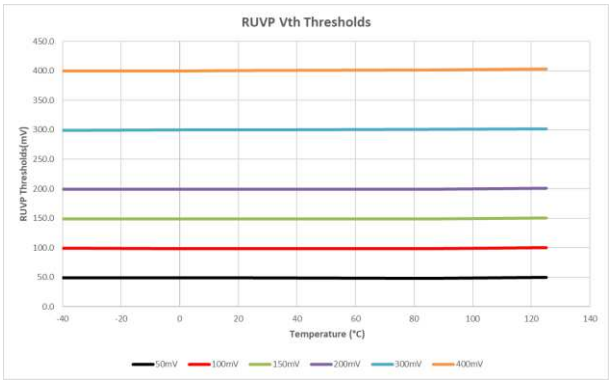

**Figure 14 Typical operating characteristics (set 1 of 2)**

## Typical operating characteristics (-40 C ≤ Tj ≤ +125 C)

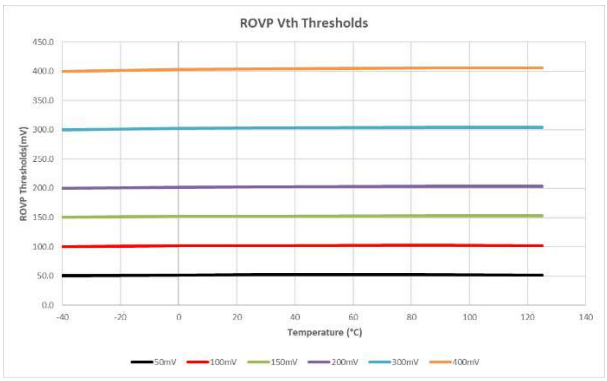
FOVP Thresholds




RUVP Thresholds




ROVP Thresholds




Analog OCP Thresholds

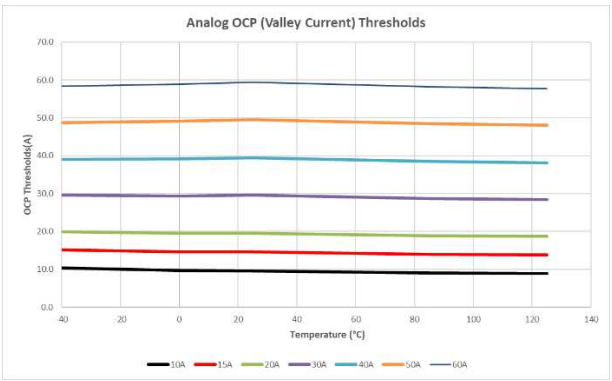



**Figure 15 Typical operating characteristics (set 2 of 2)**

# 13 General Description

The TDA38740/725 is an easy-to-use, fully integrated, and highly efficient dc-dc regulator optimized to convert a 12 V input supply to a voltage level required by high performance microprocessors, DDR memory, housekeeping supplies, base stations, etc. The onboard PWM controller and OptiMOS™ FETs with integrated bootstrap diode make TDA38740/725 a small footprint solution, providing highly efficient power delivery. Using a fast Constant On-Time (COT) control scheme simplifies design efforts and achieves fast control response. The device configuration can be easily defined using Infineon's XDP Designer GUI and is stored in the on-chip memory.

## 13.1 PMBUS Operating Mode

The TDA38740/725 can be used in PMBUS mode. In PMBUS mode, the output voltage is controlled by the PMBUS VOUT_COMMAND command. The VOUT_MODE resolution can be set to 0.244 mV/lsb, 0.488 mV/lsb, 0.977 mV/lsb, 1.953 mV/lsb, or 3.906 mV/lsb. The output voltage resolution can only be set to a minimum of 0.625 mV/lsb. The resolution is user-programmable via a configuration file.

See Table 17 for a full list of all supported PMBUS commands. Please refer to App Note AN_2203_PL12_2204_184108 for more details.

## 13.2 Multiple Time Programming Memory (MTP)

The MTP stores the device configuration. At power-up, MTP contents are transferred to operating registers for access during device operation. MTP allows customization during both design and high-volume manufacturing. MTP integrity is verified by Cyclic Redundancy Check (CRC) validation on each power up. The controller will not start up in the event of a CRC error.

The TDA38740/725 offers up to 24 writes to configure basic device parameters such as frequency, fault operation characteristics, and boot voltage. This represents a significant size and component saving compared to traditional analog methods. In addition to this, the TDA38740/725 also allows loading of multiple (up to 16) configuration files and automatic selection of a unique file after power-up based on the resistor value at the SM-ADDR/PROG pin.

## 13.3 Voltage Sense

An error voltage is generated from the difference between the target voltage, defined by the output voltage and load line (if implemented), and the differentially sensed output voltage (remote sense). The error voltage is digitized by a high-speed, high-precision ADC. An anti-alias filter provides the necessary high frequency noise rejection. The gain and offset of the voltage sense circuitry for each loop is factory trimmed to deliver the required accuracy.

In order to achieve tight regulation in vout_scale_loop of 1:2 where a resistor divider is used to feedback the output voltage, connect a 31 kΩ resistor R3 in parallel to the top resistor R1 of the divider as shown in Figure 4. This will compensate for the error caused by impedance of the Analog front end (AFE) circuit. The recommended value for R1 and R2 is 499 Ohms and the recommended tolerance for R1, R2 and R3 is 1%.

## 13.4 PMBus Interface

A PMBus interface is used to communicate with the TDA38740/725. This two-wire serial interface consists of clock and data signals, and operates as fast as 1 MHz. The bus provides read & write access to the internal registers for configuration, and for monitoring of operating parameters. The bus is also used to program on-chip non-volatile memory (MTP) to store operating parameters.

To ensure operation with multiple devices on the bus, a base address for TDA38740/25 is programmed into the MTP. The unique slave address for the device is a combination of the base address in the device register plus the offset generated by the SM_ARR/PROG pin (depending on the resistor value connected to the pin).

To protect customer configuration and information, the PMBus interface can be configured for either limited access or locked with a 16-bit software password. Limited access includes both write and read protection options. In addition, there is a telemetry-only mode which only allows reads from the telemetry registers.

Refer to the PMBus Command Codes in Table 17 for more information. Through the PMBus, it is possible to access configuration registers and the PMBus registers in the device. It has a 7-bit register to set the base PMBus address 0x40[6:0] of the device. Please refer to the App note AN_2204_PL12_2204_183614 for more information on the register map.

## 13.5 Infineon XDP Designer GUI

The Infineon XDP Designer GUI provides the designer with a comprehensive design environment that includes input settings, output settings, telemetry and PMBus interface. With these tools, a designer can monitor and set system configuration settings for fault thresholds and output behavior in real time. The XDP Designer GUI allows real-time design monitoring of key parameters such as output current and power, input current and power, efficiency, temperature, and faults. Figure 16 shows the GUI home screen with the available parameter windows.

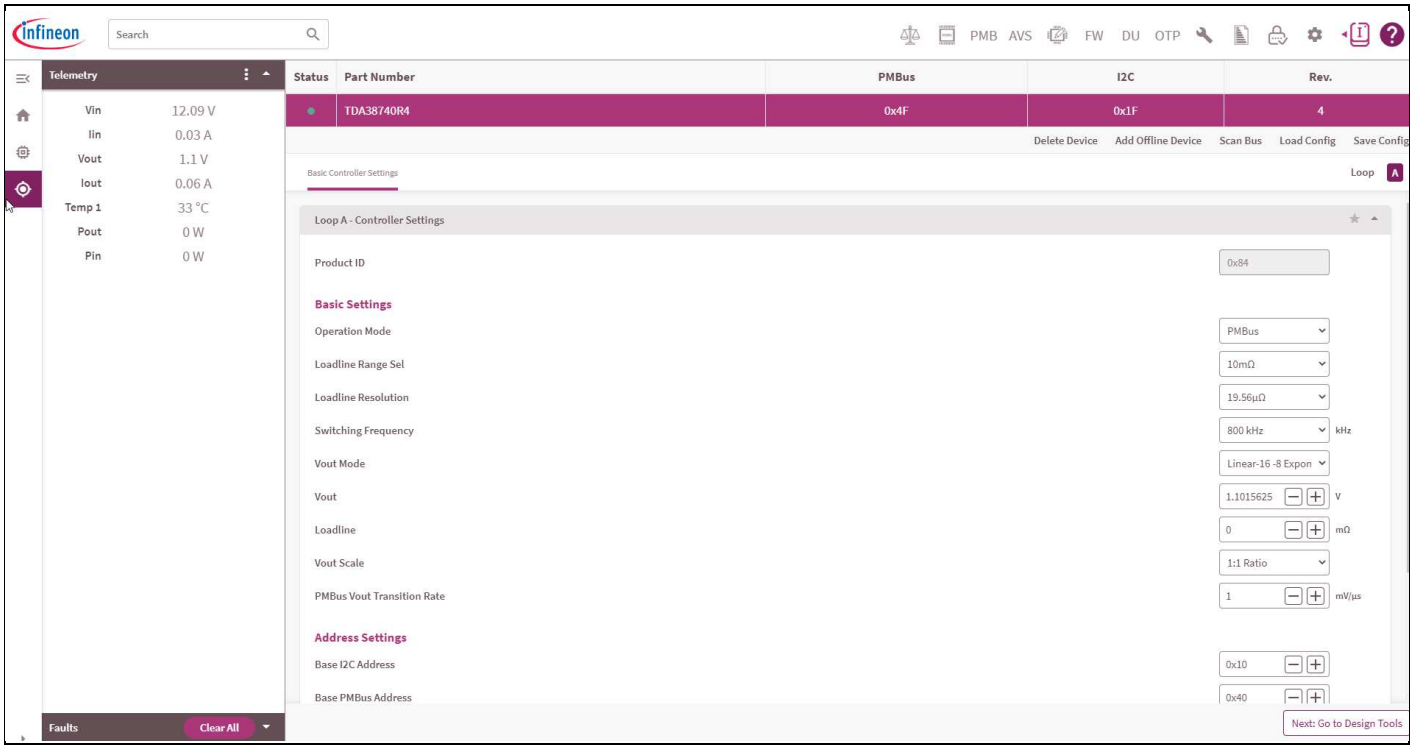



**Figure 16 XDP Designer GUI home screen.**

## 13.6 Programming

Once a design is complete, the XDP Designer GUI produces a complete configuration file. These configurations files can be saved and loaded.

## 13.7 Real-time Monitoring

The TDA38740/725 can be accessed through the use of PMBus Command codes (described in Table 17) to read the real-time status of the power supply (dc-dc converter) including input and output voltages, input and output currents, input and output power and temperature.

# 14 Theory of Operation

## 14.1 Device Power-On and Initialization

TDA38740/725 is ready to communicate as soon as Vcc is above the threshold of 3.7 V. The device starts switching once the Enable signal is pulled high. Based on whether Vcc is supplied externally or an internal LDO is used, the recommended power-up sequences are shown in Figure 17.

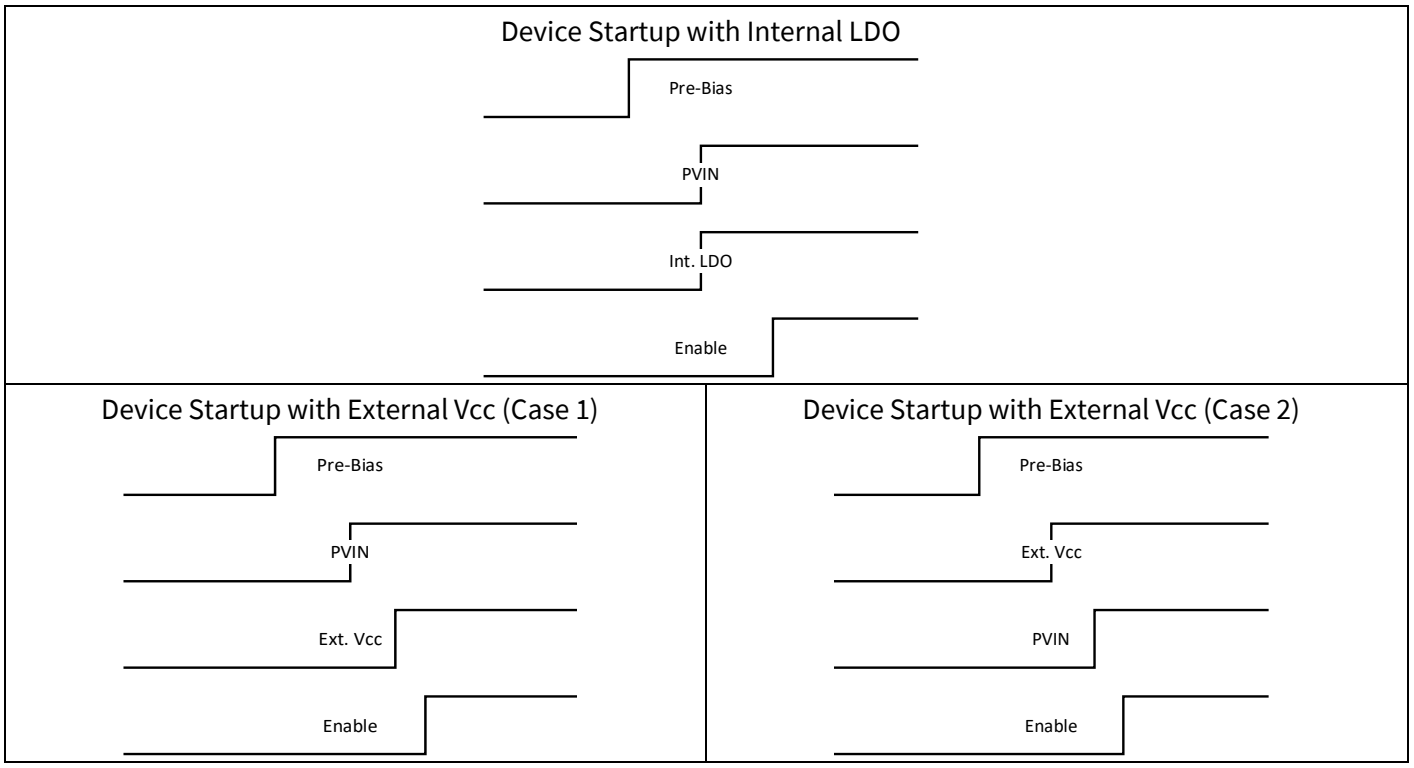



**Figure 17 Device power-on sequence.**

## 14.2 Pre-bias start-up

The TDA38740/725 is able to start up into a pre-charged output without causing oscillations and disturbances of the output voltage. When TDA38740/725 starts up with a pre-biased output voltage, both control FET and Sync FET are kept off until the internal soft-start signal exceeds the FB voltage. The sequencing recommendation with pre-bias is shown in Figure 17.

When turned on into a prebiased output voltage, the device can trigger a HSS fault and/or ROVP fault. In order to avoid the false triggering of these faults, the following conditions should be met:

- The Startup sequence should follow the sequencing shown in Figure 17
- The PVIN voltage slew rate should be greater than 10 V/ms
- The VBT pin should be connected to a high impedance (>1 MΩ) or left floating
- The “power down analog circuit when the output is not enabled” feature should be disabled (set register 0x6C value to 0xF240)

## 14.3 Internal Low-Dropout (LDO) Regulator

The TDA38740/725 has an integrated low-dropout LDO regulator to provide the bias voltage for internal circuitry. VIN pin is the input for the LDO. When the VCC voltage rises above the VCC_UVLO_Start threshold and the EN voltage is above the Enable_UVLO_Start threshold, the soft-start sequence starts. When using the internal LDO for single rail operation, the VIN pin should be connected to the PVIN pin. To save power losses on the LDO, an external bias voltage can be used by connecting the VIN pin to the VCC/LDO pin. Figure 18 illustrates the possible configurations of VCC/LDO and VIN pins.

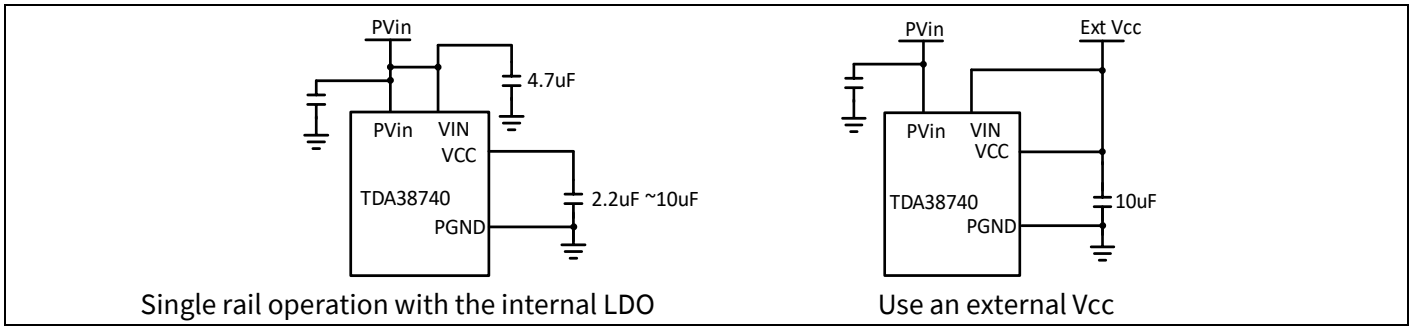



**Figure 18 Configuration of using the internal LDO or an external VCC.**

## 14.4 Fast Constant ON-Time Control

The TDA38740/725 features a proprietary Fast Constant On-Time (COT) Control, which can provide fast load transient response, good output regulation and minimize design effort. Fast COT control compares the output voltage, $V_o$, to a floor voltage combined with an internal ramp signal. When Vout drops below that signal, a PWM signal is initiated to turn on the high-side FET for a fixed on-time. The floor voltage is generated from an internal compensated error amplifier, which compares Vout with a reference voltage. Compared to traditional COT control, Fast COT control significantly improves Vout regulation.

## 14.5 EN (Enable) Pin

The EN pin controls the on/off state of the TDA38740/725. When the VCC/LDO voltage rises above the VCC_UVLO_Start threshold, the soft-start sequence starts. The EN pin voltage needs to be toggled when the VCC voltage drops below VCC_UVLO_Stop and rises above the VCC_UVLO_Start threshold to start the soft-start sequence.

The EN pin can be configured in four ways. Three of them are as shown in Figure 19. Configuration one is an external logic signal. The second and third possible configurations derive the enable signal from the PVin voltage by a resistive divider, $R_{EN1}$ and $R_{EN2}$ or tie EN to Pvin. The fourth configuration is control via PMBus register 0x204[7:0] using the PMBus lines. TDA38740/725 utilizes the PMBus ON_OFF_CONFIG command in combination with the OPERATION command, register 0x202[7:0], to control the soft enable. Using this, a preference between hardware or software enable may be established. More information is available in the PMBUs app note AN_2203_PL12_2204_184108.

The EN pin should not be left floating. There is an internal pull down resistor of 1MΩ from EN to GND pin. A pull-down resistor in the range of tens of kilohms is recommended.

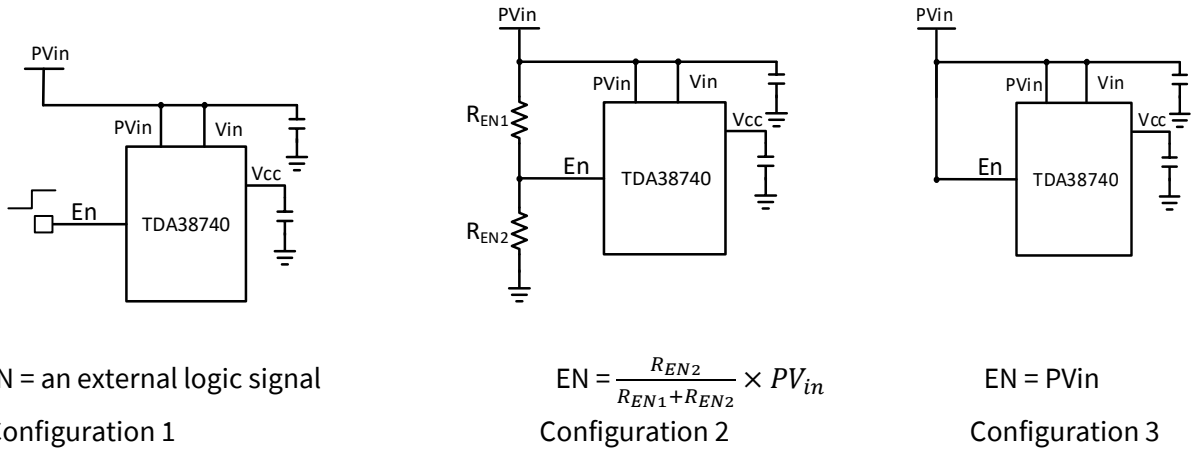



**Figure 19 Enable Configurations**

## 14.6 Switching Frequency and FCCM/DEM Operation

The TDA38740/725 offers two operation modes: Forced Continuous Conduction (FCCM) and Diode Emulation Mode (DEM). With FCCM, the TDA38740/725 always operates as a synchronous buck converter with a pseudo constant switching frequency and therefore achieves small output voltage ripple. In DEM, the synchronous FET is turned off when the inductor current is close to zero, which reduces the switching frequency and improves efficiency at light load. At heavy load, both FCCM and DEM operate in the same way. The operation mode can be selected by bit 0x5C [1] in the configuration register, value 1 for this bit programs the device to operate in FCCM mode and 0 for DEM. It should be noted that the selection of the operation mode cannot be changed on the fly. To load a new configuration, EN or VCC voltage must be cycled.

The TDA38740/725 offers eight programmable switching frequencies, $f_{sw}$, from 400 kHz to 2 MHz excluding 1600 kHz, by editing the PMBus register, 0x266[15:0], using the PMBus lines. Based on the selected $f_{sw}$, the TDA38740/725 generates the corresponding on-time of the Control FET for a given $PV_{in}$ and $V_o$, as shown by the formula below.

$$T_{on} = \frac{V_0}{PV_{in}} \times \frac{1}{f_{sw}}$$

Where $f_{sw}$ is the desired switching frequency. During operation, the TDA38740/725 monitors $PV_{in}$ and $V_o$, and can automatically adjust the on-time to maintain the pre-selected $f_{sw}$. With the increase of the load, the switching frequency can increase to compensate for the power losses. Therefore, the TDA38740/725 has a pseudo constant switching frequency.

Using the FREQUENCY_SWITCH PMBus command, the switching frequency may be programmed between 400 kHz and 2 MHz in steps of 200 kHz except 1600 kHz.

## 14.7 Soft Start

The soft-start functionality is based on the PMBus TON_RISE command. As shown in the waveform below, when the TON_RISE is set to 50 ms, the output voltage rises from zero to set value in 50 ms.

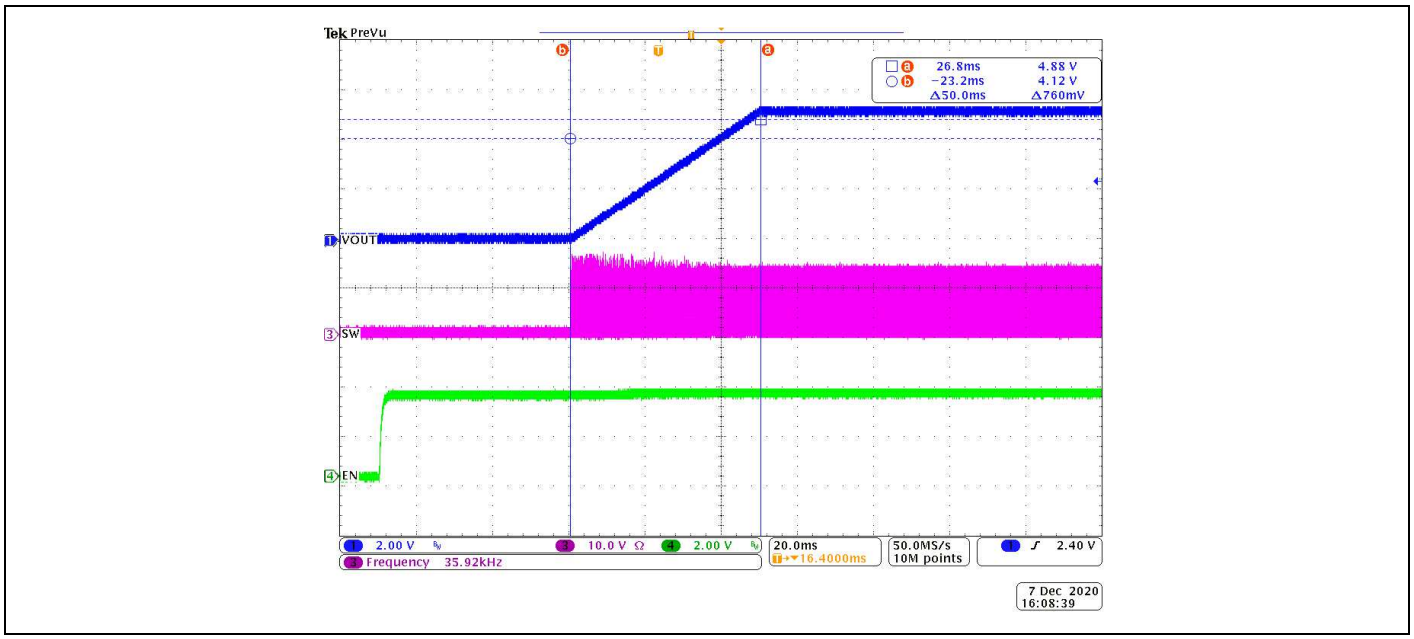



**Figure 20 Vo=5V, Ch1=Vout, Ch3=Switching node, Ch4=Enable Signal**

After the EN pin is enabled, the TON_DELAY command is executed before the TON_RISE command. Hence, the output will not begin to rise until the specified delay is completed. In the above example, the delay is also set to 50 ms.

## 14.8 Load-line

The TDA38740/725 offers a digital load line which can be set via configuration registers, without any need for external components. The load line can be programmed from 0 to 10 mΩ at a resolution of 19.53 µΩ using the VOUT_DROOP command 0x250[15:0]. The range and resolution of the VOUT_DROOP may be increased by using the bit loadline_range_sel 0x6a [6] to 0 to 50 mΩ at a resolution of 100 µΩ. In addition to this, the bandwidth of the digital load line is also programmable from 30 kHz to 500 kHz in steps of 30 kHz by using 4 bits of register 0x6a [3:0].

## 14.9 Output Voltage Differential Sensing

The TDA38740/725 VOSENP and VOSENM pins are connected across the output capacitors near the load to provide true differential remote voltage sensing with high common-mode rejection. Fast COT control compares the output voltage to a floor voltage combined with an internal ramp signal. When Vout drops below that signal, a PWM signal is initiated to turn on the high-side FET for a fixed on-time. The floor voltage is generated from an internal compensated error amplifier, which compares the Vout with a reference voltage. As shown in Figure 21, the output sense pins VOSENP and VOSENM are connected across the output capacitors.

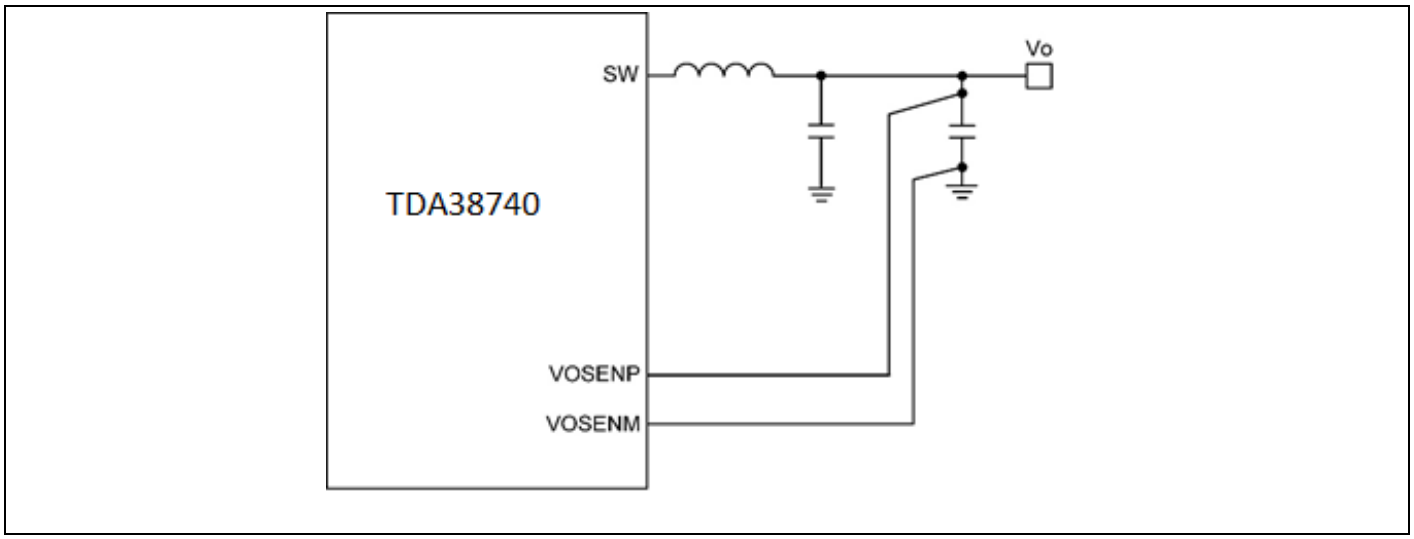



**Figure 21 Output voltage sensing connections**

## 14.10 Output Current Sensing

Current sensing for both telemetry and over current protection is done by sensing the voltage across the sync FET $R_{DS(on)}$. This method increases the converter's efficiency, reduces cost by eliminating a current sense resistor and minimizes any sensitivity to layout related noise issues. A novel scheme allows reconstruction of the inductor current from the voltage sensed across the Sync FET $R_{DS(on)}$.

# 15 Faults and Protections

## 15.1 Over Current Protection (OCP)

The TDA38740/725 has two levels of OCP protection: Analog OCP (AOCP) and Digital OCP (DOCP). The AOCP current limit is based on valley inductor current, whereas the DOCP is based on average current information. AOCP is a fast fault response, and should be set to a value that prevents failure of the device.

A novel scheme allows reconstruction of the inductor current from the voltage sensed across the Sync FET $R_{DS(on)}$. It should be noted here that it is this reconstructed average inductor current that is digitized by the ADC and used for output current reporting.

The over current (OC) fault protection circuit also uses the voltage sensed across the $R_{DS(on)}$ of the Synchronous MOSFET; however, the protection mechanism relies on a fast comparator to compare the sensed signal to the over current threshold and does not depend on the ADC or reported current. The current limit scheme uses an internal temperature compensated current source that has the same temperature coefficient as the $R_{DS(on)}$ of the Synchronous MOSFET. As a result, the over current trip threshold remains almost constant over temperature.

The TDA38740/725 AOCP can be accessed via three bits in the register map (aocp_thresh_sel [0:2]). The digital OCP (DOCP) is availble via the PMBus register IOUT_OC_FAULT_LIMIT, and the response is decided by IOUT_OC_FAULT_RESPONSE. Available responses are shutdown, retry 6 times and latch off, or retry indefinitely. The indication of the fault is available in STATUS_IOUT register in PMBus.

AOCP shall be enabled during soft-start and normal operation including FCCM and DEM modes. When AOCP is crossed, the low side MOSFET will continue to stay on for the remaining cycle and the following high side pulse will be ignored to allow inductor relaxation (pulse skipping). If an AOCP condition is detected on the rising edge of a PWM pulse, the high side will still be blocked from turning on and the pulse will be skipped.

The high side will continue to be ignored if the current remains above the AOCP threshold. A 10-count counter is implemented to count 10 AOCP events, then a signal is sent to the digital block to perform the programmed response when the Digital OCP is triggered from the Analog OCP. The counter is reset after 3 consecutive non-OCP events. The count occurs at the valley of the current. Note that COT switching frequency will decrease when skipping pulses. Figure 22 is an example AOCP response.

The TDA38740/725 also offers cycle-by-cycle AOCP response with a choice of eight selectable current limits, which is set by the resistance at ILIM pin. The selected OCP limit bank is loaded to the IC during the power up and cannot be changed on the fly. To change the OCP limit, users must cycle the EN signal or VCC voltage. Cycle-by-cycle OCP response allows the TDA38740/725 to fulfill a brief high current demand, such as a high inrush current during start-up. The output slew rate and the output capacitance will affect the AOCP during startup. At higher output voltages, a higher output slew rate or a higher output capacitance can false trigger AOCP at startup. The TON_RISE time should be increased or output capacitance should be reduced to avoid false triggering of AOCP.

The AOCP is activated when EN voltage is above its threshold. During AOCP events, the valley of the inductor current is regulated around the AOCP limit. But during the first switching cycle when the AOCP is tripped, the valley of the inductor current can drop slightly below the AOCP limit. It should be noted that AOCP events do not pull the PGOOD signal low unless the output voltage eventually drops below the Under Voltage Protection (UVP) threshold and triggers UVP.

The OCP limits are thermally compensated. The corresponding output dc current can be calculated as follows:

$$I_{out\_OCP} = I_{LIM} + \frac{\Delta i_L}{2}$$

Where: $I_{out\_OCP}$ = Output dc current when AOCP is tripped. $I_{LIM}$ = AOCP limit, which is the valley of inductor current. ΔiL = Peak-peak inductor ripple current.

To avoid the inductor saturation during AOCP events, the following criterion is recommended for the inductor saturation current rating.

$$I_{sat} \geq I_{LIM\_max} + \Delta i_L$$

Where: $I_{sat}$ is the inductor saturation current and $I_{LIM\_max}$ is the maximum spec of the AOCP limit.

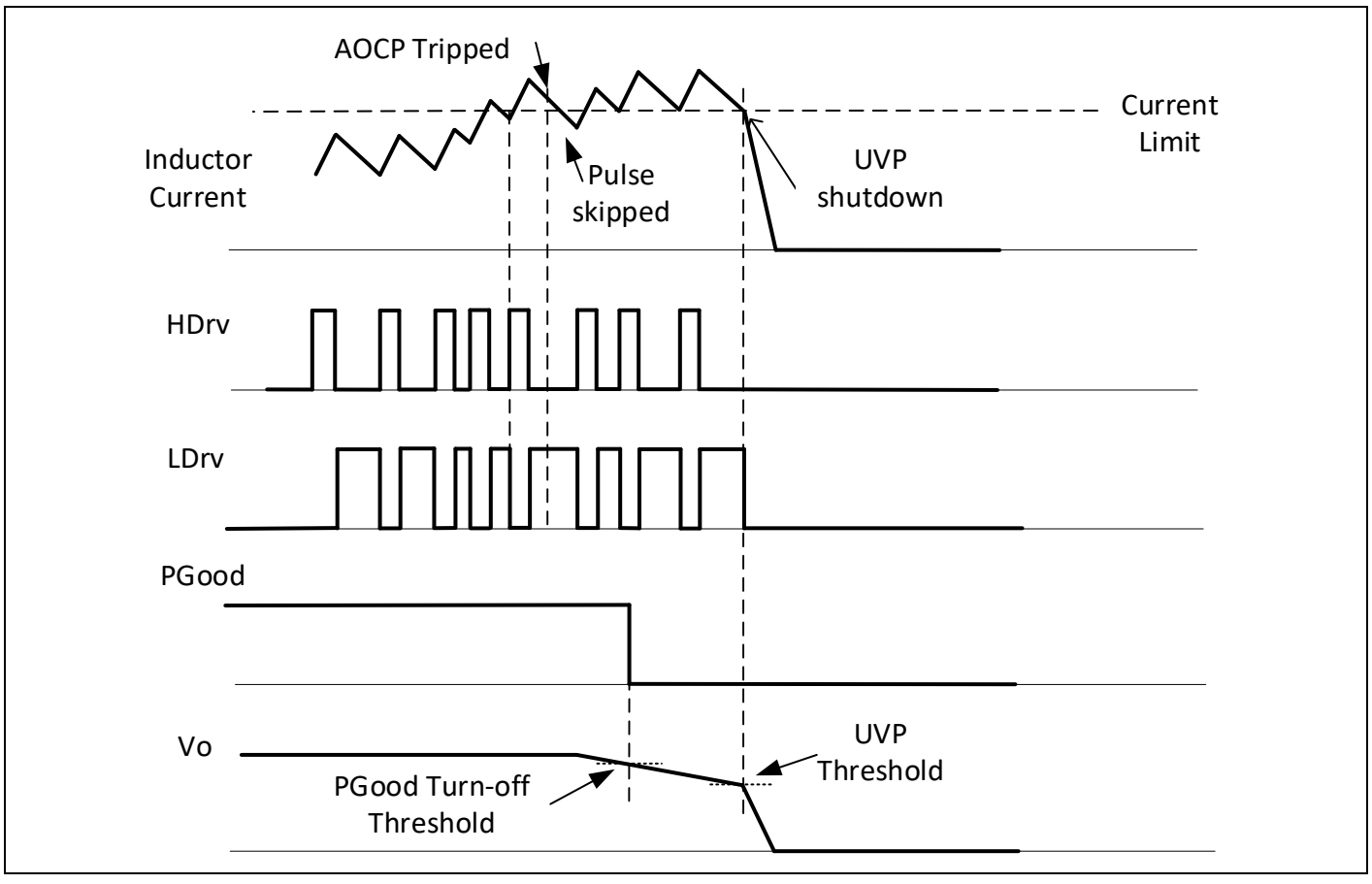



**Figure 22 AOCP response timing diagram.**

## 15.2 Output Under Voltage Protection (UVP)

The TDA38740/725 UVP response is a relative limit configurable from 50 mV to 400 mV in steps of 50 mV using the register bits relative_uvp_thresh[2:0] in configuration register 0x5e. The limit is programmed by VOUT_UV_FAULT_LIMIT PMBus command, and the response is programmed via the VOUT_UV_FAULT_RESPONSE command. Possible responses are ignore, shutdown, and retry indefinitely.

When using the VBT pin to set the output voltage, the VOUT_COMMAND value should be same as the VBT pinstrap setting to avoid improper UVP triggering.

When the UVP fault is triggered, a flag is raised and the part is tri-stated until the flag is cleared using the PMBus CLEAR_FAULTS command. The part is started again by either cycling the Vcc or the EN signal to the part. The shutdown response entails tri-stating both the MOSFETs and discharging the output either via a bleed resistor at the output or through the body diode of the low side FET.

If the response is set to retry, a user defined timer (1 ms to 8 ms in steps of 1 ms) is started as soon as the UVP fault is triggered and the output is tri-stated. At the end of the timer the output is checked against a fixed level of 250 mV. If the output is below this voltage, the start-up sequence is initiated. Otherwise, the timer is reset and the output tri-state continues (both the MOSFET's are tri-stated).

There are options for UVP protection to be lifted during voltage transitions (Vboot, Vout transition up and/or down) using the register bits blank_uv_sel[1:0] in configuration register 0x60. The options for this register are outlined in Table 15.

**Table 15 Optional UVP blanking via register blank_uv_sel (0x60[11:10]).**

| sel | Description |
|---|---|
| 3 | blank UV faults during Vout transition up or down (including Vboot) |
| 2 | blank UV faults during Vout transition up (including Vboot) |
| 1 | blank UV faults during Vboot |
| 0 | no UV fault blanking |

## 15.3 Over Voltage Protection (OVP)

The OVP response is divided into two parts: Fixed OVP (FOVP) and Relative OVP (ROVP). The Fixed OVP is typically used for start-up, all DVIDs, and when EN is low. ROVP covers all other situations during operation. Figure 23 depicts an example of when FOVP and ROVP are utilized.

When using the VBT pin to set the output voltage, the VOUT_COMMAND value should be the same as the VBT pinstrap setting to avoid improper ROVP triggering.

The FOVP has 8 distinct levels (0.8 V, 1 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V, 2.2 V, and 2.85 V in VOUT_SCALE_LOOP 1:1 and the levels are doubled in VOUT_SCALE_LOOP 1:2). FOVP is programmable via the configuration fixed_ovp_thresh [2:0] in configuration register 0x60. The response to an OVP event is programmed via the VOUT_OV_FAULT_RESPONSE command. OVP can have four responses: ignore, shutdown, and retry n (max 6) times after n (defined by PMBus) sec before latching and retry foreever. The threshold for ROVP is relative to the programmed output voltage, and can be set from 50 mV to 400 mV in steps of 50 mV. The OVP fault can also be blanked by using the bits [13:12] of register 0x60 in common regmap space. Please refer to Table 16 for more details. The threshold for ROVP is relative to the programmed output voltage, and can be set from 50 mV to 400 mV in steps of 50 mV using the I2C register relative_ovp_thresh [2:0] (0x5e [14:12]). The PMBUs commands could be over-ridden by using the relative_ovp_thresh_en (0x5e [15]) bit to over-ride the PMBUs commands.

**Table 16 Optional OVP blanking via blank_ov_sel(0x60[13:12])**

| sel | Description |
|---|---|
| 3 | blank OV faults during DVID up or down (including Vboot) |
| 2 | blank OV faults during DVID up (including Vboot) |
| 1 | blank OV faults during Vboot |
| 0 | no OV fault blanking |

When the output triggers an FOVP event the OVP flag is set, low side switch is turned ON and high side switch is turned OFF. The low side switch is turned ON till the output voltage is dragged down to the set FOVP threshold. After that the output voltage walks down to zero with its natural decay.

When the output triggers an ROVP event, the VID set point is moved to 0 V at a controlled slew rate of 30 V/uS and the OVP flag is set. Next the low side switch is turned ON and the high side is turned off. This allows the output to discharge until Vout set point reaches zero or Vout catches up with the VID set point at which point the low side and high side switched turn ON and OFF as required to maintain the output at the VID set point. How fast the output voltage discharges during this event is determined by the output voltage, output capacitance and output inductor. This determines if the output voltage is discharged to zero by the end of the controlled VID ramp down. At the end of the ramp, if the output is not already at zero, the output voltage will discharge to zero with its natural decay.

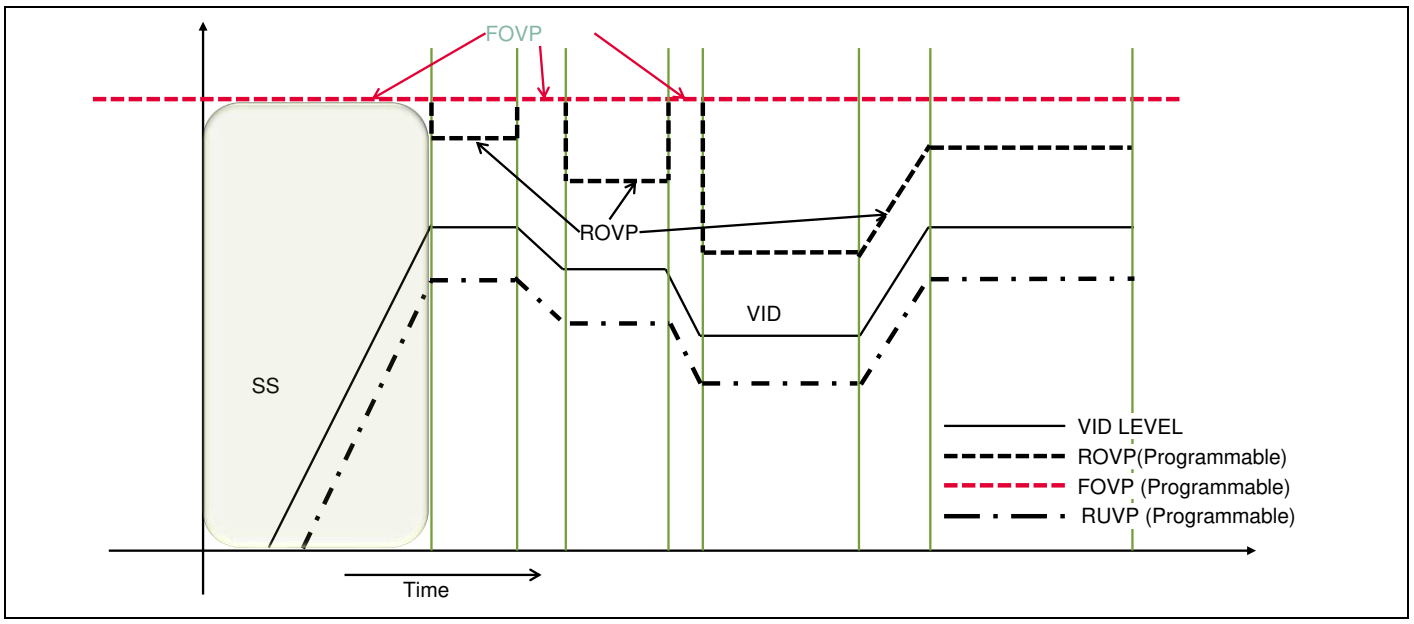



**Figure 23 OVP example diagram. Note the situations in which FOVP takes over from ROVP.**

## 15.4 Over Temperature Protection (OTP)

The temperature is measured by a thermal sensor in the controller die. Temperature protection is programmable via the OT_FAULT_LIMIT, OT_WARN_LIMIT, and OT_FAULT_RESPONSE PMBus registers. The TDA38740/725 supports three responses: ignore, shutdown, and retry idefinitely. The fault is non-latching.

An OTP event is triggered when the device temperature reaches the OT_FAULT_LIMIT. The switching output is tri-stated and the output discharges, while staying biased with the internal LDO on. With the output off, the device cools until reaching the OTP_WARN_LIMIT, and if set to retry, the device will hiccup with the potential for pre-biased startup.

## 15.5 Boot Under Voltage Lockout (UVLO)

The voltage from the BOOT pin to PHASE pin is monitored on the TDA38740/725. If the Boot UVLO lower threshold violation is detected within the PWM cycle, the event is counted and a fault is asserted after 10 violations. After 3 consecutive cycles without a BOOT UVLO event (above the lower threshold during the PWM cycle), the counter resets. To clear the fault Vcc or EN has to be cycled. The Boot UVLO fault is in the fail_code_sticky register.

## 15.6 Minimum On - Time and Minimum Off - Time

The minimum on-time refers to the shortest time for the Control MOSFET to be reliably turned on. The minimum off-time refers to the minimum time duration in which the Synchronous FET stays on before a new PWM pulse is generated. The minimum off-time is needed for TDA38740/725 to charge the bootstrap capacitor, and to sense the current of the Synchronous MOSFET for OCP.

For applications requiring a small duty cycle, it is important that the selected switching frequency results in an on-time larger than the maximum spec of the minimum on-time in the Section 7. Otherwise, the resulting switching frequency may be lower than the desired target. The following formula can be used to check for the minimum on-time requirement.

$$\frac{V_0}{kf_{sw} \times V_{in}} > \max\ spec\ of\ T_{on(\min)}$$

Where $f_{sw}$ is the desired switching frequency. *k* is the variation of the switching frequency. As a rule of thumb, select *k* = 1.25 to ensure design margin.

For applications requiring a high duty cycle, it is important to make sure a proper switching frequency is selected so that the resulting off-time is longer than the maximum spec of the minimum off-time in the Section 7 which can be calculated as shown below.

$$\frac{V_{in} - V_0}{kf_{sw} \times V_{in}} > \max\ spec\ of\ T_{off(\min)}$$

Where $f_{sw}$ is the desired switching frequency. *k* is the variation of the switching frequency. As a rule of thumb, select *k* = 1.25 to ensure the design margin.

The resulting maximum duty cycle is therefore determined by the selected on-time and minimum off-time.

$$D_{max} = \frac{T_{on}}{T_{on} + T_{off(\min)}}$$

## 15.7 High-Side Short (HSS) Detection

The TDA38740/725 offers high-side FET short detection. The phase pin is monitored when the low-side FET is active. HSS monitoring happens both at start-up and during normal operation. In an HSS event, if the HSS threshold is reached, the PGOOD pin is asserted. Once the HSS threshold is reached, the low-side FET is turned on and the switching stops. There is no current reporting during this time. The fault is sticky and only clears when either the VCC or EN signal is cycled.

# 16 Faults Communication

TDA38740/725 supports the the following FAULTs OCP, OVP, UVP and OTP via telemetry.

## 16.1 PMBUS Slave Addressing

The TDA38740/725 supports PMBus through the use of exclusive addressing. By using a 7-bit address, the user can configure the device to any one of 127 different PMBus addresses. Once the address of the TDA38740/725 is set, it can be locked to protect it from being overwritten. Optionally, a resistor can be tied to the SM_ADDR/PROG pin to generate an offset as shown in Figure 24 .

Setting a base 7-bit PMBus address of 40h with a resistor offset of +15 sets the 7-bit PMBus address to 4Fh.

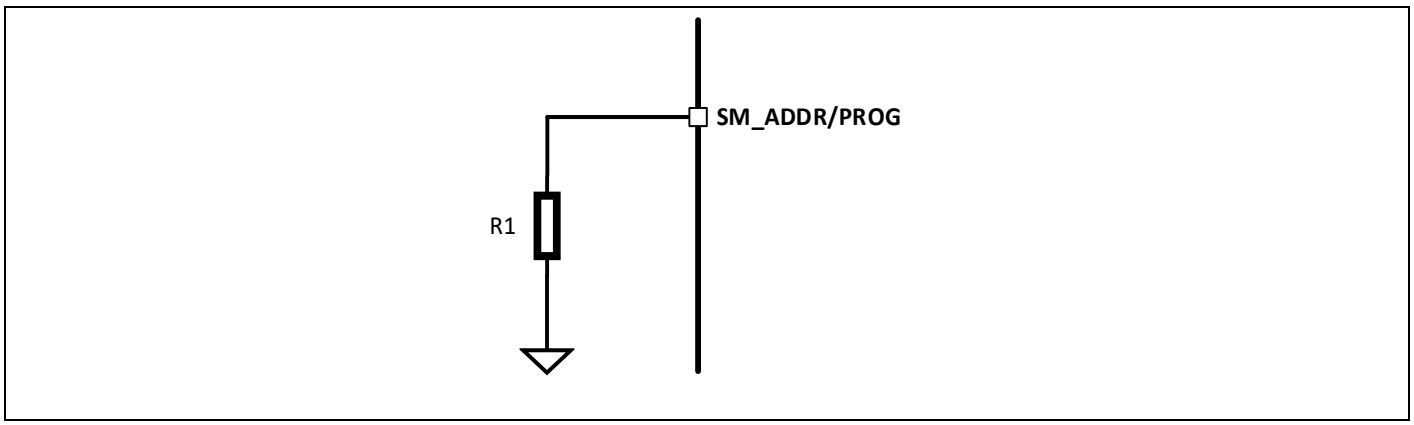



**Figure 24 SM-ADDR/PROG Pin Components**

## 16.2 Real-Time Telemetry

TDA38740/725 provides real-time accurate measurement of input voltage, output voltage, output current, temperature, output power, and input power over the PMBus interface. Output voltage is calculated based upon the output voltage setting and the result is reported through the PMBus.

## 16.3 SMBUS/PMBUS PROTOCOLS

To access TDA38740 and TDA38725 configuration and monitoring registers, 4 different protocols are required:

- the SMBus Read/Write Byte/Word protocol with/without PEC (for status and monitoring)
- the SMBus Send Byte protocol with/without PEC (for CLEAR_FAULTS only)
- the SMBus Block Read protocol for accessing Model and Revision information
- the SMBus Process call (for accessing Configuration Registers)

In addition, the TDA38740/725 supports:

- Alert Response Address (ARA)
- Bus timeout
- Group Command for writing to many VRs with one command

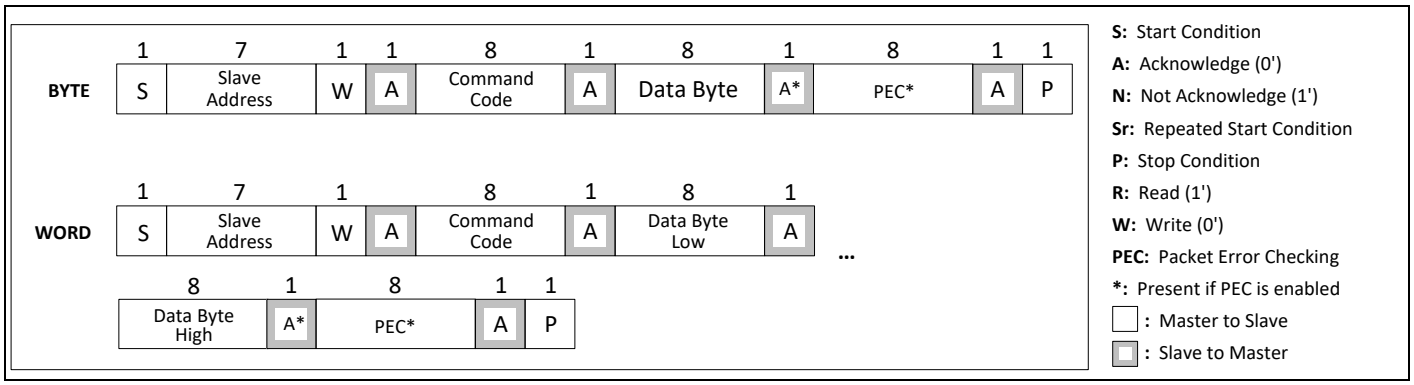



**Figure 25 SMBus Write Byte/Word**

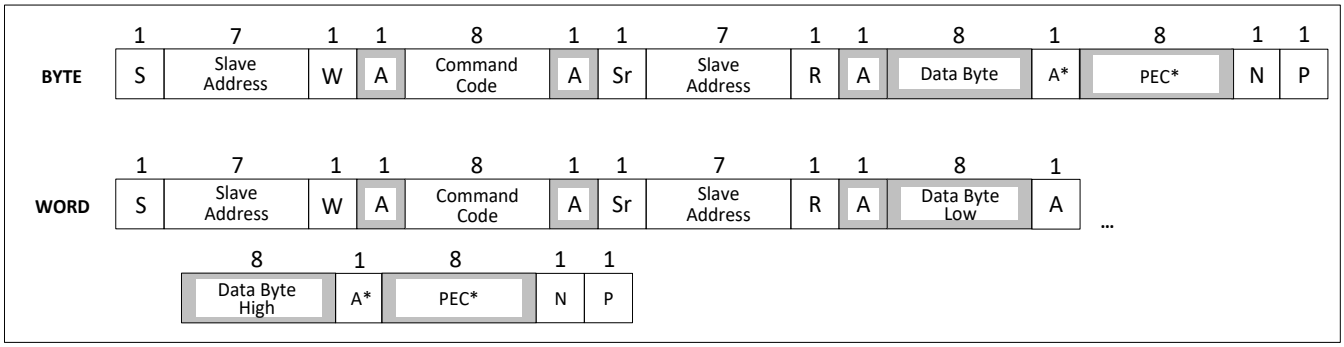



**Figure 26 SMBus Read Byte/Word**

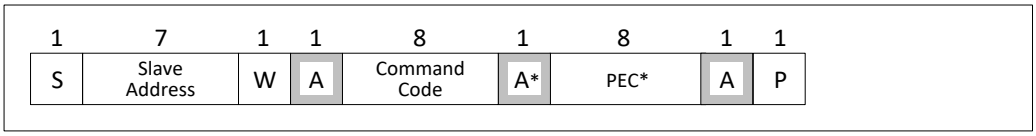



**Figure 27 SMBus Send Byte**

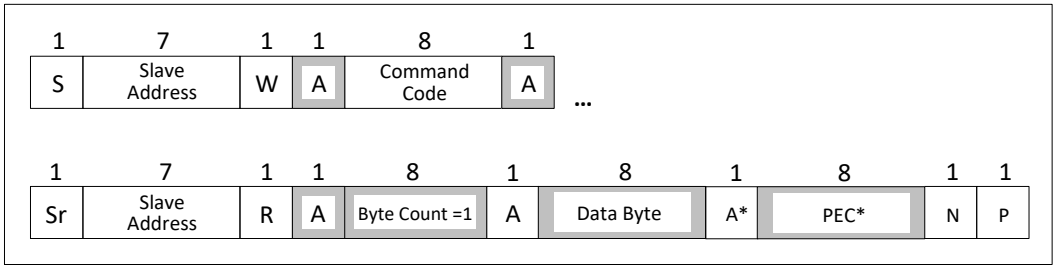



**Figure 28 SMBus Block Read with Byte Count=1**

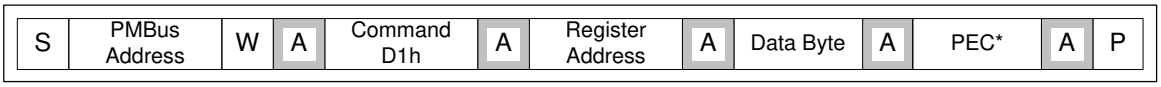



**Figure 29 MFR specific command to Write an IR Register**

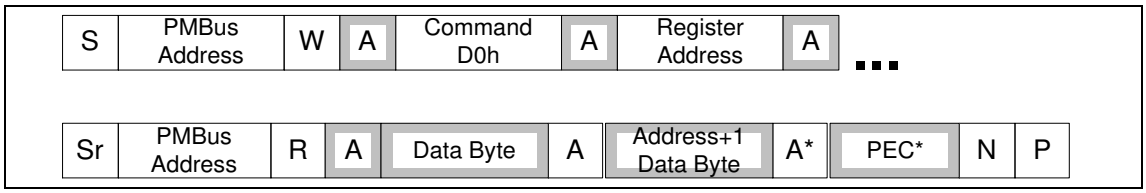



**Figure 30 SMBus Custom Process Call to Read an IR Register**

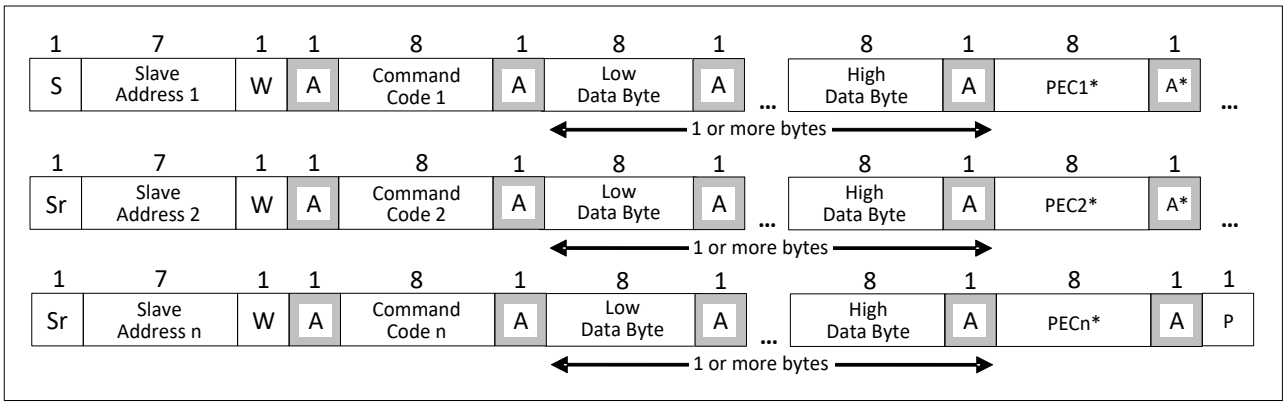



**Figure 31 Group Command**

**Table 17 PMBus Commands Supported**

| I2C Register Address | COMMAND | PMBus PROTOCOL | PMBus COMMAND CODE | DESCRIPTION |
|---|---|---|---|---|
| 0x200 | PAGE | Read/Write Byte | 00h | Allows access of each loop via paging. |
| 0x202 | OPERATION | Read/Write Byte | 01h | Enables or disables the output and controls margining. Ignores OVP on Margin High, UVP on Margin Low. |
| 0x204 | ON_OFF_CONFIG | Read/Write Byte | 02h | Configures the combination of CONTROL pin and OPERATION commands needed to turn the unit on and off. |
| 0x206 | CLEAR FAULTS | Send Byte | 03h | Clears contents of Fault registers |
| 0x20A | PAGE_PLUS_WRITE | Write Block | 05h | Set the PAGE within a device, send a command, and send the data for the command in one packet. |
| 0x20C | PAGE_PLUS_READ | Block Write/ Block Read Process Call | 06h | Set the PAGE within a device, send a command, and read the returned data by the command in one packet |

| I2C Register Address | COMMAND | PMBus PROTOCOL | PMBus COMMAND CODE | DESCRIPTION |
|---|---|---|---|---|
| 0x220 | WRITE_PROTECT | Read/Write Byte | 10h | Protects from overwriting the configuration files and modes accidentally |
| 0x222 | STORE_DEFAULT_ALL | Sen Byte | 11h | Instructs the device to copy the entire contents of the configuration registers to the NVM |
| 0x224 | RESTORE_DEFAULT_ALL | Send Byte | 12h | Reloads the OTP |
| 0x22A | STORE_USER_ALL | Send Byte | 15h | Stores the user OTP section |
| 0x22C | RESTORE_USER_ALL | Send Byte | 16h | Reloads the user OTP section |
| 0x232 | CAPABILITY | Read Byte | 19h | Returns 1010xxxx to indicate Packet Error Checking is supported. Maximum bus speed is 400 kHz |
| 0x236 | SMBALERT_MASK | Block Write/ Block Read Process Call | 1Bh | Set to prevent warning or fault conditions from asserting the SMBALERT# signal. Write command code for STATUS register to be masked in the low byte, the bit to be masked in the High byte. |
| 0x240 | VOUT_MODE | Read/Write Byte | 20h | Sets the format for VOUT related commands. Linear mode, -8, -9, and -12 exponents supported. |
| 0x242 | VOUT_COMMAND | Read/Write Word | 21h | Sets the voltage to which the device should set the output. Format according to VOUT_MODE. Resolution is 5 mV when the IC Vout is configured with a load line. Resolution is 5 mV or 0.625 mV when the IC is configured without a load line. |
| 0x248 | VOUT_MAX | Read/Write Word | 24h | Sets an upper limit on the output voltage the unit can command. Format according to VOUT_MODE. |
| 0x24A | VOUT_MARGIN_HIGH | Read/Write Word | 25h | Sets the margin high voltage when commanded by OPERATION. Must be in format determined by VOUT_MODE. |
| 0x24C | VOUT_MARGIN_LOW | Read/Write Word | 26h | Sets the margin low voltage when commanded by OPERATION. Must be in format determined by VOUT_MODE. |
| 0x24E | VOUT_TRANSITION_RATE | Read/Write Word | 27h | Sets the rate at which the output changes voltage due to VOUT_COMMAND or OPERATION commands. |
| 0x250 | VOUT_DROOP | Read/Write Word | 28h | Allows the user to set the load-line value in resolution of 5/256 Ω. Exponent is 1 |
| 0x252 | VOUT_SCALE_LOOP | Read/Write Word | 29h | Used to account for any external attenuation network on VOUT sense feedback and provide correct VOUT reporting. |
| 0x256 | VOUT_MIN | Read/Write Word | 2Bh | Sets a lower limit on the commanded output voltage. Format according to VOUT_MODE |
| 0x266 | FREQUENCY_SWITCH | Read/Write Word | 33h | Sets the switching frequency in kHz per table found in user note UN0047. Exp = 0, 1 |
| 0x26A | VIN_ON | Read/Write Word | 35h | Sets the value of the input voltage at which the unit should begin power conversion. Exp = -1. |

| I2C Register Address | COMMAND | PMBus PROTOCOL | PMBus COMMAND CODE | DESCRIPTION |
|---|---|---|---|---|
| 0x26C | VIN_OFF | Read/Write Word | 36h | Sets the value of the input voltage at which the unit, once operation has started, should stop power conversion. Exp = -1. |
| 0x270 | IOUT_CAL_GAIN | Read/Write Word | 38h | Used to calibrate the output current's gain |
| 0x272 | IOUT_CAL_OFFSET | Read/Write Word | 39h | Used to null out any offsets in the output current sensing circuitry. Exp = 2. |
| 0x280 | VOUT_OV_FAULT_ LIMIT | Read Only | 40h | Returns the value of the output voltage, measured at the sense or output pins, that causes an output over voltage fault. |
| 0x282 | VOUT_OV_FAULT_ RESPONSE | Read/Write Byte | 41h | Instructs the device on what action to take in response to an output over voltage fault. Only shutdown and ignore are supported. |
| 0x288 | VOUT_UV_FAULT_ LIMIT | Read Only | 44h | Returns the value of the output voltage, measured at the sense or output pins, that causes an output under voltage fault. |
| 0x28A | VOUT_UV_FAULT_ RESPONSE | Read/Write Byte | 45h | Instructs the device on what action to take in response to an output under voltage fault. Only shutdown and ignore are supported. |
| 0x28C | IOUT_OC_FAULT_ LIMIT | Read/Write Word | 46h | Sets the value of the output current, in amperes, that causes the over current detector to indicate an over current fault condition. Set by writing this command in Linear format with a -1 exponent. |
| 0x28E | IOUT_OC_FAULT_ RESPONSE | Read/Write Byte | 47h | Instructs the device on what action to take in response to an output over current fault. Only C0h (shutdown immediately), F8h (hiccup forever), and D8 (hiccup 3 times) are supported. |
| 0x29E | OT_FAULT_LIMIT | Read/Write Word | 4Fh | Sets the temperature, in degrees Celsius, of the unit at which it should indicate an over temperature fault. Exp = 0. |
| 0x2A0 | OT_FAULT_RESPONSE | Read/Write Byte | 50h | Instructs the device on what action to take in response to an over temperature fault. Only shutdown and ignore are supported. |
| 0x2A2 | OT_WARN_LIMIT | Read/Write Word | 51h | Sets the temperature, in degrees Celsius, of the unit at which it should indicate an over temperature Warning alarm. Exp = 0. |
| 0x2AA | VIN_OV_FAULT_LIMIT | Read/Write Word | 55h | Sets the value of the input voltage that causes an input over voltage fault. Exp = -4. |
| 0x2AC | VIN_OV_FAULT_RESPONSE | Read/Write Byte | 56h | Instructs the device on what action to take in response to an input over voltage fault. Only shutdown and ignore are supported. |
| 0x2BC | POWER_GOOD_ON | Read/Write Word | 5Eh | Sets the output voltage at which an optional POWER_GOOD signal should be asserted. Format according to VOUT_MODE. See Note 14 |

| I2C Register Address | COMMAND | PMBus PROTOCOL | PMBus COMMAND CODE | DESCRIPTION |
|---|---|---|---|---|
| 0x2BE | POWER_GOOD_OFF | Read/Write Word | 5Fh | Sets the output voltage at which an optional POWER_GOOD signal should be negated. Format according to VOUT_MODE. See Note 14 |
| 0x2C0 | TON_DELAY | Read/Write Word | 60h | Sets the time, in milliseconds, from when a start condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to rise. Exp = 0. |
| 0x2C2 | TON_RISE | Read/Write Word | 61h | Sets the time, in milliseconds, from when the output starts to rise until the voltage has entered the regulation band. Exp = 0. |
| 0x2C8 | TOFF_DELAY | Read/Write Word | 64h | Sets the time (in ms) from when a stop condition is received (as programmed by the ON_OFF_CONFIG command) until the unit stops transferring energy to the output. Exp = 0. |
| 0x2CA | TOFF_FALL | Read/Write Word | 65h | Sets the time, in milliseconds, from the end of the turn-off delay time until the voltage is commanded to zero. Exp = 0. |
| 0x2F0 | STATUS_BYTE | Read/Write Byte | 78h | Returns 1 byte where the bit meanings are:<br>Bit <7> Reserved<br>Bit <6> Output off (due to fault or enable)<br>Bit <5> Output over-voltage fault<br>Bit <4> Output over current fault<br>Bit <3> Input Under voltage fault<br>Bit <2> Temperature fault<br>Bit <1> Communication/Memory/Logic fault<br>Bit <0>: None of the Above |
| 0x2F2 | STATUS_WORD | Read/Write Word | 79h | Returns 2 bytes where the Low byte is the same as the STATUS_BYTE data. The High byte has bit meanings are:<br>Bit <7> Output high or low fault<br>Bit <6> Output over current fault<br>Bit <5> Input voltage or current fault.<br>Bit <4> MFR_SPECIFIC<br>Bit <3> POWR GOOD#<br>Bit <2:0> Not Supported |
| 0x2F4 | STATUS_VOUT | Read/Write Byte | 7Ah | Bit <7> Output over voltage Fault<br>Bit <6> Not Supported<br>Bit <5> Not Supported<br>Bit <4> Output under voltage Fault<br>Bit <3> VOUT_MAX Warning<br>Bit <2:0> Not Supported |

| I2C Register Address | COMMAND | PMBus PROTOCOL | PMBus COMMAND CODE | DESCRIPTION |
|---|---|---|---|---|
| 0x2F6 | STATUS_IOUT | Read/Write Byte | 7Bh | Bit <7> Output Over current Fault<br>Bit <6> Not Supported<br>Bit <5> Output Overcurent Warning<br>Bit <4:0> Not Supported |
| 0x2F8 | STATUS_INPUT | Read/Write Byte | 7Ch | Bit <7> Input over voltage Fault<br>Bit <6:0> Not Supported |
| 0x2FA | STATUS_TEMPERATURE | Read/Write Byte | 7Dh | Bit <7> Over Temperature Fault<br>Bit <6> Over Temperature Warning<br>Bit <5:0> Reserved |
| 0x2FC | STATUS_CML | Read/Write Byte | 7Eh | Returns 1 byte where the bit meanings are:<br>Bit <7> Invalid or unsupported command<br>Bit <6> Invalid or unsupported data<br>Bit <5> PEC fault<br>Bit <4:2> Reserved<br>Bit <1> Other communication fault not listed here<br>Bit <0> Reserved |
| 0x310 | READ_VIN | Read Word | 88h | Returns the input voltage in Volts |
| 0x312 | READ_IIN | Read Word | 89h | Returns the input current in Amperes |
| 0x316 | READ_VOUT | Read Word | 8Bh | Returns the output voltage in the format set by VOUT_MODE |
| 0x318 | READ_IOUT | Read Word | 8Ch | Returns the output current in Amperes |
| 0x31A | READ_TEMPERATURE_1 | Read Word | 8Dh | Returns the addressed loop NTC temperature in degrees Celsius |
| 0x32C | READ_POUT | Read Word | 96h | Returns the output power in Watts |
| 0x32E | READ_PIN | Read Word | 97h | Returns the input power in Watts |
| 0x330 | PMBUS_REVISION | Read Byte | 98h | Reports PMBus Part I rev 1.1 & PMBUs Part II rev 1.2 |
| 0x332 | MFR_ID | Block Read/Write Byte count = 2 | 99h | The MFR_ID is set to IR (ASCII 52 49) unless programmed differently in the USER registers of the controller. |
| 0x334 | MFR_MODEL | Block Read, Byte count = 1 | 9Ah | The MFR_MODEL is the same as the device ID if the USER register for Manufacturer model is 00. Otherwise MFR_Model command returns the value in the USER register for MFR_MODEL. |
| 0x336 | MFR_REVISION | Block Read, Byte count = 2 | 9Bh | The MFR_REVISION is the same as the device revision if the USER register for Manufacturer revision is 00. Otherwise MFR_REVISION command returns the value in the USER register for MFR_REVISION. |
| 0x35A | IC_DEVICE_ID | Block Read | ADh | Returns a 1-byte code with the following values:<br>84h = TDA38740 |
| 0x35C | IC_DEVICE_REV | Block Read | AEh | The IC revision that is stored inside the IC |

| I2C Register Address | COMMAND | PMBus PROTOCOL | PMBus COMMAND CODE | DESCRIPTION |
|---|---|---|---|---|
| 0x3A0 | MFR_READ/WRITE_ REG | Custom MFR protocol | D0h | Read/Write I2C registers |
| 0x382 | MFR_VENDOR_INFO_1 | Read Word | C1h | Returns the product id and silicon revision |
| 0x384 | MFR_VENDOR_INFO_2 | Read/ write Wod | | Available for vendor use. Default 0x0 |

*Note:*

14. *PGOOD_ON and PGOOD_OFF thresholds are asserted at half of the programmed value when VOUT_SCALE_LOOP is set to 1:2 mode. The threshold values should be set to twice of the desired PGOOD levels.*

## 16.4 11-BIT Linear Data Format

Monitored parameters use the Linear Data Format encoding into 1 Word (2 bytes), where:

$$Value = Y * 2^N$$

Note N and Y are “signed” values. If VOUT is set to linear format (by VOUT_MODE), then N is set by the VOUT_MODE command and only Y is returned in the data-field as a 16-bit unsigned number.

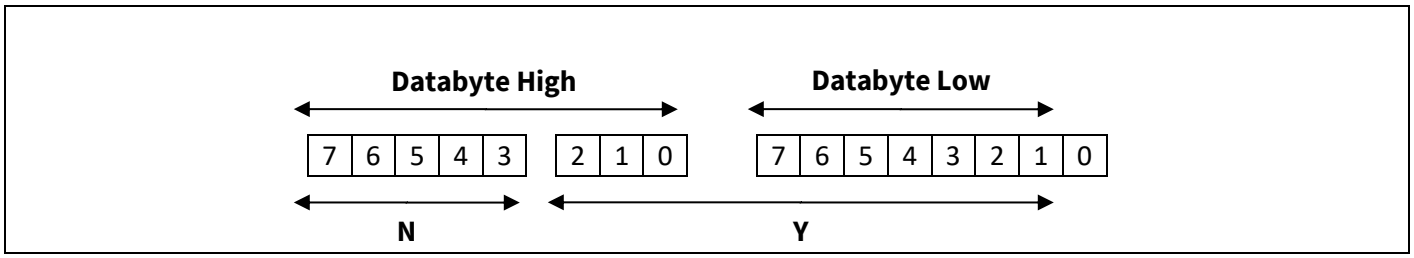



**Figure 32 11-Bit Linear Data Format**

## 16.5 16-BIT Linear Data Format

This format is only used for VOUT related commands (READ_VOUT, VOUT_COMMAND, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW, POWER_GOOD_ON, and POWER_GOOD_LOW):

$$Value = Y * 2^N$$

Note N and Y are “signed” values. If VOUT is set to linear format (by VOUT_MODE), then N is set by the VOUT_MODE command and only Y is returned in the data-field as a 16-bit unsigned number.

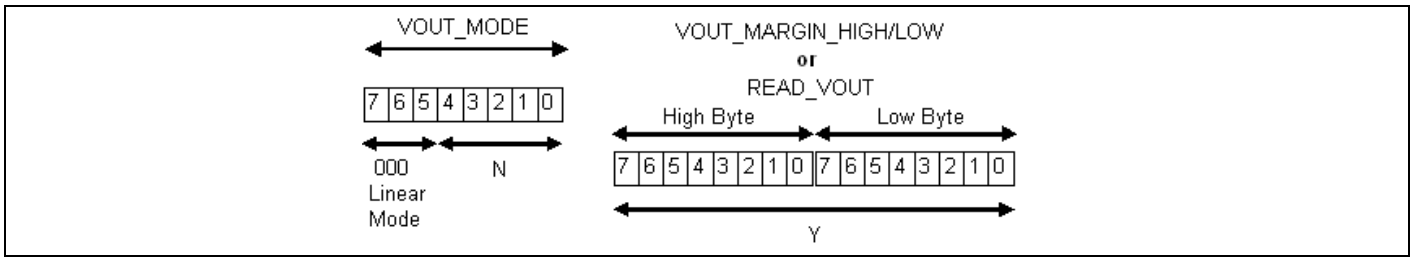


**Figure 33 16-BIT Linear Data Format**

# 17 Design example

In this section, an example is used to explain how to design a buck regulator with the TDA38740/725. The application circuit is shown in Figure 3. The design specifications are given below.

- $PV_{in}$ = 12 V (±10%)
- $V_o$ = 1.0 V
- $I_o$ = 40 A
- $V_o$ ripple voltage = ±1% of $V_o$
- Load transient response = ± 3% of $V_o$ with a step load current = 9 A and slew rate = 30 A/µs

## 17.1 Enabling the TDA38740/725

The TDA38740/725 has a precise Enable threshold voltage, the Enable feedback resistor, $R_{EN1}$ and $R_{EN2}$, can be calculated as follows.

$$PV_{in(\min)} \times \frac{R_{EN2}}{R_{EN1} + R_{EN2}} \geq V_{EN(\max)}$$

$$R_{EN2} \geq R_{EN1} \times \frac{V_{EN(\max)}}{PV_{in(\min)} - V_{EN(\max)}}$$

Where $V_{EN(max)}$ is the maximum spec of the En-start-threshold as defined in the Absolute Maximum Ratings table. For $PV_{in\ (min)}$=10.8 V, select $R_{EN1}$=49.9 kΩ and $R_{EN2}$=7.5 kΩ.

## 17.2 Programming the Switching Frequency and Operation Mode

The TDA38740/725 has very good efficiency performance and is suitable for high switching frequency operation. In this case, 800 kHz is selected to achieve a good compromise between the efficiency, passive component size and dynamic response. In addition, FCCM operation is selected to ensure a small output ripple voltage over the entire load range. The switching frequency and FCCM operation can be selected via register bits.

## 17.3 Selecting Input Capacitors

Without input capacitors, the pulse current of Control MOSFET is directly from the input supply power. Due to the impedance on the cable, the pulse current can cause disturbance on the input voltage and potential EMI issues. The input capacitors filter the pulse current, resulting in almost constant current from the input supply. The input capacitors should be selected to tolerate the input pulse current, and to reduce the input voltage ripple. The RMS value of the input ripple current can be expressed by:

$$I_{RMS} = I_o \times \sqrt{D \times (1 - D)}$$

$$D = \frac{V_o}{PV_{in}}$$

Where $I_{RMS}$ is the RMS value of the input capacitor current. $I_o$ is the output current and D is the Duty Cycle. For $I_o$ = 40 A and $D_{(max)}$ = 0.09, the resulting RMS current flowing into the input capacitor is $I_{rms}$ = 11.6 A.

To meet the requirement of the input ripple voltage, the minimum input capacitance can be calculated as follows.

$$C_{in(\min)} > \frac{I_o \times (1-D) \times D}{f_{sw} \times (\Delta PV_{in} - ESR \times I_o \times (1-D))}$$

Where $\Delta PV_{in}$ is the maximum allowable peak-to-peak input ripple voltage, and ESR is the equivalent series resistor of the input capacitors. Ceramic capacitors are recommended due to low ESR, ESL and high RMS current capability. For $I_o$ = 40 A, $f_{sw}$ = 800 kHz, ESR = 3 mΩ, and $\Delta PV_{in}$ = 240 mV, $C_{in(min)}$ > 32 µF. To account for the de-rating of ceramic capacitors under a bias voltage, 8 x 22 µF/0805/25 V MLCC and 1 x 4.7uF/25 V MLCC are used for the input capacitors. In addition, a bulk capacitor is recommended if the input supply is not located close to the voltage regulator.

## 17.4 Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. A low inductor value results in a large ripple current, lower efficiency and high output noise, but helps with size reduction and transient load response. Generally, the desired peak-to-peak ripple current in the inductor (Δi) is found between 20% and 50% of the output current.

The inductor saturation current must be higher than the maximum spec of the OCP limit plus the peak-to-peak inductor ripple current. For some core material, inductor saturation current may decrease as the increase of temperature. So it is important to check the inductor saturation current at the maximum operating temperature.

The inductor value for the desired operating ripple current can be determined using the following relation:

$$L = (PV_{in(\max)} - V_o) \times \frac{D_{min}}{\Delta i_{L(\max)} \times F_{sw}}$$

$$D_{min} = \frac{V_o}{PV_{in(\max)}}$$

$$I_{sat} \geq OCP_{max} + \Delta i_{L(\max)}$$

Where: $PV_{in(max)}$ = Maximum input voltage; $\Delta iL_{max}$ = Maximum peak-to-peak inductor ripple current; $OCP_{max}$ = maximum spec of the OCP limit as defined in Section 15.1, and $I_{sat}$ = inductor saturation current. In this case, select inductor L =150 nH to achieve $\Delta iL_{max}$ = 25% of $I_{omax}$. The $I_{sat}$ should be no less than 52 A.

## 17.5 Output Capacitor Selection

The output capacitor selection is mainly determined by the output voltage ripple and transient requirements.

To satisfy the $V_o$ ripple requirement, $C_o$ should satisfy the following criterion.

$$C_o > \frac{\Delta i_{Lmax}}{8 \times \Delta V_{or} \times f_{sw}}$$

Where $\Delta V_{or}$ is the desired peak-to-peak output ripple voltage. For $\Delta iL_{max}$= 7.5 A, $\Delta V_{or}$ =20 mV, $f_{sw}$ = 800 kHz, $C_o$ must be larger than 59 µF. The ESR and ESL of the output capacitors, as well as the parasitic resistance or inductance due to PCB layout, can also contribute to the output voltage ripple. It is suggested to use Multi-Layer Ceramic Capacitor (MLCC) for their low ESR, ESL and small size.

To meet the transient response requirements, the output capacitors should also meet the following criterion.

$$C_o > \frac{L \times \Delta I^2_{o(\max)}}{2 \times \Delta V_{oL} \times V_o}$$

Where $\Delta V_{OL}$ is the allowable $V_o$ deviation during the load transient. $\Delta I_{o(max)}$ is the maximum step load current. Please note that the impact of ESL, ESR, control loop response, transient load slew rate, and PWM latency is not considered in the calculation shown above. Extra capacitance is usually needed to meet the transient requirements. As a rule of thumb, we can triple the $C_o$ that is calculated above as a starting point, and then optimize the design based on the bench measurement. In this case, to meet the transient load requirement (i.e. $\Delta V_{OL}$= 30 mV, $\Delta I_{o(max)}$ = 9 A), select $C_o$ = ~600 µF. For more accurate estimation of $C_o$, simulation tool should be used to aid the design.

## 17.6 Bootstrap Capacitor

For most applications, a 0.1 µF ceramic capacitor is recommended for bootstrap capacitor placed between PHASE and BOOT Pin. For applications requiring $PV_{in}$ equal to or above 14 V, a small resistor of 1~2 Ω should be used in series with the BOOT pin to ensure the maximum SW node spike voltage does not exceed 20 V.

## 17.7 VI and VCC/LDO bypass Capacitor

Please see the recommendation in 13.4 on the internal LDO. A 10 µF MLCC is selected for the VCC/LDO bypass capacitor and a 4.7 µF MLCC is selected for the VIN bypass capacitor.

## 17.8 Design Recommendations

Listed below are the design recommendations for proper device operation:

- A 100 Ohm minimum load resistor should be connected across the output
- Add a 0.1 uF and 1 uF ceramic cap across PVIN and PGND
- Add 0.1 uF and 2.2 uF across VDRV to PGND.
- The internal LDO should not be used to power external devices

# 18 Layout Recommendations

PCB layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results. Following design guidelines are recommended to achieve the best performance.

- Bypass capacitors, including input/output capacitors, VIN, VCC and VDRV bypass capacitors, should be placed near the corresponding pins as close as possible.
- Place bypass capacitors from TDA38740/725 power input (Drain of Control MOSFET) to PGND (Source of Synchronous MOSFET) to reduce noise and ringing in the system. The output capacitors should be terminated to a ground plane that is away from the input PGND to mitigate the switching spikes on the Vo. The bypass capacitor shared by VCC and VDRV should be terminated to PGND.
- Place a boot strap capacitor near the TDA38740/725 BOOT and PHASE pin as close as possible to minimize the loop inductance.
- SW node copper should only be routed on the top layer to minimize the impact of switching noises
- Connect AGND pin to the PGND pad through a single point connection. On the TDA38740/725 demo board, AGND pin is connected to the exposed PGND pad with a copper trace.
- Via holes can be placed on PVin and PGND pads to aid thermal dissipation.
- Wide copper polygons are desired for PVin and PGND connections in favor of power losses reduction and thermal dissipation. Sufficient via holes should be used to connect power traces between different layers.
- Output voltage sensing in TDA38740/725 is done differentially using the VOSENP and VOSENM pins.
    - A pair of PCB traces with at least 15 mil trace width, running close to each other and away from any noise sources such as inductor and SW nodes, should be used to implement Kelvin sensing of the voltage across a high-frequency bypass capacitor of 0.1 µF or higher.
    - The ground connection of the remote sensing signal must be terminated at VOSENM pin.
    - The Vo connection of the remote sensing signal must be connected to the feedback resistor divider with the lower feedback resistor terminated at VOSENM pin for output voltages greater than 2.5 V.
    - Shield the pair of remote sensing lines with ground planes above and below.
    - Do **NOT** connect VOSENM pin and AGND pin in this configuration
- The EN pin and configuration pins including SM_ADDRS/PROG, VBT, TON/MODE, and ILIM should be terminated to a quiet ground. On the TDA38740/725 standard demo board, they are terminated to the PGND copper plane away from the power current flow. Alternatively, they can be terminated to a dedicated AGND PCB trace.

## 18.1 PCB Metal and Component Placement

Evaluation has shown that the best overall performance is achieved using the substrate/PCB layout as shown in the following figures. PQFN devices should be placed to an accuracy of 0.050 mm on both X and Y axes. Self-centering behavior is highly dependent on solders and processes, and experiments should be run to confirm the limits of self-centering on specific processes.

For further information, please refer to “SupIRBuck™ Multi-Chip Module (MCM) Power Quad Flat No-Lead (PQFN) Board Mounting Application Note.” (AN1132)

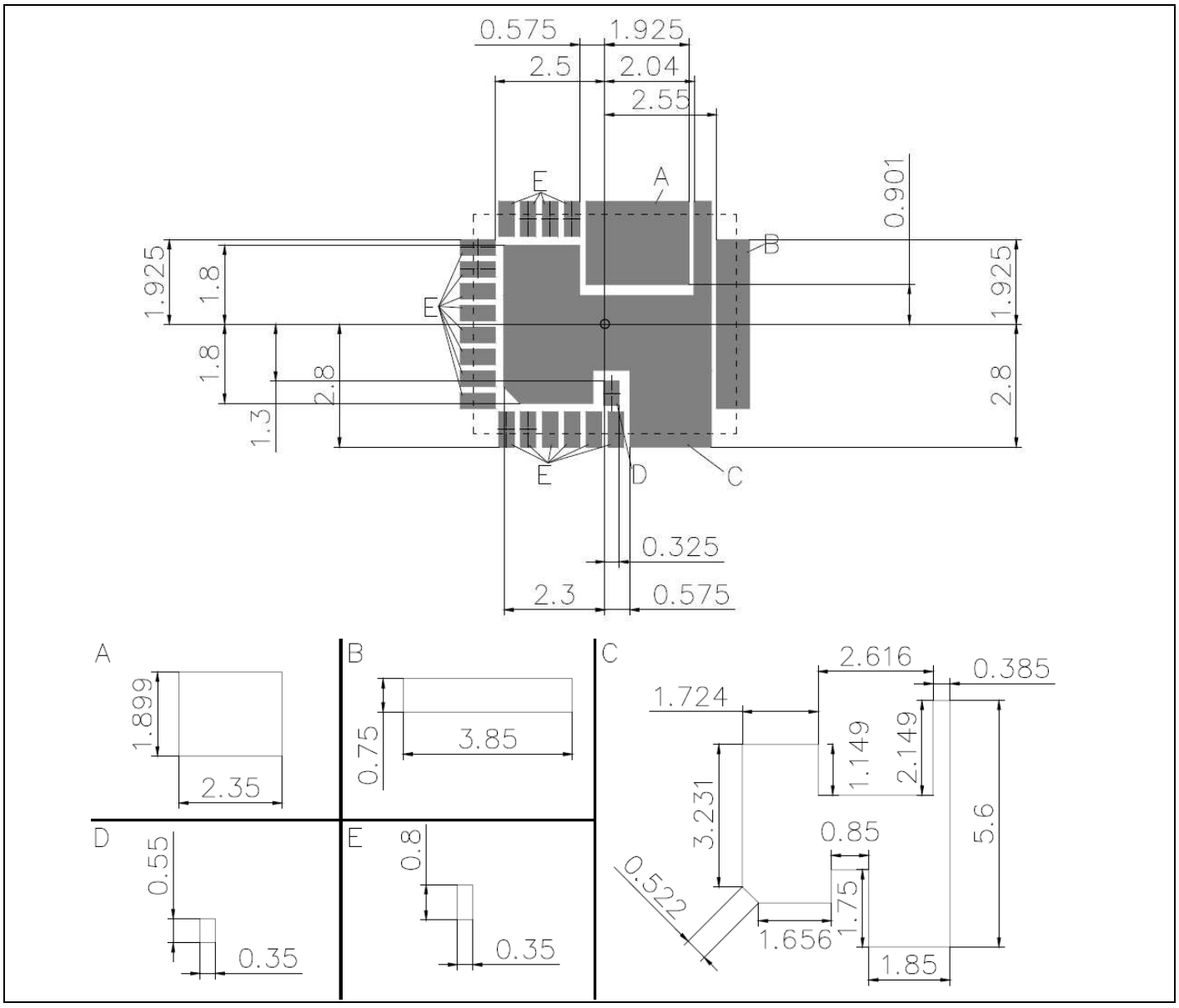



**Figure 34 PCB metal pad sizing and spacing (all dimensions in mm)**

## 18.2 Solder Resist

Infineon recommends that larger Power or Land Area pads are Solder Mask Defined (SMD.) This allows the underlying copper traces to be as large as possible, which helps in terms of current carrying capability and device cooling capability. When using SMD pads, the underlying copper traces should be at least 0.05 mm larger (on each edge) than the Solder Mask window, in order to accommodate any layer to layer misalignment. (i.e. 0.1 mm in X & Y.) When using NSMD pads, the Solder Resist Window should be larger than the Copper Pad by at least 0.025 mm on each edge, (i.e. 0.05 mm in X&Y,) in order to accommodate any layer to layer misalignment. Ensure that the solder resist in-between the smaller signal lead areas is at least 0.15 mm wide, due to the high x/y aspect ratio of the solder mask strip.

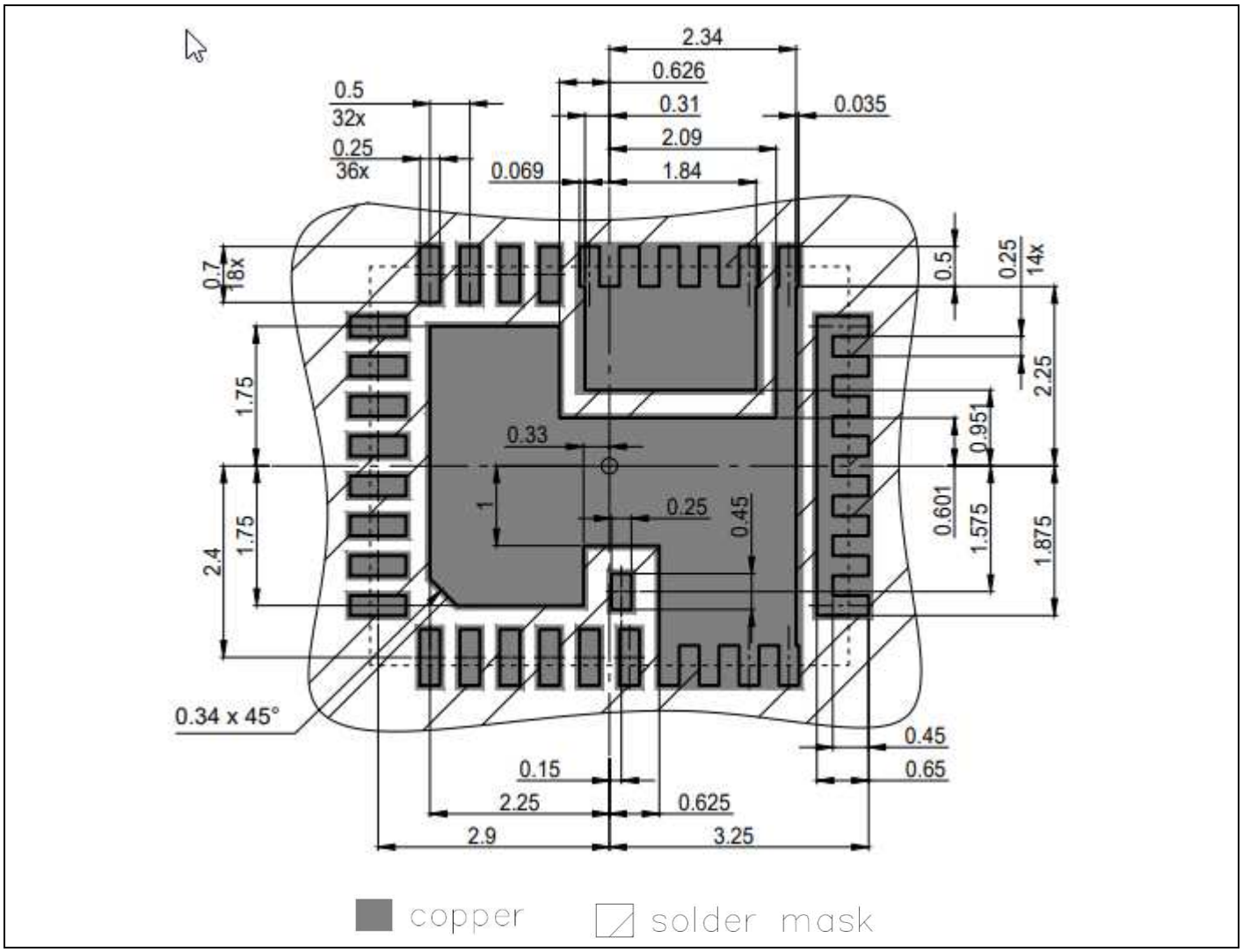



**Figure 35 Solder resist**

## 18.3 Stencil Design

Stencils for PQFN packages can be used with thicknesses of 0.100-0.250 mm (0.004-0.010”). Stencils thinner than 0.100 mm are unsuitable because they deposit insufficient solder paste to make good solder joints with the ground

pad; high reductions sometimes create similar problems. Stencils in the range of 0.125 mm-0.200 mm (0.005-0.008”), with suitable reductions, give the best results.

A recommended stencil design is shown in Figure 36. This design is for a stencil thickness of 0.127 mm (0.005”). The reduction should be adjusted for stencils of other thicknesses.

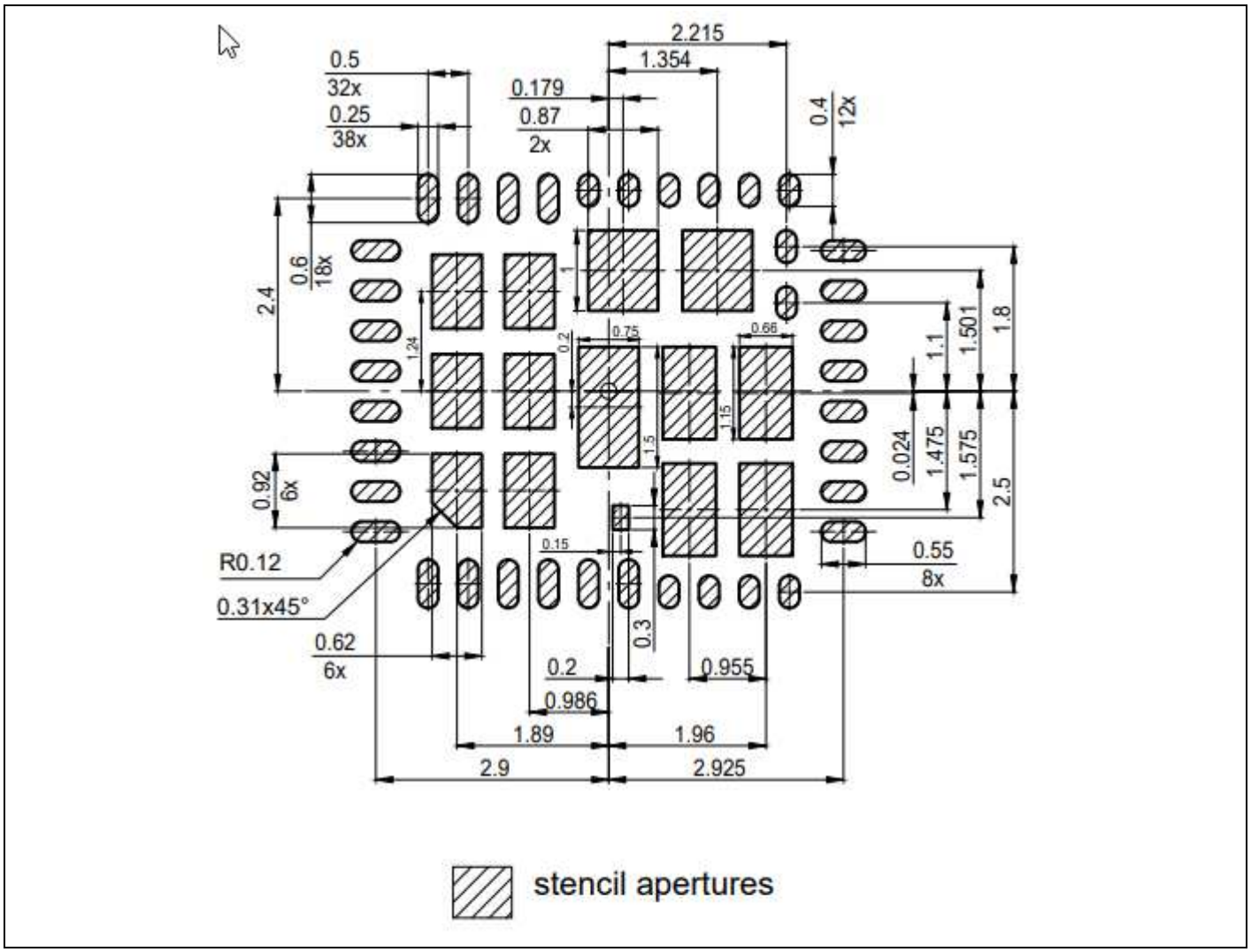



**Figure 36 Stencil pad size and spacing (all dimensions in mm)**

# 19 Package

## 19.1 Marking Information

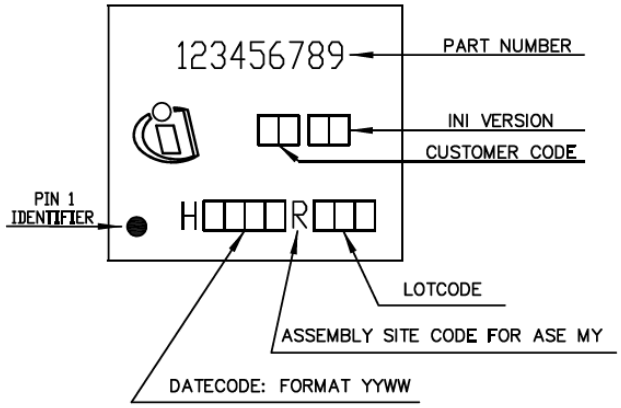
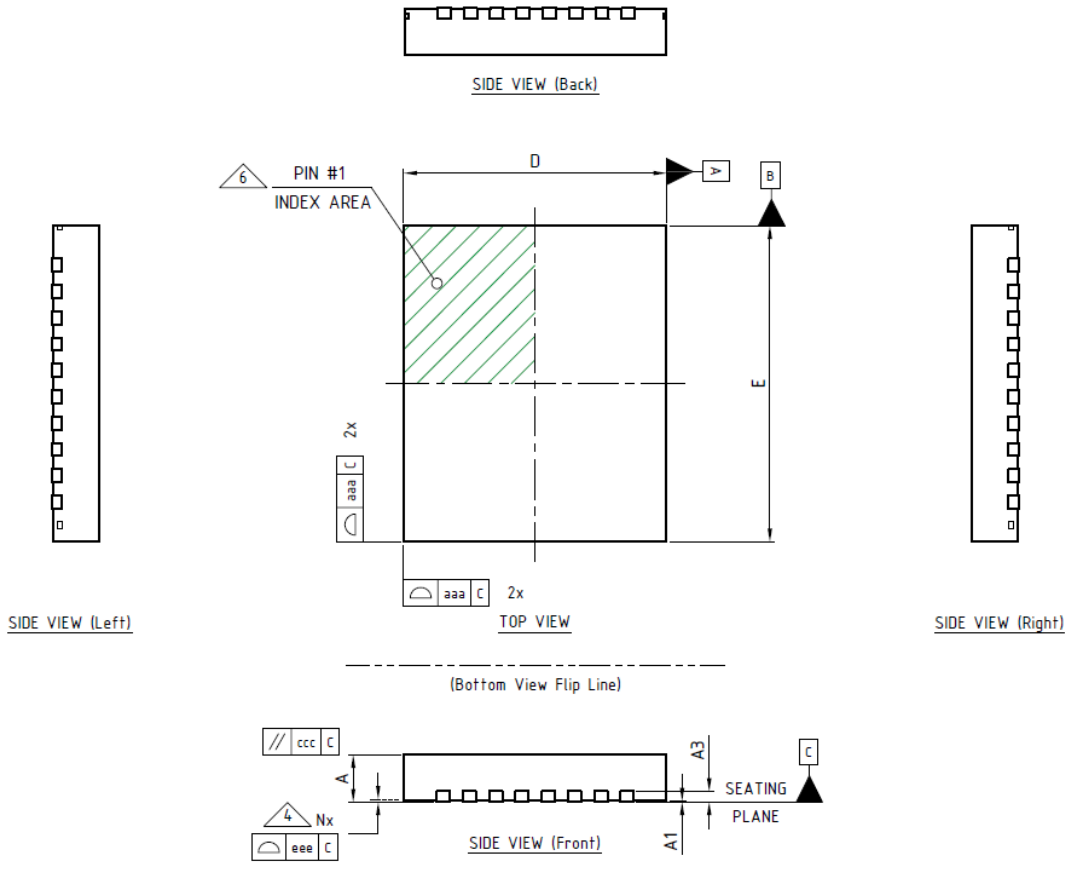
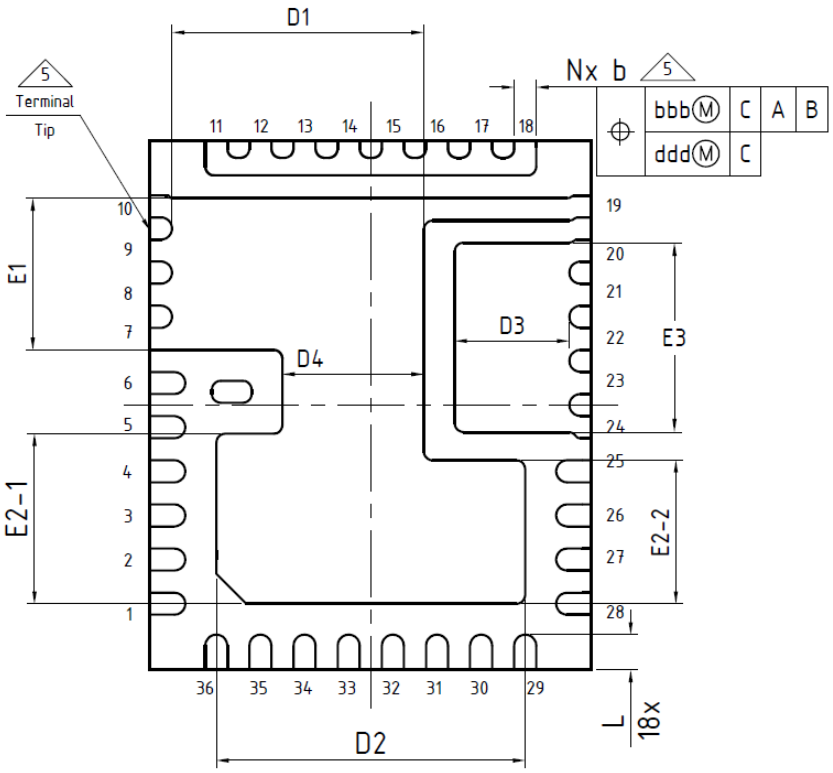



**Figure 37 Package Marking**

## 19.2 Dimensions



## Package




| Dimension Table | | | | |
|---|---|---|---|---|
| Thickness / Symbol | V | | | NOTE |
| | MINIMUM | NOMINAL | MAXIMUM | |
| A | 0.80 | 0.90 | 1.00 | |
| A1 | 0.00 | 0.02 | 0.05 | |
| A3 | --- | 0.20 Ref | --- | |
| b | 0.20 | 0.25 | 0.30 | 5 |
| D | 4.90 | 5.00 | 5.10 | |
| D1 | 2.750 | 2.850 | 2.950 | |
| D2 | 3.40 | 3.50 | 3.60 | |
| D3 | 1.199 | 1.299 | 1.399 | |
| D4 | 1.500 | 1.600 | 1.700 | |
| E | 5.90 | 6.00 | 6.10 | |
| E1 | 1.615 | 1.715 | 1.815 | |
| E2-1 | 1.825 | 1.925 | 2.025 | |
| E2-2 | 1.524 | 1.624 | 1.724 | |
| E3 | 2.045 | 2.145 | 2.245 | |
| L | 0.35 | 0.40 | 0.45 | |
| aaa | | 0.05 | | |
| bbb | 0.10 | | | |
| ccc | 0.10 | | | |
| ddd | 0.05 | | | |
| eee | 0.08 | | | |
| N | 36 | | | 3 |
| NOTES | 1, 2 | | | |
| LF PART NO. | T B A | | | |
| LF DWG. NO. | T B A | | | |

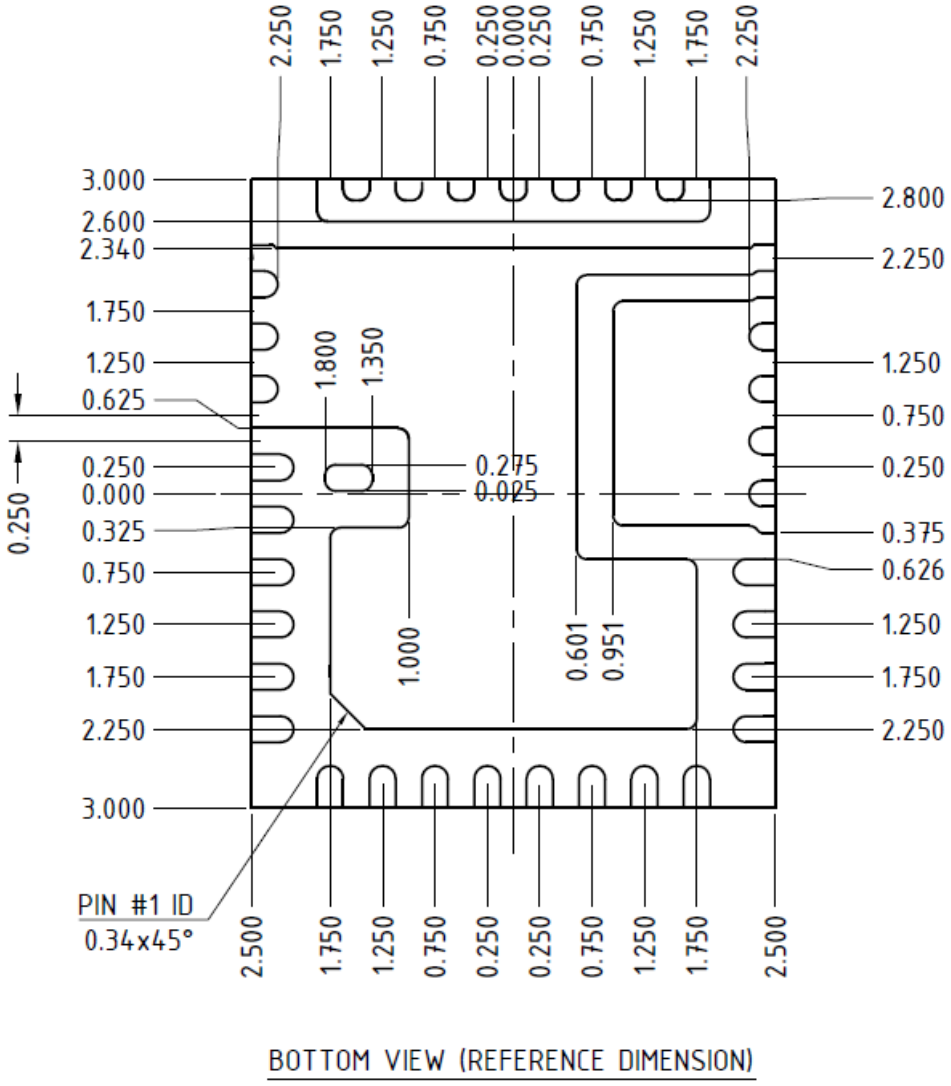



**Figure 38 Package Dimensions**

## 19.3 Tape and Reel Information

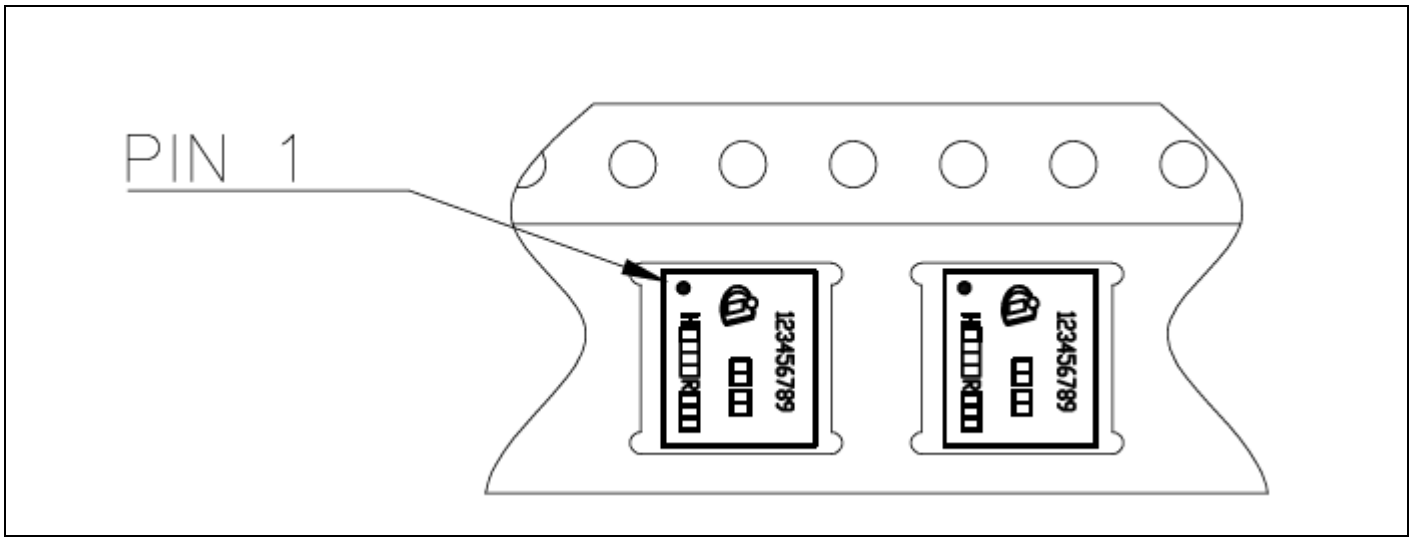



**Figure 39 Pin 1 Orientation in Tape & Reel**

# 20 Environmental Qualifications

**Table 18**

| Qualification Level | | Industrial | |
|---|---|---|---|
| **Moisture Sensitivity** | | 5 x 6 mm QFN Package | JEDEC Level 2 @ 260°C |
| **ESD** | **Human Body Model** | ANSI/ESDA/JEDEC JS-001, Class 2 (2000V to < 4000V) | |
| | **Charged Device Model** | ANSI/ESDA/JEDEC JS-002, Class C3 (≥ 1000V) | |
| **RoHS2 Compliant** | | Yes with exemption 7a | |

## Revision History

TDA38740/725

**Revision: 2022-05-13, Rev. 2.2**

| Previous Revision | | |
|---|---|---|
| Revision | Date | Subjects (major changes since last revision) |
| 2.0 | 2022-04-08 | Release of final version |
| 2.1 | 2022-04-13 | Updated the Abs max table with VIN-PH voltage |
| 2.2 | 2022-05-13 | Final datasheet revision - updated block diagram and EC table |



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