



## Product Change Notification / SYST-13CRBN870

---

### Date:

14-Feb-2024

### Product Category:

N-Channel Enhancement Mode Mosfets

### PCN Type:

Document Change

### Notification Subject:

Data Sheet - TN2640 Data Sheet

### Affected CPNs:

[SYST-13CRBN870\\_Affected\\_CPN\\_02142024.pdf](#)

[SYST-13CRBN870\\_Affected\\_CPN\\_02142024.csv](#)

### Notification Text:

SYST-13CRBN870

Microchip has released a new Datasheet for the TN2640 Data Sheet of devices. If you are using one of these devices please read the document located at [TN2640 Data Sheet](#).

**Notification Status:** Final

#### Description of Change:

- Updated Figure 2-9 in Section 2.0 "Typical Performance Curves".
- Updated package drawings in Section 5.0 "Packaging Information".

**Impacts to Data Sheet:** See above details.

**Reason for Change:** To Improve Productivity

**Change Implementation Status:** Complete

**Date Document Changes Effective:** 14 Feb 2024

**NOTE:** Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices::N/A

## Attachments:

[TN2640 Data Sheet](#)

Please contact your local [Microchip sales office](#) with questions or concerns regarding this notification.

## Terms and Conditions:

If you wish to receive Microchip PCNs via email please register for our PCN email service at our [PCN home page](#) select register then fill in the required fields. You will find instructions about registering for Microchips PCN email service in the [PCN FAQ](#) section.

If you wish to change your PCN profile, including opt out, please go to the [PCN home page](#) select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

Affected Catalog Part Numbers (CPN)

TN2640K4-G

TN2640LG-G

TN2640N3-G

## N-Channel Enhancement-Mode Vertical DMOS FET

### Features

- 2V Maximum Low Threshold
- High Input Impedance
- Low Input Capacitance
- Fast Switching Speeds
- Low On-Resistance
- Free from Secondary Breakdown
- Low Input and Output Leakage

### Applications

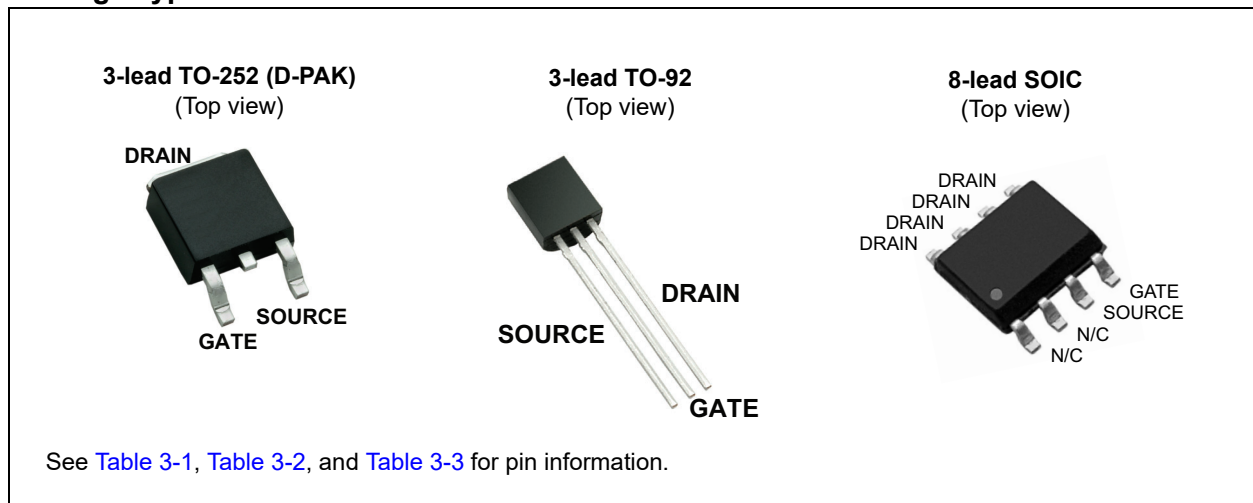
- Logic-Level Interfaces (Ideal for TTL and CMOS)
- Solid-State Relays
- Battery-Operated Systems
- Photovoltaic Drives
- Analog Switches
- General Purpose Line Drivers
- Telecommunication Switches

### General Description

The TN2640 low-threshold Enhancement-mode (normally-off) transistor uses a vertical DMOS structure and a well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Microchip's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Package Types



# TN2640

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings†

Drain-to-Source Voltage .....	$BV_{DSS}$
Drain-to-Gate Voltage .....	$BV_{DGS}$
Gate-to-Source Voltage .....	$\pm 20V$
Operating Ambient Temperature, $T_A$ .....	$-55^{\circ}C$ to $+150^{\circ}C$
Storage Temperature, $T_S$ .....	$-55^{\circ}C$ to $+150^{\circ}C$

† **Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

### DC ELECTRICAL CHARACTERISTICS

**Electrical Specifications:**  $T_A = 25^{\circ}C$  unless otherwise specified. All DC parameters are 100% tested at  $25^{\circ}C$  unless otherwise stated. (Pulse test: 300  $\mu s$  pulse, 2% duty cycle)

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	$BV_{DSS}$	400	—	—	V	$V_{GS} = 0V, I_D = 1 mA$
Gate Threshold Voltage	$V_{GS(th)}$	0.8	—	2	V	$V_{GS} = V_{DS}, I_D = 2 mA$
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	-2.5	-4	mV/ $^{\circ}C$	$V_{GS} = V_{DS}, I_D = 2 mA$ ( <b>Note 1</b> )
Gate Body Leakage Current	$I_{GSS}$	—	—	100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
Zero-Gate Voltage Drain Current	$I_{DSS}$	—	—	10	$\mu A$	$V_{GS} = 0V,$ $V_{DS} = \text{Maximum rating}$
		—	—	1	mA	$V_{DS} = 0.8$ Maximum rating, $V_{GS} = 0V, T_A = 125^{\circ}C$ ( <b>Note 1</b> )
On-State Drain Current	$I_{D(ON)}$	1.5	3.5	—	A	$V_{GS} = 5V, V_{DS} = 25V$
		2	4	—	A	$V_{GS} = 10V, V_{DS} = 25V$
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	3.2	5	$\Omega$	$V_{GS} = 4.5V, I_D = 500 mA$
		—	3	5	$\Omega$	$V_{GS} = 10V, I_D = 500 mA$
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	—	0.75	%/ $^{\circ}C$	$V_{GS} = 10V, I_D = 500 mA$ ( <b>Note 1</b> )

**Note 1:** Specification is obtained by characterization and is not 100% tested.

### AC ELECTRICAL CHARACTERISTICS

**Electrical Specifications:**  $T_A = 25^{\circ}C$  unless otherwise specified. All AC parameters are not 100% sample tested.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Forward Transconductance	$G_{FS}$	200	330	—	mmho	$V_{DS} = 25V, I_D = 100 mA$
Input Capacitance	$C_{ISS}$	—	210	225	pF	$V_{GS} = 0V, V_{DS} = 25V, f = 1 MHz$
Common-Source Output Capacitance	$C_{OSS}$	—	30	50	pF	
Reverse Transfer Capacitance	$C_{RSS}$	—	8	15	pF	
Turn-On Delay Time	$t_{d(ON)}$	—	4	15	ns	
Rise Time	$t_r$	—	15	20	ns	$V_{DD} = 25V, I_D = 2A, R_{GEN} = 25\Omega$
Turn-Off Delay Time	$t_{d(OFF)}$	—	20	25	ns	
Fall Time	$t_f$	—	22	27	ns	
<b>DIODE PARAMETER</b>						
Diode Forward Voltage Drop	$V_{SD}$	—	—	0.9	V	$V_{GS} = 0V, I_{SD} = 200 mA$ ( <b>Note 1</b> )
Reverse Recovery Time	$t_{rr}$	—	300	—	ns	$V_{GS} = 0V, I_{SD} = 1A$

**Note 1:** All DC parameters are 100% tested at  $25^{\circ}C$  unless otherwise stated.  
(Pulse test: 300  $\mu s$  pulse, 2% duty cycle)

## TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
<b>TEMPERATURE RANGE</b>						
Operating Ambient Temperature	$T_A$	-55	—	+150	°C	
Storage Temperature	$T_S$	-55	—	+150	°C	
<b>PACKAGE THERMAL RESISTANCE</b>						
3-lead TO-252 (D-PAK)	$\theta_{JA}$	—	81	—	°C/W	
8-lead SOIC	$\theta_{JA}$	—	101	—	°C/W	
3-lead TO-92	$\theta_{JA}$	—	132	—	°C/W	

## THERMAL CHARACTERISTICS

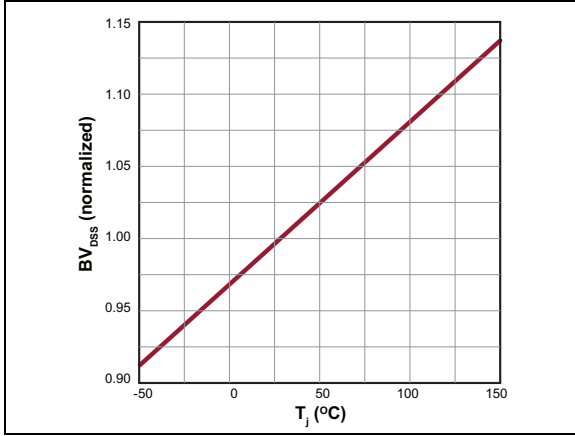
Package	$I_D$ (Note 1) (Continuous) (mA)	$I_D$ (Pulsed) (A)	Power Dissipation at $T_A = 25^\circ\text{C}$ (W)	$I_{DR}$ (Note 1) (mA)	$I_{DRM}$ (A)
3-lead TO-252 (D-PAK)	500	3	2.5 (Note 2)	500	3
8-lead SOIC	260	2	1.3 (Note 2)	260	2
3-lead TO-92	220	2	0.74	220	2

**Note 1:**  $I_D$  (continuous) is limited by maximum  $T_J$ .

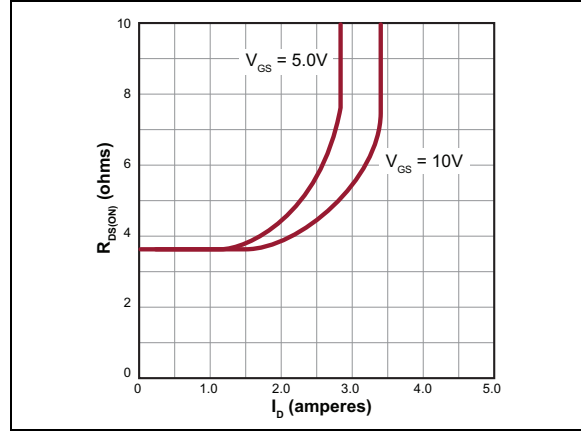
**2:** Mounted on an FR4 board, 25 mm x 25 mm x 1.57 mm

## 2.0 TYPICAL PERFORMANCE CURVES

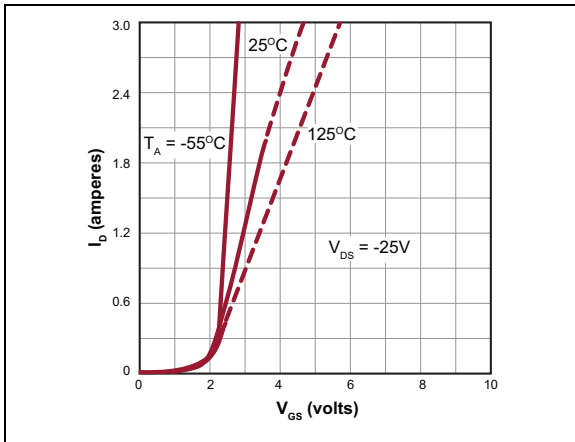
**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.



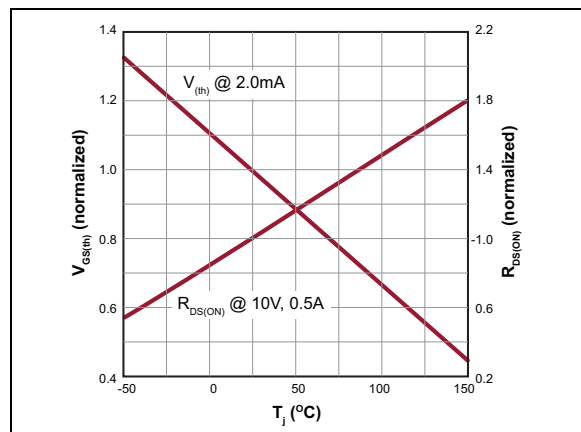
**FIGURE 2-1:**  $BV_{DSS}$  Variation with Temperature.



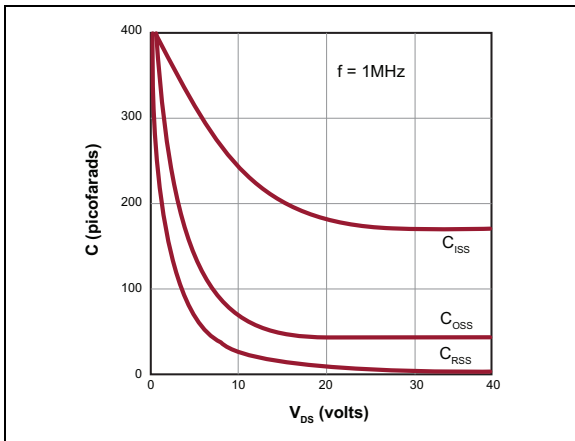
**FIGURE 2-4:** On-Resistance vs. Drain Current.



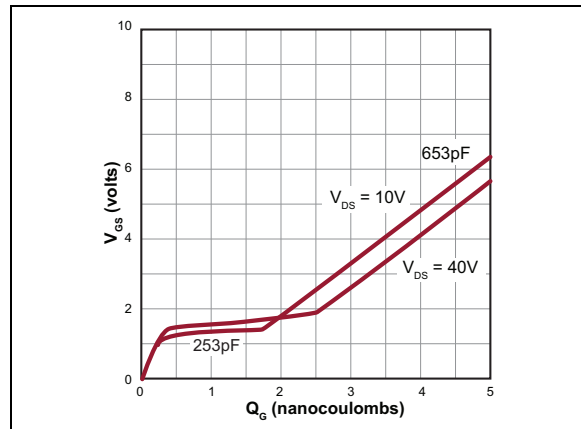
**FIGURE 2-2:** Transfer Characteristics.



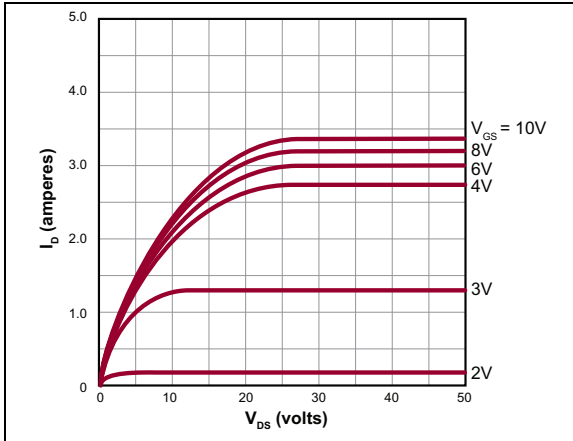
**FIGURE 2-5:**  $V_{GS(th)}$  and  $R_{DS(ON)}$  Variation with Temperature.



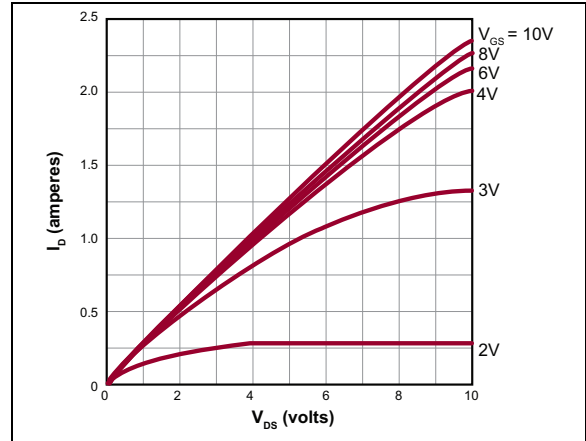
**FIGURE 2-3:** Capacitance vs. Drain-to-Source Voltage.



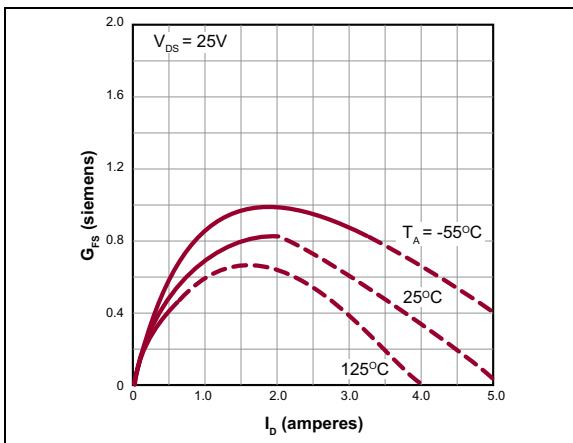
**FIGURE 2-6:**  $V_{GS(th)}$  and  $R_{DS(ON)}$  Variation with Temperature.



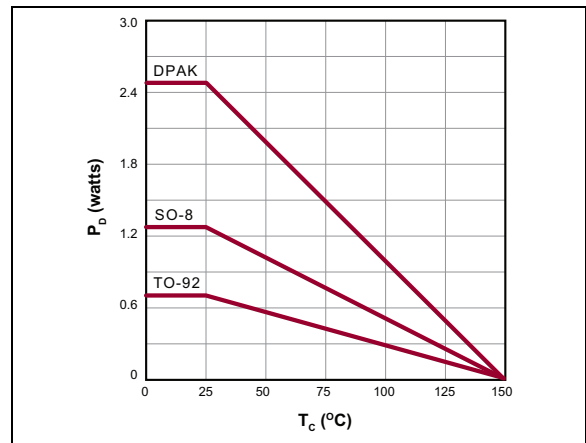
**FIGURE 2-7:** Output Characteristics.



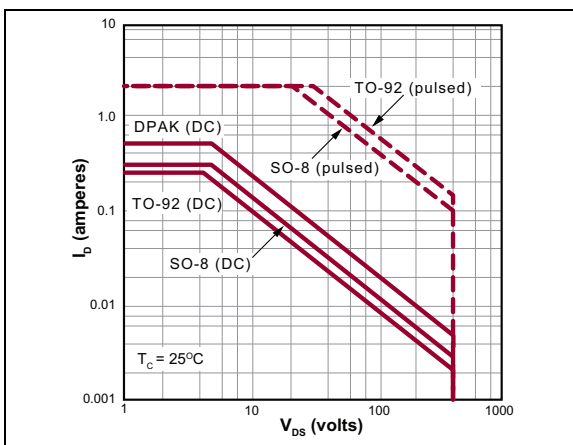
**FIGURE 2-10:** Saturation Characteristics.



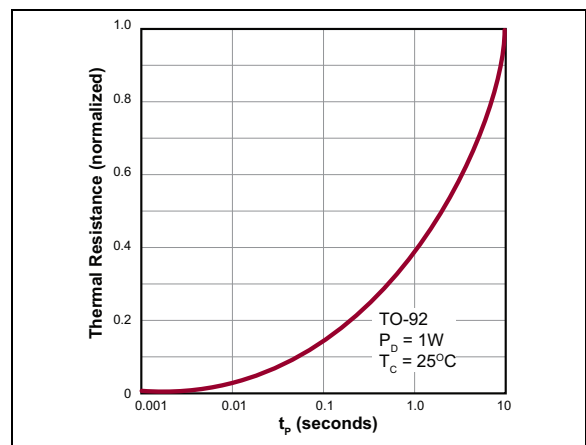
**FIGURE 2-8:** Transconductance vs. Drain Current.



**FIGURE 2-11:** Power Dissipation vs. Temperature.



**FIGURE 2-9:** Maximum Rated Safe Operating Area.



**FIGURE 2-12:** Thermal Characteristics.



# TN2640

---

---

## 3.0 PIN DESCRIPTION

Table 3-1, Table 3-2, and Table 3-3 show the description of pins in TN2640. Refer to [Package Types](#) for the location of the pins.

**TABLE 3-1: 3-LEAD TO-252 (DPAK) PIN FUNCTION TABLE**

Pin Number	Pin Name	Description
1	Gate	Gate
3	Source	Source
4	Drain	Drain

**TABLE 3-2: 8-LEAD SOIC PIN FUNCTION TABLE**

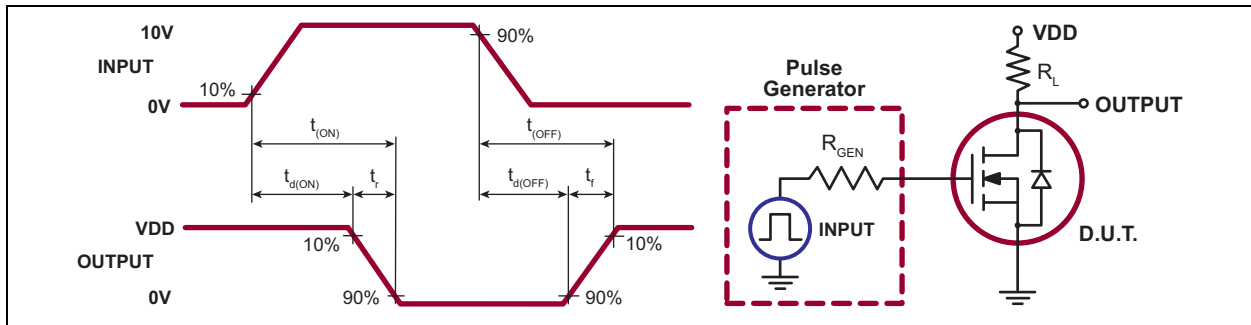
Pin Number	Pin Name	Description
1	N/C	No connect
2	N/C	No connect
3	Source	Source
4	Gate	Gate
5	Drain	Drain
6	Drain	Drain
7	Drain	Drain
8	Drain	Drain

**TABLE 3-3: 3-LEAD TO-92 PIN FUNCTION TABLE**

Pin Number	Pin Name	Description
1	Source	Source
2	Gate	Gate
3	Drain	Drain

## 4.0 FUNCTIONAL DESCRIPTION

Figure 4-1 illustrates the switching waveforms and test circuit for TN2640.



**FIGURE 4-1:** Switching Waveforms and Test Circuit.

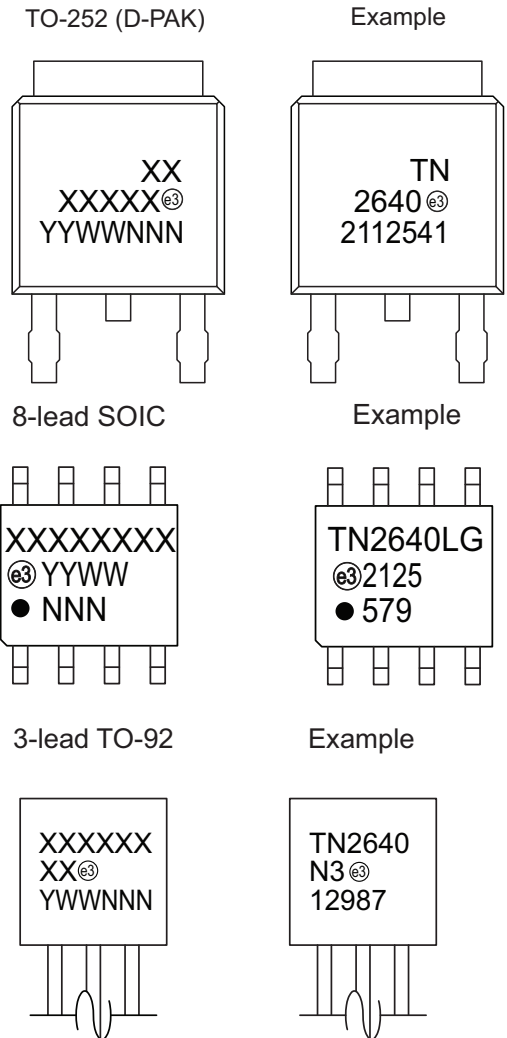
**TABLE 4-1: PRODUCT SUMMARY**

$BV_{DSS}/BV_{DGS}$ (V)	$R_{DS(ON)}$ (Maximum) ( $\Omega$ )	$I_{D(ON)}$ (Minimum) (A)	$V_{GS(th)}$ (Maximum) (V)
400	5	2	2

# TN2640

## 5.0 PACKAGING INFORMATION

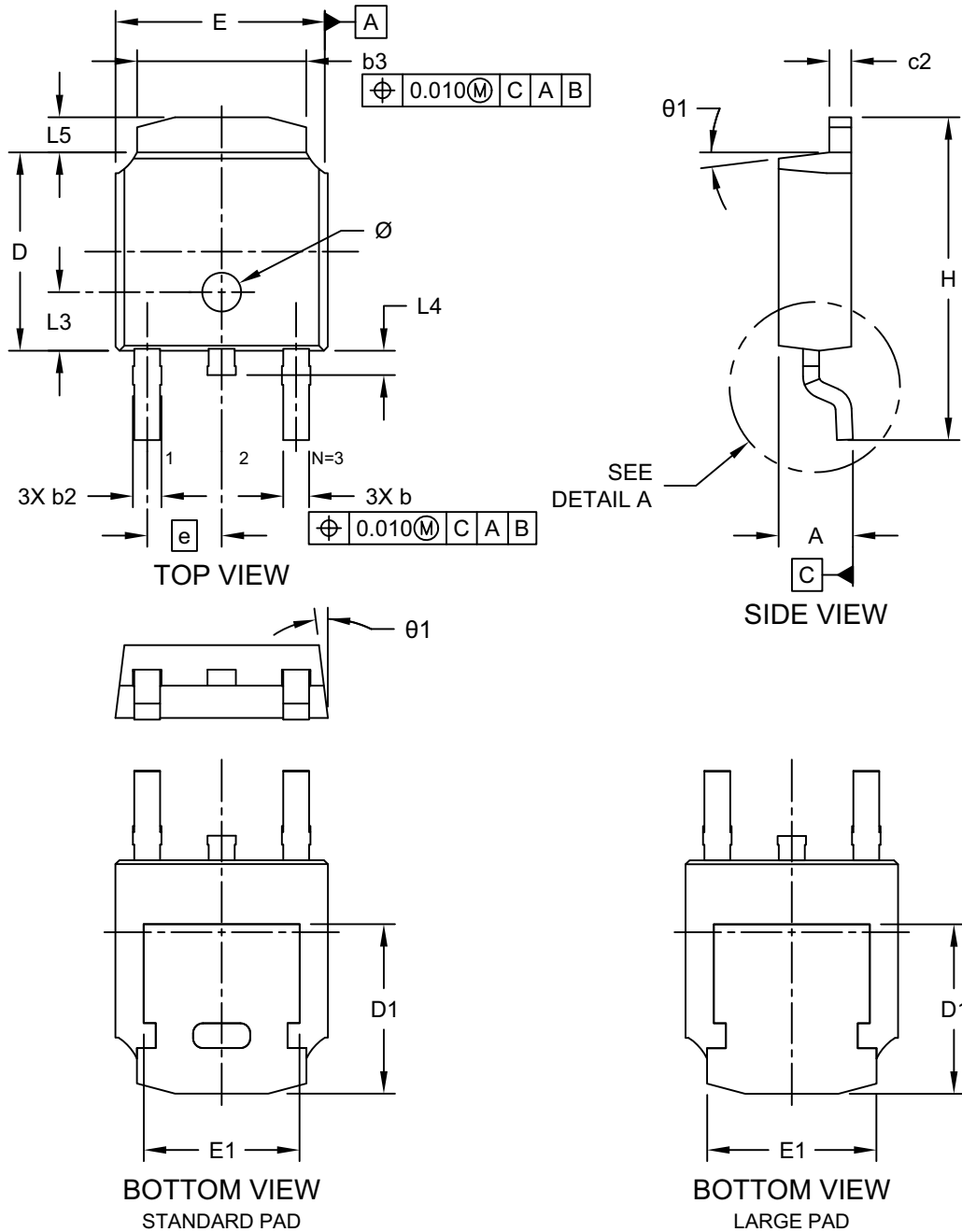
### 5.1 Package Marking Information



<b>Legend:</b>	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC <sup>®</sup> designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.	

## 3-Lead Deca-Watt Package, TO-252 (EA) - [DPAK]; Supertex Legacy Package Code K4

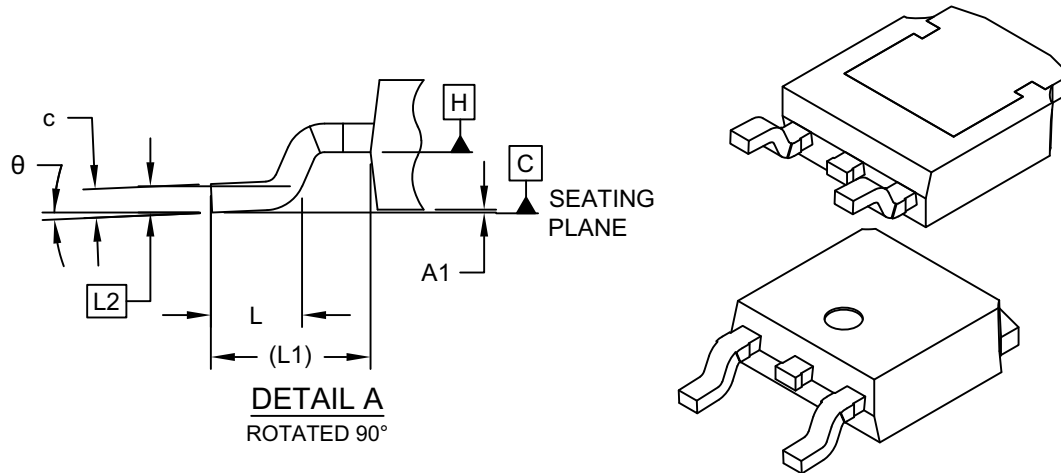
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



# TN2640

## 3-Lead Deca-Watt Package, TO-252 (EA) - [DPAK]; Supertex Legacy Package Code K4

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units	INCHES		
	MIN	NOM	MAX
N (Leads)	3		
e	.090 BSC		
A	.086	-	.094
A1	.000	-	.005
b	.028	-	.035
b2	.030	-	.045
c	.018	-	.024
c2	.018	-	.035
D	.235	.240	.245
D1	.205	-	-
E	.250	-	.265
E1	.170	-	-
H	.370	-	.410
L	.055	.060	.070
L1	.108 REF		
L2	.020 BSC		
L3	.065	-	.077
L4	.024	-	.035
L5	.035	-	.050
theta	1°	-	5°
theta1	7° REF		

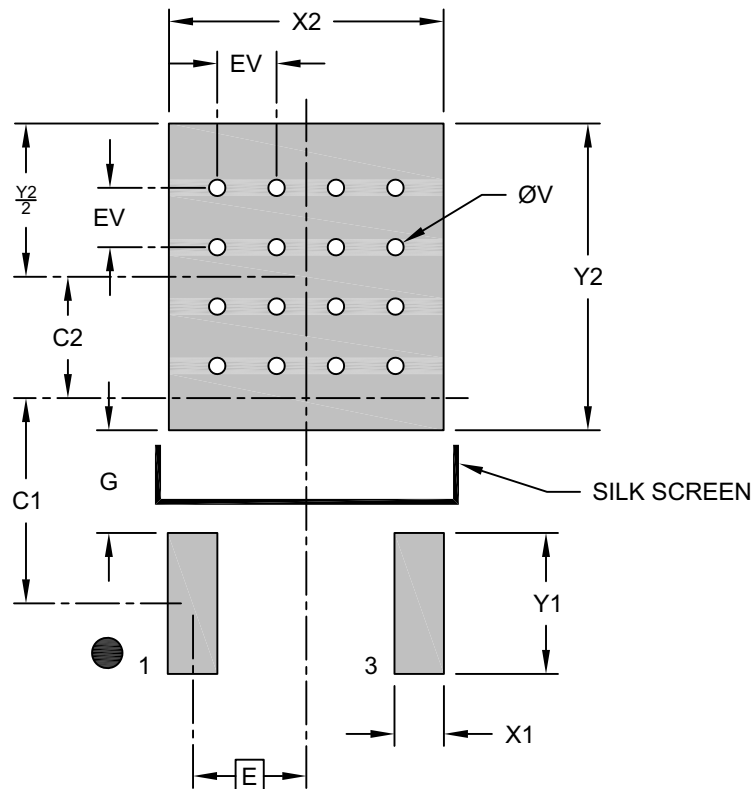
**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensioning and tolerancing per ASME Y14.5M  
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
 REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-189 Rev C Sheet 1 of 2

## 3-Lead Deca-Watt Package, TO-252 (EA) - [DPAK]; Supertex Legacy Package Code K4

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	INCHES		
		MIN	NOM	MAX
Contact Pitch	E	.090 BSC		
Center Pad Width	X2			.219
Center Pad Length	Y2			.244
Contact Pad Spacing	C1		.163	
Contact Pad Spacing	C2		.096	
Contact Pad Width (Xnn)	X1			.039
Contact Pad Length (Xnn)	Y1			.112
Contact Pad to Contact Pad (Xnn)	G	.412		
Thermal Via Diameter	V		.013	
Thermal Via Pitch	EV		.047	

Notes:

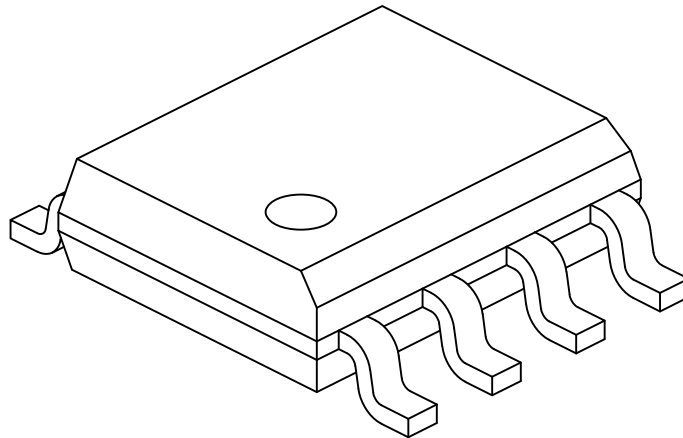
- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2189 Rev C



## 8-Lead Plastic Small Outline (C2X) - Narrow, 3.90 mm (.150 In.) Body [SOIC] Atmel Legacy Global Package Code SWB

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

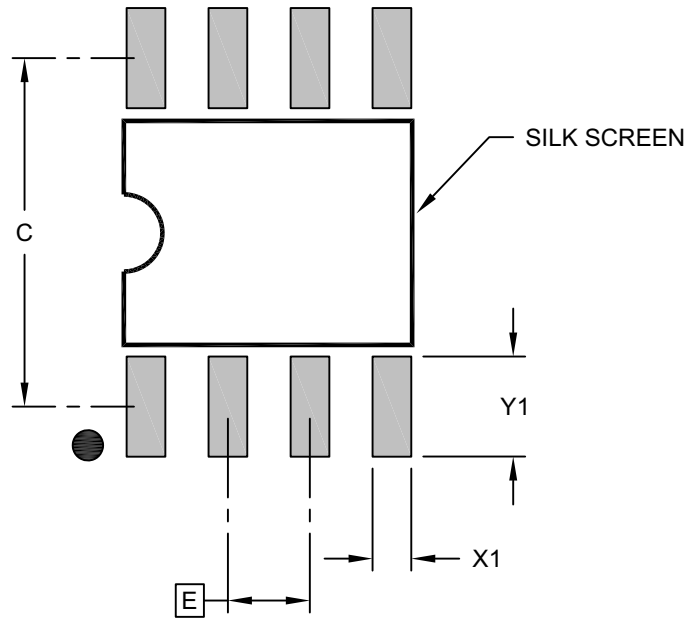
Microchip Technology Drawing No. C04-057-C2X Rev K Sheet 2 of 2



# TN2640

## 8-Lead Plastic Small Outline (C2X) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

**Notes:**

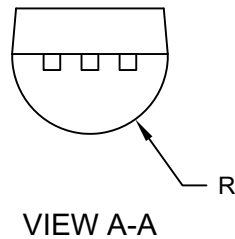
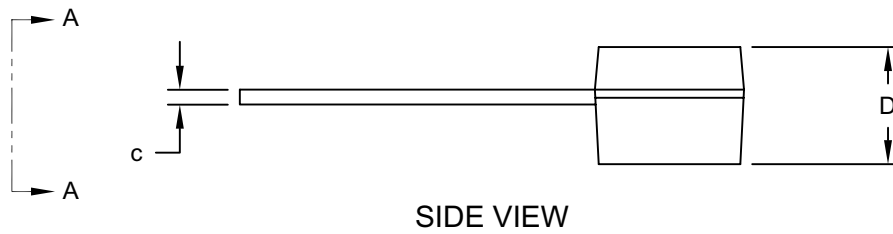
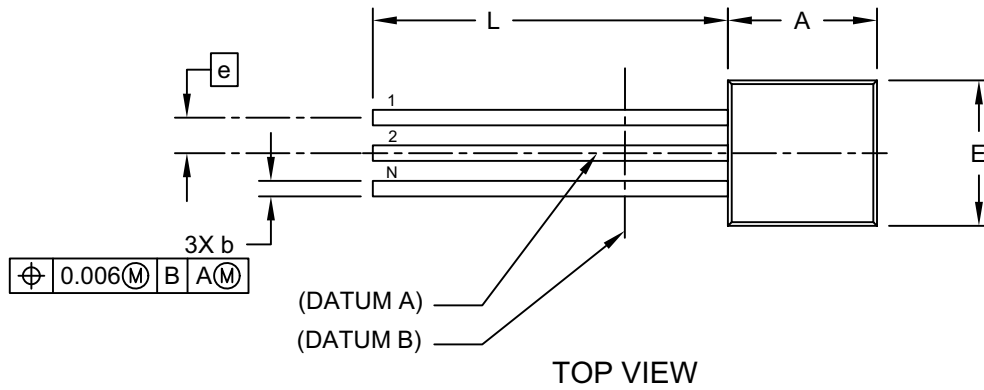
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-C2X Rev K

## 3-Lead Plastic Transistor Outline (TO) [TO-92]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

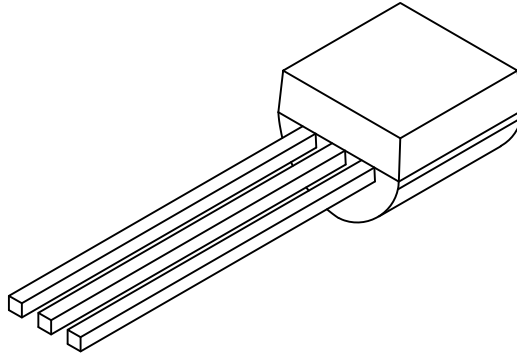


Microchip Technology Drawing C04-101-TO Rev D Sheet 1 of 2

# TN2640

## 3-Lead Plastic Transistor Outline (TO) [TO-92]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES		
		MIN	NOM	MAX
Number of Pins	N	3		
Pitch	e	.050 BSC		
Bottom to Package Flat	D	.125	-	.165
Overall Width	E	.175	-	.205
Overall Length	A	.170	-	.210
Molded Package Radius	R	.080	-	.105
Tip to Seating Plane	L	.500	-	-
Lead Thickness	c	.014	-	.021
Lead Width	b	.014	-	.022

**Notes:**

1. Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" per side.
2. Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-101-TO Rev D Sheet 2 of 2

## APPENDIX A: REVISION HISTORY

### Revision B (February 2024)

- Updated [Figure 2-9](#) in [Section 2.0 “Typical Performance Curves”](#).
- Updated package drawings in [Section 5.0 “Packaging Information”](#).

### Revision A (February 2021)

- Converted Supertex Doc# DSFP-TN2640 to Microchip DS20005795A.
- Changed the package marking format.
- Updated the quantity of the 8-lead SOIC from 2500/Reel to 3300/Reel to align it with the actual BQM.
- Removed the TO-92 N3 P002, P003, P005, P013, and P015 media types to align package specifications with the actual BQM.
- Made minor text changes throughout the document.

# TN2640

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>		<u>XX</u>	-	<u>X</u>	-	<u>X</u>
Device	Package Options			Environmental		Media Type
Device:	TN2640	=		N-Channel Enhancement-Mode Vertical DMOS FET		
Packages:	K4	=		3-lead TO-252 (D-PAK)		
	LG	=		8-lead SOIC		
	N3	=		3-lead TO-92		
Environmental:	G	=		Lead (Pb)-free/RoHS-compliant Package		
Media Types:	(blank)	=		2000/Reel for a K4 Package		
		=		3300/Reel for an LG Package		
		=		1000/Bag for an N3 Package		

Examples:	
a) TN2640K4-G:	N-Channel Enhancement-Mode Vertical DMOS FET, 3-lead TO-252 (D-PAK), 2000/Reel
b) TN2640LG-G:	N-Channel Enhancement-Mode Vertical DMOS FET, 8-lead SOIC, 3300/Reel
c) TN2640N3-G:	N-Channel Enhancement-Mode Vertical DMOS FET, 3-lead TO-92, 1000/Bag

---

---

**Note the following details of the code protection feature on Microchip products:**

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable" Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

---

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at <https://www.microchip.com/en-us/support/design-help/client-support-services>.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

For information regarding Microchip's Quality Management Systems, please visit [www.microchip.com/quality](http://www.microchip.com/quality).

**Trademarks**

The Microchip name and logo, the Microchip logo, Adaptec, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, CryptoMemory, CryptoRF, dsPIC, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, ClockWorks, The Embedded Control Solutions Company, EtherSynch, Flashtec, Hyper Speed Control, HyperLight Load, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet-Wire, SmartFusion, SyncWorld, TimeCesium, TimeHub, TimePictra, TimeProvider, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, Clockstudio, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, Espresso T1S, EtherGREEN, EyeOpen, GridTime, IdealBridge, IGA, In-Circuit Serial Programming, ICSP, INICnet, Intelligent Paralleling, IntelliMOS, Inter-Chip Connectivity, JitterBlocker, Knob-on-Display, MarginLink, maxCrypto, maxView, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, mSiC, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, Power MOS IV, Power MOS 7, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, RTAX, RTG4, SAM-ICE, Serial Quad I/O, simpleMAP, SimpliPHY, SmartBuffer, SmartHLS, SMART-I.S., storClad, SQL, SuperSwitcher, SuperSwitcher II, Switchtec, SynchroPHY, Total Endurance, Trusted Time, TSHARC, Turing, USBCheck, VariSense, VectorBlox, VeriPHY, ViewSpan, WiperLock, XpressConnect, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, and Symmcom are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2024, Microchip Technology Incorporated and its subsidiaries.

All Rights Reserved.

ISBN: 978-1-6683-4038-7



# MICROCHIP

## Worldwide Sales and Service

### AMERICAS

**Corporate Office**  
2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200  
Fax: 480-792-7277  
Technical Support:  
<http://www.microchip.com/support>  
Web Address:  
[www.microchip.com](http://www.microchip.com)

#### Atlanta

Duluth, GA  
Tel: 678-957-9614  
Fax: 678-957-1455

#### Austin, TX

Tel: 512-257-3370

#### Boston

Westborough, MA  
Tel: 774-760-0087  
Fax: 774-760-0088

#### Chicago

Itasca, IL  
Tel: 630-285-0071  
Fax: 630-285-0075

#### Dallas

Addison, TX  
Tel: 972-818-7423  
Fax: 972-818-2924

#### Detroit

Novi, MI  
Tel: 248-848-4000

#### Houston, TX

Tel: 281-894-5983

#### Indianapolis

Noblesville, IN  
Tel: 317-773-8323  
Fax: 317-773-5453  
Tel: 317-536-2380

#### Los Angeles

Mission Viejo, CA  
Tel: 949-462-9523  
Fax: 949-462-9608  
Tel: 951-273-7800

#### Raleigh, NC

Tel: 919-844-7510

#### New York, NY

Tel: 631-435-6000

#### San Jose, CA

Tel: 408-735-9110  
Tel: 408-436-4270

#### Canada - Toronto

Tel: 905-695-1980  
Fax: 905-695-2078

### ASIA/PACIFIC

**Australia - Sydney**  
Tel: 61-2-9868-6733

**China - Beijing**  
Tel: 86-10-8569-7000

**China - Chengdu**  
Tel: 86-28-8665-5511

**China - Chongqing**  
Tel: 86-23-8980-9588

**China - Dongguan**  
Tel: 86-769-8702-9880

**China - Guangzhou**  
Tel: 86-20-8755-8029

**China - Hangzhou**  
Tel: 86-571-8792-8115

**China - Hong Kong SAR**  
Tel: 852-2943-5100

**China - Nanjing**  
Tel: 86-25-8473-2460

**China - Qingdao**  
Tel: 86-532-8502-7355

**China - Shanghai**  
Tel: 86-21-3326-8000

**China - Shenyang**  
Tel: 86-24-2334-2829

**China - Shenzhen**  
Tel: 86-755-8864-2200

**China - Suzhou**  
Tel: 86-186-6233-1526

**China - Wuhan**  
Tel: 86-27-5980-5300

**China - Xian**  
Tel: 86-29-8833-7252

**China - Xiamen**  
Tel: 86-592-2388138

**China - Zhuhai**  
Tel: 86-756-3210040

### ASIA/PACIFIC

**India - Bangalore**  
Tel: 91-80-3090-4444

**India - New Delhi**  
Tel: 91-11-4160-8631

**India - Pune**  
Tel: 91-20-4121-0141

**Japan - Osaka**  
Tel: 81-6-6152-7160

**Japan - Tokyo**  
Tel: 81-3-6880-3770

**Korea - Daegu**  
Tel: 82-53-744-4301

**Korea - Seoul**  
Tel: 82-2-554-7200

**Malaysia - Kuala Lumpur**  
Tel: 60-3-7651-7906

**Malaysia - Penang**  
Tel: 60-4-227-8870

**Philippines - Manila**  
Tel: 63-2-634-9065

**Singapore**  
Tel: 65-6334-8870

**Taiwan - Hsin Chu**  
Tel: 886-3-577-8366

**Taiwan - Kaohsiung**  
Tel: 886-7-213-7830

**Taiwan - Taipei**  
Tel: 886-2-2508-8600

**Thailand - Bangkok**  
Tel: 66-2-694-1351

**Vietnam - Ho Chi Minh**  
Tel: 84-28-5448-2100

### EUROPE

**Austria - Wels**  
Tel: 43-7242-2244-39  
Fax: 43-7242-2244-393

**Denmark - Copenhagen**  
Tel: 45-4485-5910  
Fax: 45-4485-2829

**Finland - Espoo**  
Tel: 358-9-4520-820

**France - Paris**  
Tel: 33-1-69-53-63-20  
Fax: 33-1-69-30-90-79

**Germany - Garching**  
Tel: 49-8931-9700

**Germany - Haan**  
Tel: 49-2129-3766400

**Germany - Heilbronn**  
Tel: 49-7131-72400

**Germany - Karlsruhe**  
Tel: 49-721-625370

**Germany - Munich**  
Tel: 49-89-627-144-0  
Fax: 49-89-627-144-44

**Germany - Rosenheim**  
Tel: 49-8031-354-560

**Israel - Ra'anana**  
Tel: 972-9-744-7705

**Italy - Milan**  
Tel: 39-0331-742611  
Fax: 39-0331-466781

**Italy - Padova**  
Tel: 39-049-7625286

**Netherlands - Drunen**  
Tel: 31-416-690399  
Fax: 31-416-690340

**Norway - Trondheim**  
Tel: 47-7288-4388

**Poland - Warsaw**  
Tel: 48-22-3325737

**Romania - Bucharest**  
Tel: 40-21-407-87-50

**Spain - Madrid**  
Tel: 34-91-708-08-90  
Fax: 34-91-708-08-91

**Sweden - Gothenberg**  
Tel: 46-31-704-60-40

**Sweden - Stockholm**  
Tel: 46-8-5090-4654

**UK - Wokingham**  
Tel: 44-118-921-5800  
Fax: 44-118-921-5820