The Future of Analog IC Technology®

MP8864

High-Efficiency, 4 A, 21 V, Synchronous Step-Down Converter with I^2C Interface

DESCRIPTION

The MP8864 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with an I^2C control interface. It offers a very compact solution to achieve a 4 A continuous output current with excellent load and line regulation over a wide input supply range. The MP8864 has synchronous-mode operation for higher efficiency over the output load range.

The reference voltage level is controlled, on-the-fly through a 3.4 Mbps I^2C serial interface. The voltage range can be adjusted from 0.6 V to 1.87 V in 10 mV steps. Also, the voltage slew rate, switching frequency, enable, and power-saving mode are selectable through the I^2C interface.

Current-mode operation provides fast transient response and eases loop stabilization. Full protection features include over-current protection (OCP), over-voltage protection (OVP), and thermal shutdown (TSD).

The MP8864 requires a minimal number of readily available, standard external components and is available in a 15-pin QFN15 (3mm x 3mm) package.

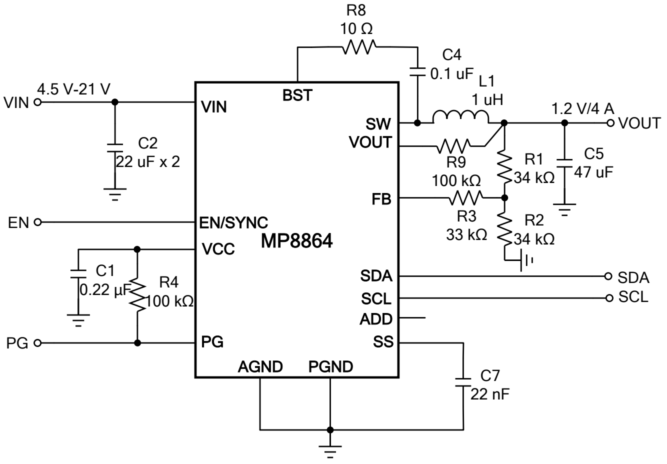
FEATURES

- Wide 4.5 V to 21 V Operation Input Range
- 50 mΩ/23 mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- 1% VOUT Accuracy
- I^2C Programmable Reference Voltage Range from 0.6 V to 1.87 V in 10 mV Steps with Slew-Rate Control
- I^2C Selectable Switching Frequency. Default 600 kHz Switching Frequency
- Programmable Output Voltage
- Power-Saving Mode, OTP, and OCP via I^2C
- Power Good Indication
- 1-Bit I^2C Address Set Pin
- OCP in Hiccup Mode
- External Soft-Start
- Available in a QFN 3mm x 3mm Package

APPLICATIONS

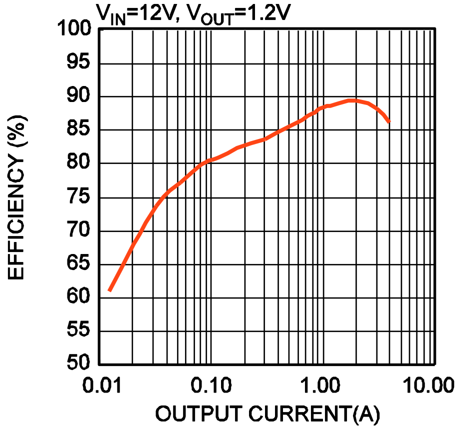
- SoC and Media Processors
- General Consumer
- Distributed Power Systems

TYPICAL APPLICATION



Efficiency vs. Output Current

V_{IN}=12V, V_{OUT}=1.2V



ORDERING INFORMATION

Part Number	Package	Top Marking
MP8864GQ*****	QFN-15 (3mm x 3mm)	*See Below*
EVKT-8864	Evaluation Kit	

*****For Tape & Reel, add suffix –Z (e.g. MP8864GQ–Z);

TOP MARKING

APEY

LLL

APE: Product code of MP8864GQ
Y: Year code
LLL: Lot number

EVALUATION KIT EVKT-8864

EVKT-8864 Kit contents: (Items below can be ordered separately).

#	Part Number	Item	Quantity
1	EV8864-Q-00A	MP8864GQ evaluation board	1
2	EVKT-USBI2C-02	Includes one USB to I2C dongle, one USB cable, and one ribbon cable	1
3	Tdrive-8864	USB Flash drive that stores the GUI installation file and supplemental documents	1

Order direct from MonolithicPower.com or our distributors.

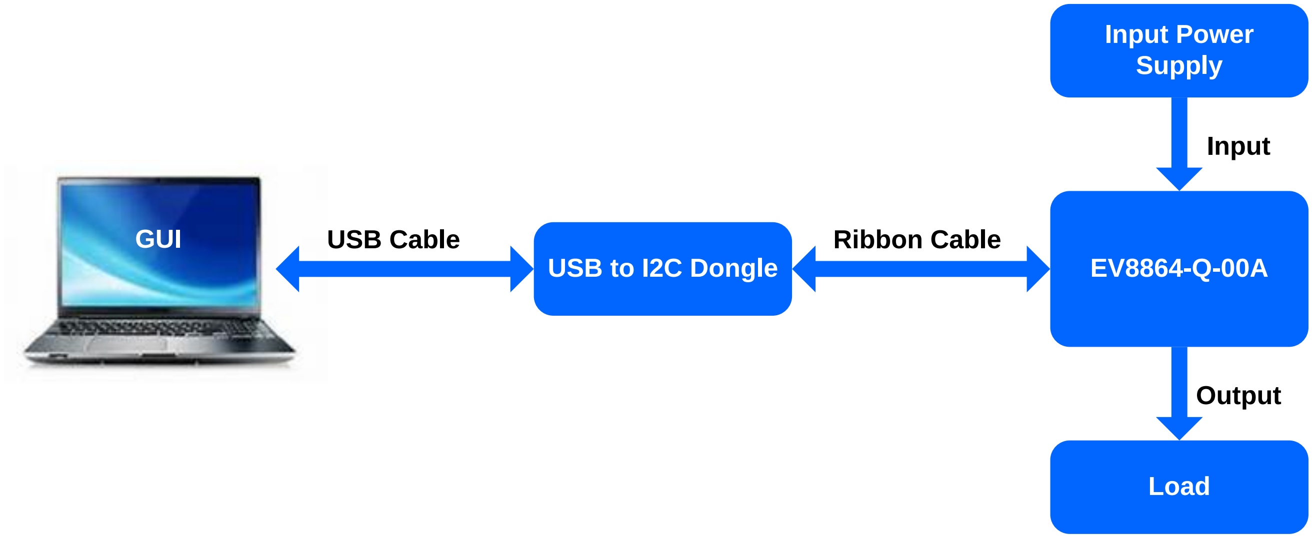
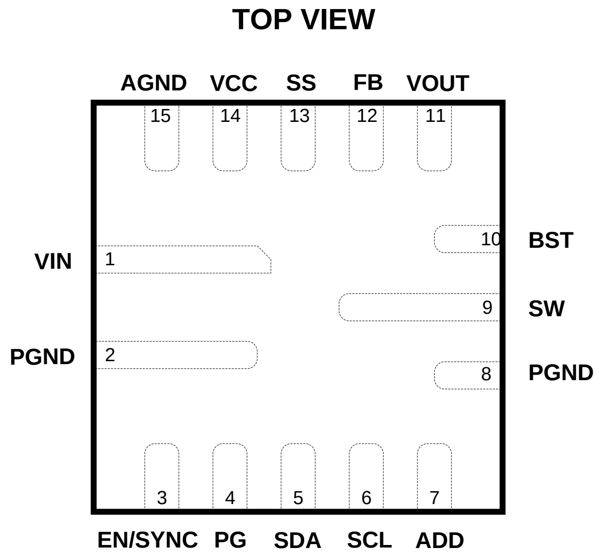


Figure 1: EVKT-8864 Evaluation Kit Set-Up

PACKAGE REFERENCE



QFN-15 (3mm x 3mm)

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} …………………………….. ......-0.3 V to 22 V
V_{SW}……………………………….-0.3 V(-5 V for <10 ns) to V_{IN}+0.3 V (27 V for <25 ns)
V_{BST} ……………………………. V_{SW}+5.5 V
All other pins………………...... -0.3 V to 5.4 V (2)
Continuous power dissipation (T_A = +25°C) (3)
………………………………………………2.5 W
Junction temperature…………………….150°C
Lead temperature…………………………260°C
Storage temperature……………-65°C to 150°C

Recommended Operating Conditions (4)

Supply voltage (V_{IN})………………4.5V to 21 V
Output voltage (V_{OUT})……………………………
……………………0.6 V to V_{IN} x D_{MAX} or 5.2 V (5)
Operating junction temp. (T_J)… -40°C to +125°C

Thermal Resistance (6) θ_{JA} θ_{JC}

QFN-15 (3mm x 3mm)…..…. …50…12…°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) For additional details on EN's absolute max. rating, please refer to the "EN/SYNC Control" section on page 15.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) The output voltage cannot exceed the 5.2 V absolute maximum value at any input condition.
6) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} =12 V, T_J = -40°C to 125°C (7), unless otherwise noted, the typical value is based on the average value when T_J=25ºC.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0 V, T_J=25°C			5	μA
Supply current (quiescent)	I_q	V_{EN} = 2 V, No switching, PFM mode		500	760	μA
HS switch-on resistance	HS_{RDS-ON}	V_{BST-SW}=5 V		50		mΩ
LS switch-on resistance	LS_{RDS-ON}	V_{CC} =5 V		23		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0 V, V_{SW} =12 V			1	μA
Current limit (8)	I_{LIMIT}	Under 40% Duty cycle	5.5	7.5		A
Default oscillator frequency	f_{SW}	V_{FB}=500 mV	480	600	680	kHz
Foldback frequency	f_{FB}	V_{FB}=250 mV		0.5		f_{SW}
Maximum duty cycle	D_{MAX}	V_{FB}=500 mV	90	95		%
Minimum on time(8)	t_{ON_MIN}			60		ns
Feedback voltage	V_{REF}	T_J =25°C	594	600	606	mV
	V_{REF}	T_J = -40°C to 125°C	588	600	612	mV
VOUT	V_{OUT}=1.2 V	T_J = 25°C	1188	1200	1212	mV
	V_{OUT}=1.2 V	T_J = -40°C to 125°C	1182	1200	1218	mV
FB current	I_{OUT}	V_{FB}=620 mV		10	50	nA
EN rising threshold	V_{EN_Rise}		1.2	1.4	1.6	V
EN hysteresis	V_{EN_HYS}			150		mV
EN input current	I_{EN}	V_{EN}=2 V		2		μA
SYNC frequency range	f_{SYNC}		0.3		2	MHz
ADD high level	V_{ADD_H}		2			V
ADD low level	V_{ADD_L}				0.4	V
VIN under-voltage lockout threshold-rising	$INUV_{Vth}$		3.8	4	4.25	V
VIN under-voltage lockout threshold-hysteresis	$INUV_{HYS}$			600		mV
VCC regulator	V_{CC}			5		V
VCC load regulation		I_{CC}=5 mA		1.5		%
Power good threshold rising	PGV_{th-Hi}	V_{REF}=600 mV		0.9		VOUT
Power good threshold falling	PGV_{th-Lo}	V_{REF}=600 mV		0.7		VOUT
Power good deglitch time (8)	PG_{Td}			80		μs
Soft-start current	I_{SS}		6	12	18	μA
Thermal shutdown (8)	T_{TSD}			160		°C
Thermal hysteresis (8)	T_{TSD_HYS}			20		°C
DAC resolution(8)	DAC			7		bits

NOTES:

7) Not tested in production and guaranteed by over-temperature correlation.

8) Guaranteed by design and characterization test.

I/O Level Characteristics [(9)]

Parameter	Symbol	Condition	HS Mode		LS Mode		Units
			Min	Max	Min	Max	
Low-level input voltage	V_{IL}		-0.5	0.3 V_{Bus}	-0.5	0.3 V_{Bus}	V
High-level input voltage	V_{IH}		0.7 V_{Bus}	V_{Bus}+0.5	0.7 V_{Bus}	V_{Bus}+0.5	V
Hysteresis of Schmitt trigger inputs	V_{HYS}	V_{Bus}>2 V	0.05 V_{Bus}	-	0.05 V_{Bus}	-	V
		V_{Bus}<2 V	0.1 V_{Bus}	-	0.1 V_{Bus}	-	
Low-level output voltage (open drain) at 3 mA sink current	V_{OL}	V_{Bus}>2 V	0	0.4	0	0.4	V
		V_{Bus}<2 V	0	0.2 V_{Bus}	0	0.2 V_{Bus}	
Low-level output current	I_{OL}		-	3	-	3	mA
Transfer gate-on resistance for currents between SDA and SCAH, or SCL and SCLH	R_{onL}	VOL level, IOL= 3 mA	-	50	-	50	Ω
Transfer gate-on resistance between SDA and SCAH, or SCL and SCLH	R_{onH}	Both signals (SDA and SDAH, or SCL and SCLH) at V_{Bus} level	50	-	50	-	kΩ
Pull-up current of the SCLH current source	I_{cs}	SCLH output levels between 0.3 V_{Bus} and 0.7 V_{Bus}	2	6	2	6	mA
Rise time of the SCLH or SCL signal	t_{rCL}	Output rise time (current source enabled) with an external pull-up current source of 3 mA					
		Capacitive load from 10 pF to 100 pF	10	40			ns
		Capacitive load of 400 pF	20	80			ns
Fall time of the SCLH or SCL signal	t_{fCL}	Output fall time (current source enabled) with an external pull-up current source of 3 mA					
		Capacitive load from 10 pF to 100 pF	10	40			ns
		Capacitive load of 400 pF	20	80	20	250	ns

I/O Level Characteristics *(continued)*

Parameter	Symbol	Condition	HS Mode		LS Mode		Units
			Min	Max	Min	Max	
Rise time of SDAH signal	t_{rDA}	Capacitive load from 10 pF to 100 pF	10	80	-	-	ns
		Capacitive load of 400 pF	20	160	20	250	ns
Fall time of SDAH signal	t_{fDA}	Capacitive load from 10 pF to 100 pF	10	80	-	-	ns
		Capacitive load of 400 pF	20	160	20	250	ns
Pulse width of spikes that must be suppressed by the input filter	t_{SP}		0	10	0	50	ns
Input current for each I/O	I_i	Input voltage between 0.1 V_{Bus} and 0.9 V_{Bus}	-	10	-10	+10	μA
Capacitance for each I/O	C_i		-	10	-	10	pF

I²C Port Signal Characteristics

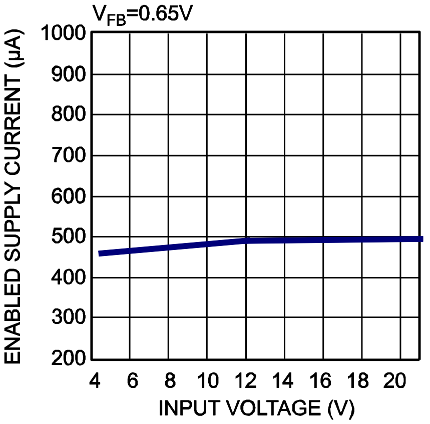
Parameter	Symbol	Condition	Cb=100 pF		Cb=400 pF		Units
			Min	**Max**	**Min**	**Max**	
SCLH and SCL clock frequency	f_{SCHL}		0	3.4	0	0.4	MHz
Set-up time for a repeated start condition	$T_{SU;STA}$		160	-	600	-	ns
Hold time (repeated) start condition	$T_{HD;STA}$		160	-	600	-	ns
Low period of the SCL clock	t_{LOW}		160	-	1300	-	ns
High period of the SCL clock	t_{HIGH}		60	-	600	-	ns
Data set-up time	$T_{SU:DAT}$		10	-	100	-	ns
Data hold time	$T_{HD;DAT}$		0	70	0	-	ns
Rise time of SCLH signal	t_{rCL}		10	40	20*0.1Cb	300	ns
Rise time of SCLH signal after a repeated start condition and after an acknowledge bit	t_{fCL1}		10	80	20*0.1Cb	300	ns
Fall time of SCLH signal	T_{fCL}		10	40	20*0.1Cb	300	ns
Rise time of SDAH signal	t_{fDA}		10	80	20*0.1Cb	300	ns
Fall time of SDAH signal	T_{fDA}		10	80	20*0.1Cb	300	ns
Set-up time for stop condition	$T_{SU;STO}$		160	-	600	-	ns
Bus free time between a start and stop condition	T_{BUF}		160	-	1300	-	ns
Data valid time	$T_{VD;DAT}$		-	16	-	90	ns
Data valid acknowledge time	$T_{VD;ACK}$		-	160	-	900	ns
Capacitive load for each bus line	C_b	SDAH and SCLH line	-	100	-	400	pF
		SDAH+SDA line and SCLH+SCL line	-	400	-	400	pF
Noise margin at the low level	C_i	For each connected device	-	0.1V_{Bus}	0.1 V_{Bus}	-	V
Noise margin at the high level	V_{nH}	For each connected device	-	0.2V_{Bus}	0.2 V_{Bus}	-	V

Notes:

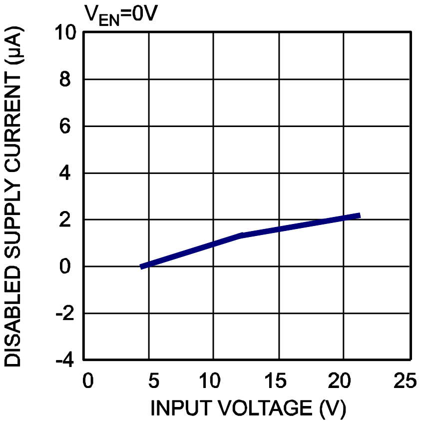
9) VBUS is the I²C bus voltage, 3.0 V to 3.6 V range, 3.3 V typical.

TYPICAL CHARACTERISTICS

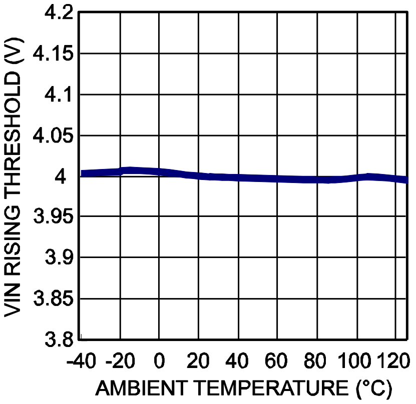
V_{IN} = 12 V, V_{OUT} = 1.2 V, L = 1 µH, T_A = 25°C, unless otherwise noted.



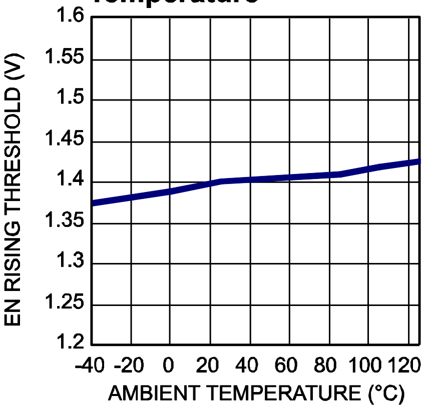
Enabled Supply Current vs. Input Voltage



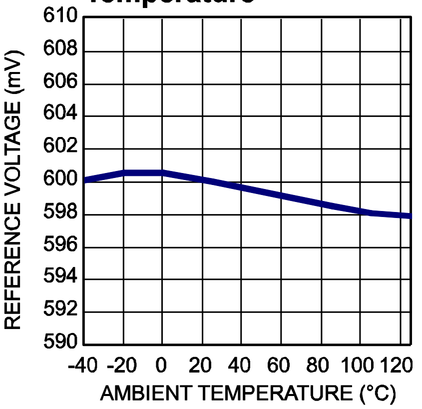
Disabled Supply Current vs. Input Voltage



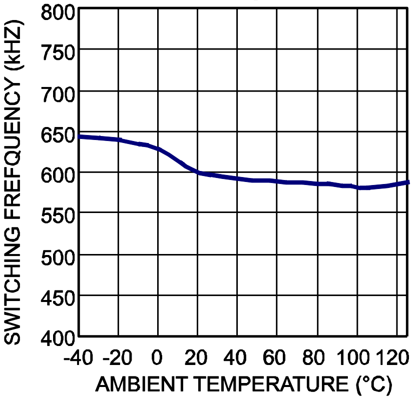
VIN UVLO Rising Threshold vs. Temperature



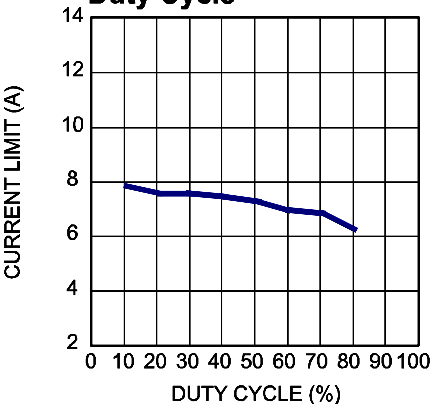
EN Rising Threshold vs. Temperature



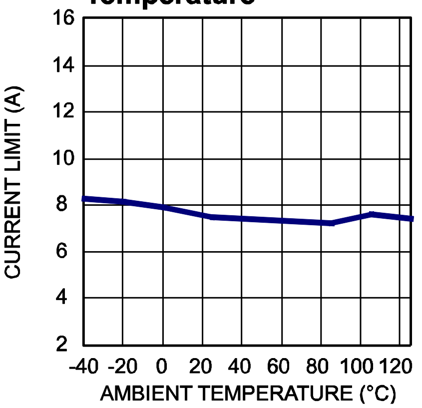
Reference Voltage vs. Temperature



Switching Frequency vs. Ambient Temperature



Current Limit vs. Duty Cycle

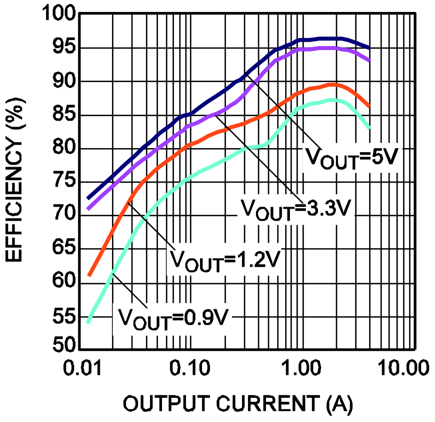


Current Limit vs. Temperature

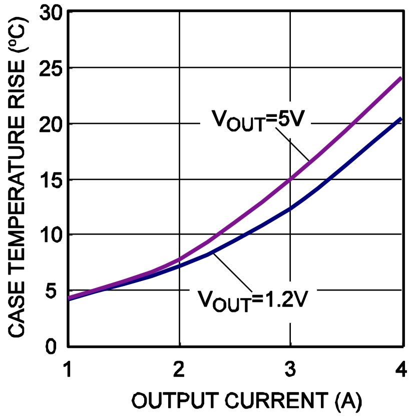
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12 V, V_{OUT} = 1.2 V, L = 1 µH, T_A = 25°C, unless otherwise noted.

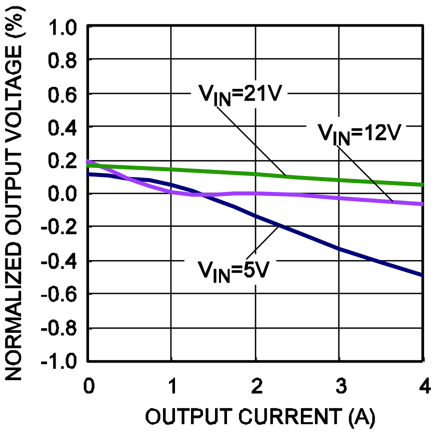
Efficiency vs. Output Current



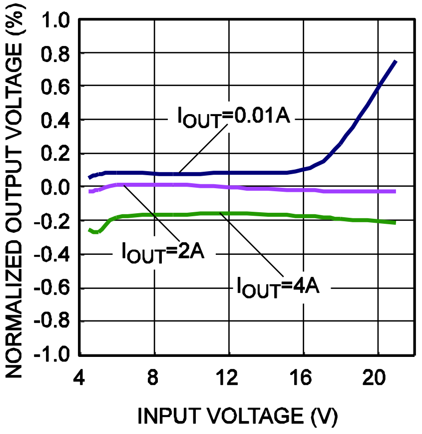
Case Temperature Rise vs. Output Current



Load Regulation



Line Regulation
V_{IN}=5V-21V

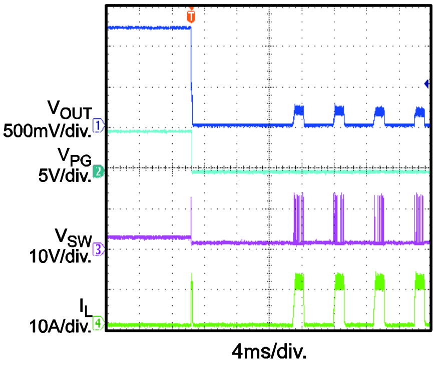


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12 V, V_{OUT} = 1.2 V, L = 1 μH, T_A = 25°C, unless otherwise noted.

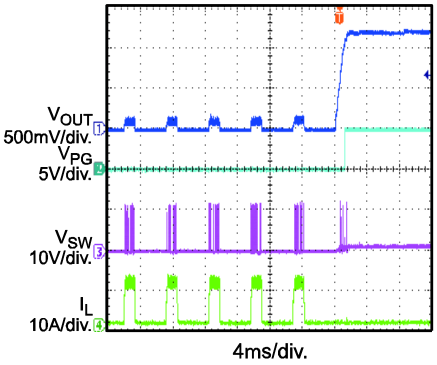
Short Entry

I_{OUT} = 0A



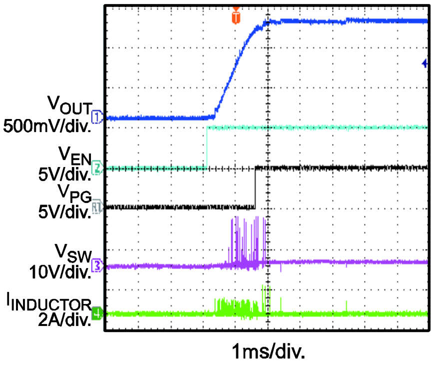
Short Recovery

I_{OUT} = 0A



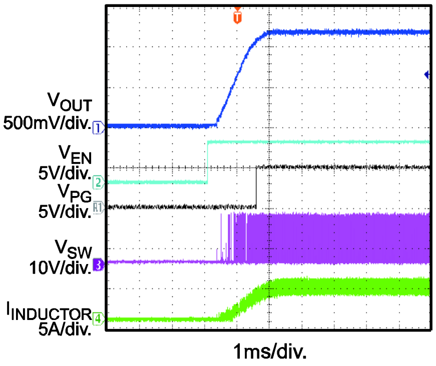
Start-Up through Enable

I_{OUT} = 0A



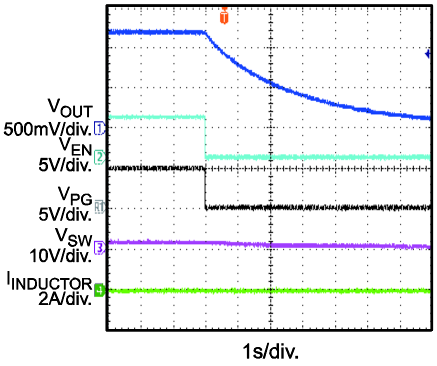
Start-Up through Enable

I_{OUT} = 4A



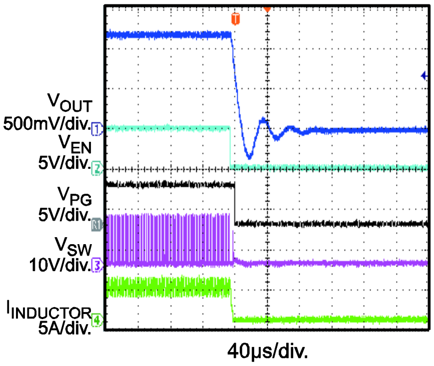
Shutdown through Enable

I_{OUT} = 0A



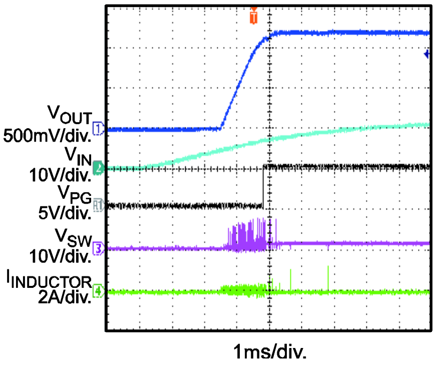
Shutdown through Enable

I_{OUT} = 4A



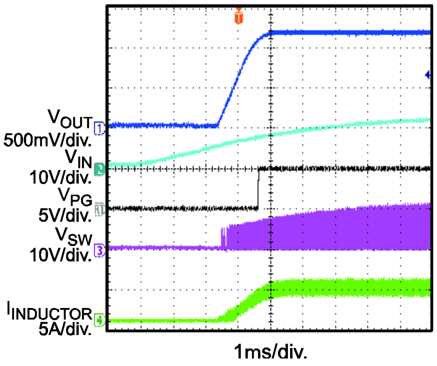
Start-Up through Input Voltage

I_{OUT} = 0A



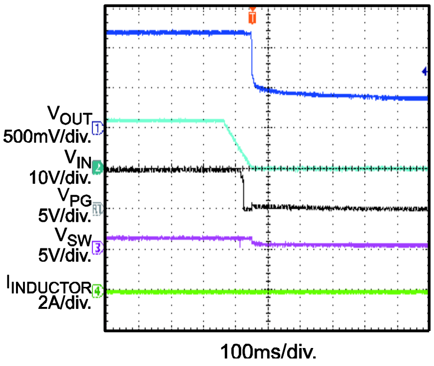
Start-Up through Input Voltage

I_{OUT} = 4A



Shutdown through Input Voltage

I_{OUT} = 0A

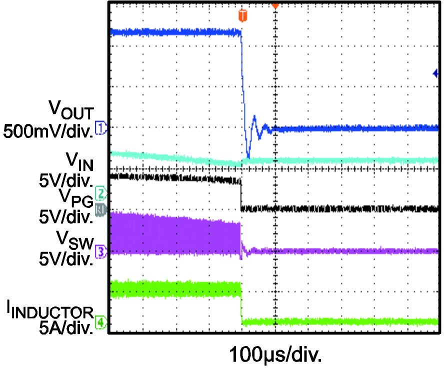


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12 V, V_{OUT} = 1.2 V, L = 1 µH, T_A = 25°C, unless otherwise noted.

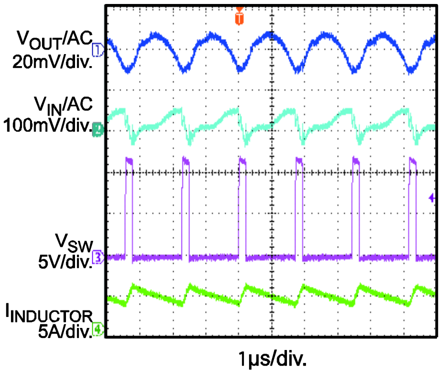
Shutdown through Input Voltage

I_{OUT} = 4A



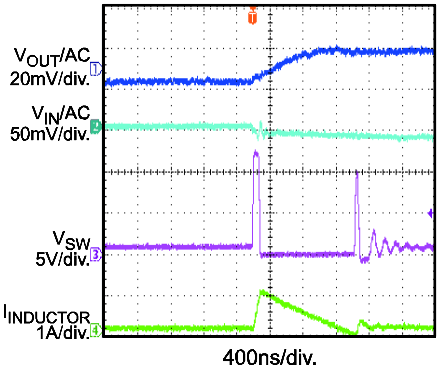
Input/Output Ripple

I_{OUT} = 4A



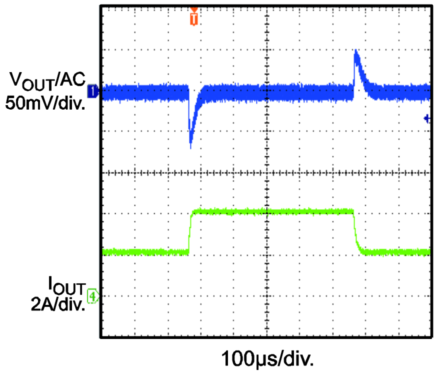
Input/Output Ripple

I_{OUT} = 0A



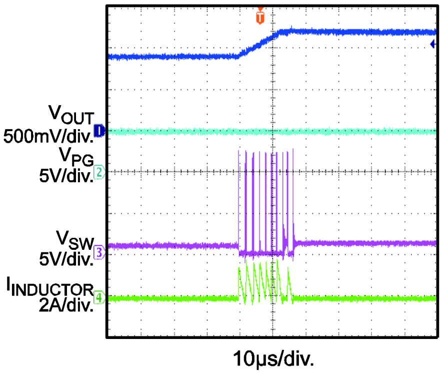
Load Transient Response

I_{OUT} = 2A to 4A



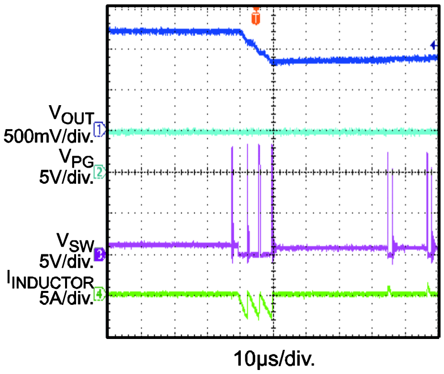
I^2C Control Slew Rate

Slew rate=16mV/µs, I_{OUT} = 0A, from 0.9V to 1.2V



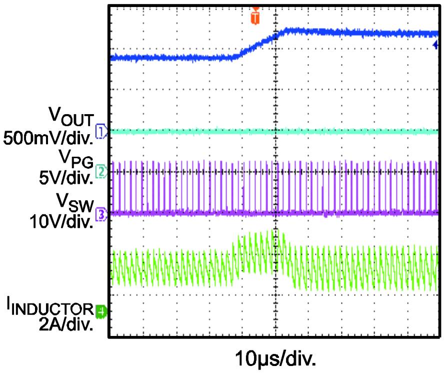
I^2C Control Slew Rate

Slew rate=16mV/µs, I_{OUT} = 0A, from 1.2V to 0.9V



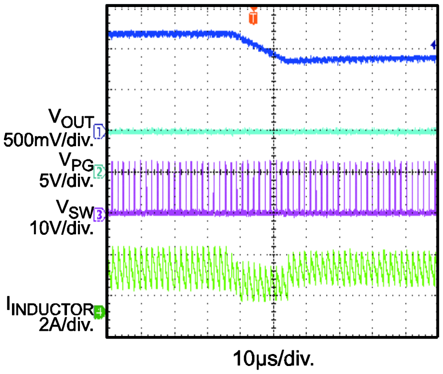
I^2C Control Slew Rate

Slew rate=16mV/µs, I_{OUT} = 2A, from 0.9V to 1.2V



I^2C Control Slew Rate

Slew rate=16mV/µs, I_{OUT} = 2A, from 1.2V to 0.9V



PIN FUNCTIONS

Pin #	Name	Description
1	VIN	**Supply voltage**. The MP8864 operates from a 4.5 V to 21 V input rail. VIN requires a ceramic capacitor to decouple the input rail. Connect VIN using a wide PCB trace.
2, 8	PGND	**System ground**. PGND is the reference ground of the regulated output voltage. PGND requires special consideration during PCB layout (see the “PCB Layout Guidelines” section on page 24). Connect PGND to GND with copper traces and vias.
3	EN/SYNC	**EN high to enable the MP8864**. EN/SYNC has an internal 1 MΩ pull-down resistor to ground.
4	PG	**Power good**. PG is an open-drain structure.
5	SDA	**I^{2}C serial data.**
6	SCL	**I^{2}C serial cloc**k.
7	ADD	**I^{2}C address set pin.** Leave ADD floating or pull it to VCC to set one address. Pulling ADD to ground sets an additional, different address.
9	SW	**Switch output.** Connect SW using a wide PCB trace.
10	BST	**Bootstrap.** BST requires a capacitor between SW and BST to form a floating supply across the high-side switch driver.
11	VOUT	**Sense input of output voltage in I^{2}C control loop.**
12	FB	**Feedback.** Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage in the FB control loop. Connecting FB to VCC sets the default output voltage at 0.9 V.
13	SS	**Soft-start.** Connect a capacitor from SS to ground to set the soft-start time.
14	VCC	**Internal 5V LDO regulator output**. Decouple with a 0.22 µF capacitor.
15	AGND	**Signal ground.** AGND is not connected internally to system ground. Ensure AGND is connected to system ground in the PCB layout.

FUNCTIONAL BLOCK DIAGRAM

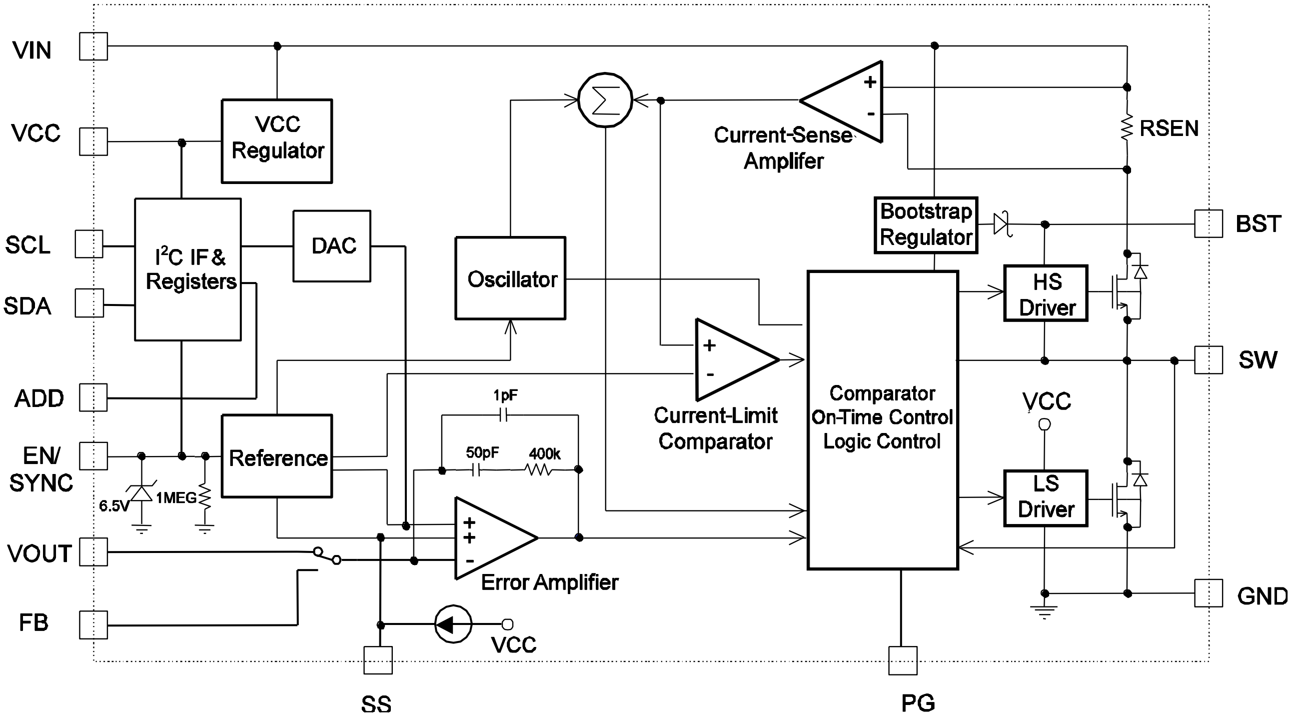


Figure 2—Functional block diagram

OPERATION

The MP8864 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. It offers a very compact solution that achieves a 4 A continuous output current with excellent load and line regulation over a wide input supply range.

The MP8864 has three working modes: advanced asynchronous modulation (AAM) mode, discontinuous conduction mode (DCM), and continuous conduction mode (CCM). When the MODE bit is set to "1" in the I^{2}C register, the MP8864 always operates in CCM.

AAM Control Operation

In a light-load condition, the MP8864 works in advanced asynchronous modulation (AAM) mode (see Figure 3). The V_{AAM} is an internal fixed voltage when the input and output voltages are fixed. V_{COMP} is the error amplifier output, which represents the peak inductor-current information. When V_{COMP} is lower than V_{AAM}, the internal clock is blocked. This causes the MP8864 to skip pulses, achieving the light-load power save. Refer to AN032 for additional details.

The internal clock re-sets every time V_{COMP} is higher than V_{AAM}. Simultaneously, the high-side MOSFET (HS-FET) turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP}.

The light-load feature in this device is optimized for 12 V input applications.

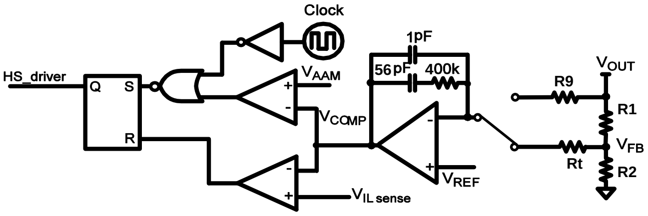


Figure 3—Simplified AAM control logic

DCM Control Operation

The V_{COMP} voltage ramps up as the output current increases. Once its minimum value exceeds V_{AAM}, the device enters DCM. In this mode, the internal clock initiates the PWM cycle, and the HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP}. After a period of dead time, the low-side MOSFET (LS-FET) turns on and remains on until the inductor current value decreases to zero. The device repeats the same operation in every clock cycle to regulate the output voltage (see Figure 4).

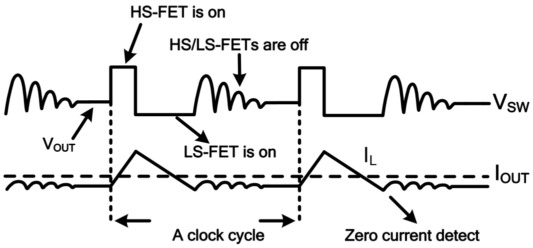


Figure 4—DCM control operation

CCM Control Operation

The device enters CCM from DCM once the inductor current no longer drops to zero in a clock cycle. In CCM, the internal clock initiates the PWM cycle, and the HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP}. After a period of dead time, the LS-FET turns on and remains on until the next clock cycle starts. The device repeats the same operation in every clock cycle to regulate the output voltage.

If $V_{ILsense}$ does not reach the value set by V_{COMP} within 95% (600 kHz switching frequency) of one PWM period, the HS-FET is forced off.

Internal Regulator

A 5 V internal regulator powers most of the internal circuitries. This regulator takes the V_{IN} input and operates in the full V_{IN} range. When V_{IN} is greater than 5 V, the output of the regulator is in full regulation. When V_{IN} is lower than 5 V, the output voltage decreases. A 0.22 μF ceramic capacitor for decoupling is required.

Error Amplifier (EA)

The error amplifier compares the FB voltage against the internal reference (REF) in the FB control loop and outputs the COMP voltage—which controls the power MOSFET current. In a I^{2}C control loop, FB is opened and VOUT is connected to the EA non-inverter input. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

EN/SYNC Control

EN/SYNC is a digital control pin that turns the regulator (including the I^{2}C block) on and off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. An internal 1 MΩ resistor from EN to GND allows EN/SYNC to be floated to shut down the chip.

EN is clamped internally using a 6.5 V series-Zener diode (see Figure 5). Connecting the EN input through a pull-up resistor to the voltage on V_{IN} limits the EN input current to less than 100 µA.

Connecting EN directly to a voltage source without a pull-up resistor requires limiting the amplitude of the voltage source to ≥6 V to prevent damage to the Zener diode.

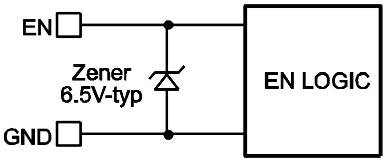


Figure 5—6.5 V Zener diode connection

The chip can be synchronized to an external clock range from 300 kHz to 2 MHz through EN/SYNC as soon as an external clock is added. Synchronize the internal clock rising edge to the external clock rising edge. Select an external clock signal with a pulse width less than 80% of the internal clock-cycle time.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP8864 UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 4 V while its falling threshold is 3.4 V.

Soft-Start (SS)

The MP8864 employs a soft-start (SS) mechanism to ensure smooth output during power-up. When EN goes high, an internal current source (12 µA) charges the SS capacitor. The SS capacitor voltage transfers over to the REF voltage to the PWM comparator. The output voltage ramps up smoothly with the SS voltage. Once the SS voltage rises above V_{REF}, it continues to ramp up until the REF voltage takes over. At this point, the soft-start is complete, and the device enters steady-state operation.

The SS capacitor value can be determined using Equation (1):

$$C_{SS}(nF) = \frac{T_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \tag{1}$$

If the output capacitors have a large capacitance value, it is NOT recommended to set a small SS time. Otherwise, it is easy to hit the current limit during SS.

Pre-Bias Start-Up

The MP8864 is designed for a monotonic start-up into a pre-biased output voltage. If the output is pre-biased to a certain voltage during start-up, the voltage on the soft-start capacitor is charged. When the soft-start capacitor's voltage exceeds the sensed output voltage at FB **(10)**, the part turns on the high-side and low-side power switches sequentially. The output voltage starts to ramp up with the soft-start slew rate.

NOTE:

10) FB voltage in the FB control loop, or VOUT voltage in the I^{2}C control loop.

Power Good Indicator (PG)

The MP8864 has power good (PG) output used to indicate whether the output voltage is ready. PG is an open-drain output. Connect PG to VCC or another voltage source through a pull-up resistor (e.g. 100 kΩ). When the input voltage is applied, PG is pulled down to GND before the internal SS is ready (V_{SS}>1.15 x V_{REF}). Once SS is ready (V_{FB}(10) is above 90% of V_{REF}), PG is pulled high (after an 80 µs delay time). During normal operation, PG is pulled low when the V_{FB}(10) drops below 70% of V_{REF} (after an 80 µs delay time).

When UVLO or OTP occur, PG is pulled low immediately. If OC (over current) occurs, PG is pulled low when V_{FB}(10) drops below 70% of V_{REF} (after an 80 µs delay time).

PG will NOT respond to an output over-voltage condition.

The PG bit in the I^{2}C register has the same indication as the external PG pin.

Output Over-Voltage Protection (OVP)

The MP8864 monitors a resistor divider (V_{FB}) to detect over voltage. When V_{FB} becomes higher than 115% of the target voltage, the LS-FET remains on until the LS current drops to -2.5 A. This discharges the output and tries to keep it within normal range. The part exits this regulation period when V_{FB}(10) drops below 105% of the reference voltage.

Over-Current Protection and Hiccup (OCP)

The MP8864 has cycle-by-cycle over-current limit control. When the inductor current peak value exceeds the set current-limit threshold, the HS-FET turns off and the LS-FET turns on and remains on until the inductor current falls below the internal *valley* current-limit threshold. The *valley* current-limit circuit decreases the operation frequency after the *peak* current-limit threshold is triggered. Meanwhile, the output voltage drops until V_{FB} is below the under-voltage (UV) threshold (50% below the reference, typically). Once UV is triggered, the MP8864 enters hiccup mode to re-start the part periodically. This protection mode is especially useful when the output is dead-shorted to ground. The average short-circuit current is reduced greatly to alleviate thermal issues and to protect the regulator. The MP8864 exits hiccup mode once the over-current condition is removed.

Thermal Shutdown (TSD)

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the die temperature exceeds 160°C, the entire chip shuts down. When the temperature is less than its lower threshold (140°C, typically) the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. The floating driver has its own UVLO protection. The UVLO's rising threshold is 2.2 V with a hysteresis of 150 mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M1, C4, L1, and C_{OUT} (see Figure 6). If V_{BST}-V_{SW} exceeds 5 V, U1 regulates M1 to maintain a 5 V BST voltage across C4. A 10 Ω resistor placed between SW and the BST capacitor is recommended to reduce SW spike voltage.

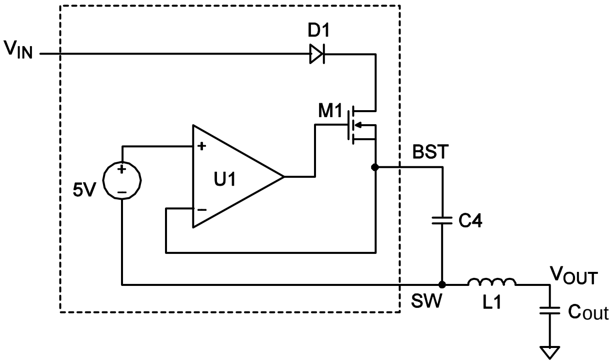


Figure 6—Internal bootstrap charging circuit

Start-Up and Shutdown

If both V_{IN} and EN exceed their respective thresholds, the chip starts up. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. During the shutdown, the signaling path is blocked first to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

I²C Control and Default Output Voltage

When the MP8864 is enabled (EN=high and VIN>UVLO), the chip starts up to an output voltage that is set by the FB feedback resistors with a programmed soft-start time; then the I²C bus can communicate with the master. If the chip does not receive the I²C communication signal continuously, it works efficiently through FB feedback and performs similar to traditional non-I²C parts.

Once the I²C receives valid output reference voltage scaling instruction (if V_BOOT="1"), the output voltage is determined by the resistor dividers R1, R2, and the V_{REF} voltage. The V_{OUT} value can be calculated using equation (2). The V_{REF} default value is 0.6 V:

$$V_{OUT} = V_{REF} \times (1 + \frac{R1}{R2}) \tag{2}$$

If V_BOOT="0," the output voltage is determined by the I²C control loop (the output voltage is sensed through VOUT), and the FB feedback control loop is disabled.

If FB is pulled up to VCC, the chip starts up directly to the default 0.9 V output voltage. In this case, the output voltage is determined by the I²C control loop.

The output reference voltage scaling is realized by adjusting the internal reference voltage (V_REF), which is the non-inverted input of the error amplifier. After the MP8864 receives a valid data byte of the output reference voltage setting, it searches the truth table for the corresponding reference voltage and then sends the command to adjust Vref with the controlled slew rate. The slew rate is determined by 3 bits of another register, which can be *read* and *write,* accordingly.

I^{2}C INTERFACE

I^{2}C Serial Interface Description

The I^{2}C is a 2-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are pulled externally to a bus voltage when they are “idle.” Connecting to the line, a master device generates the SCL signal and device address and arranges the communication sequence. The MP8864 interface is an I^{2}C slave, which supports both fast mode (400 kHz) and typically high-speed mode (3.4 Mhz). The I^{2}C interface adds flexibility to the power supply solution. The output voltage, transition slew rate, and other parameters can be controlled instantaneously by the I^{2}C interface.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low (see Figure 7).

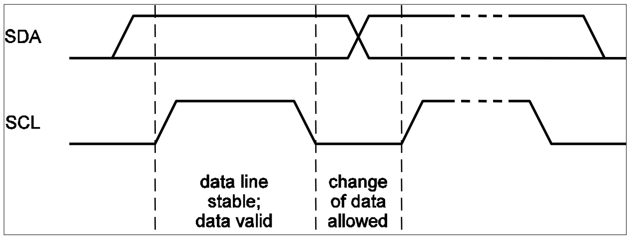


Figure 7—Bit transfer on the I^{2}C bus

Start and Stop Conditions

Start and stop are signaled by the master device, which signals the beginning and the end of the I^{2}C transfer. The start condition is defined as the SDA signal transitioning from high to low while the SCL is high. The stop condition is defined as the SDA signal transitioning from low to high while the SCL is high, as shown in Figure 8.

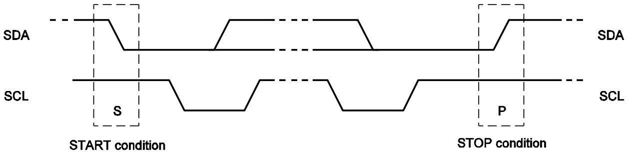


Figure 8—Start and stop conditions

Start and stop conditions are always generated by the master. The bus is busy once the start condition begins; the bus is free again after a minimum of 4.7 µs (after the stop condition). The bus stays busy if a repeated start (Sr) is generated instead of a stop condition. The start (S) and repeated start (Sr) conditions are functionally identical.

Transfer Data

Every byte put on the SDA line must be 8 bits long. Each byte must be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse, so it remains stable (low) during the high period of the clock pulse.

Data transfers follow the format shown in Figure 9. After the start condition (S), a slave address is sent. This address is 7 bits long, followed by an eighth bit which is a data direction bit (R/W). A “0” indicates a transmission (write), a “1” indicates a request for data (read). A data transfer is terminated always by a stop condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated start condition (Sr) and address another slave without first generating a stop condition (see Figure 8).

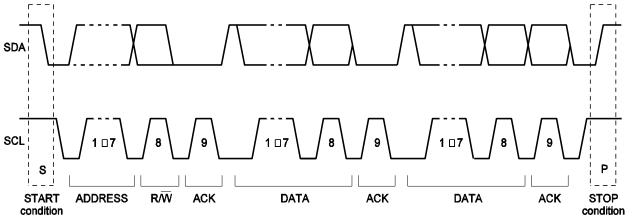


Figure 9—A complete data transfer

The MP8864 requires a start condition, a valid I^{2}C address, a register address byte, and a data byte for a single data update. After the receipt of each byte, the MP8864 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I^{2}C address selects the MP8864. The MP8864 performs an update on the falling edge of the LSB byte.

MP8864 I²C Chip Address

ADD sets the MP8864 address. The default 7-bit address of the MP8864 is “68” (hex) or “1101000” (binary) if ADD is floated or pulled up to VCC. The other MP8864 address is “60” (hex) or “1100000” (binary) if ADD is pulled to ground. When the master sends the address as an 8-bit value, the 7-bit address should be followed by “0/1” to indicate write/read operation (see Table 1).

Table 1—MP8864 address

ADD	Address (hex)	Address (binary)							
		A7	A6	A5	A4	A3	A2	A1	A0 (R/W)
Float or connected to VCC	D0	1	1	0	1	0	0	0	0
	D1	1	1	0	1	0	0	0	1
Connected to GND	C0	1	1	0	0	0	0	0	0
	C1	1	1	0	0	0	0	0	1

MP8864 Register Address

The MP8864 contains four registers: register 00 to register 03. The four registers complete the following actions:

- Register 00 sets the output voltage and decides whether the output voltage is controlled by the FB resistor divider or is set by the I²C.
- Register 01 sets the MP8864 operating features.
- Registers 02 and 03 are read registers only. Register 03 indicates the MP8864 status. *The register map is shown in the next section.*

REGISER DESCRIPTION

Register Map

ADD	NAME	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00	VSEL	R/W	V_BOOT	Output reference						
01	SysCntlreg1	R/W	EN	GO_BIT	Slew rate			Switching frequency		Mode
02	ID1	R	Vendor ID				IC revision			
03	Status	R	Reserved			VID_OK	OC	OTEW	OT	PG

Register Description

1. **Reg00 VSEL**

NAME	BITS	DEFAULT	DESCRIPTION
V_BOOT	D7	1	**FB control loop enable bit.** V_BOOT="1" means the output voltage is determined by a resistor divider connected to FB (the FB control loop). V_BOOT="0" means the output voltage is controlled by the I^2C through "VOUT" (the I^2C control loop). This bit is helpful for the default output voltage setting before the I^2C signal comes. If the I^2C is not used, the part works efficiently with FB.
Output reference	D[6:0]	0000000	**Output reference voltage**. Set the output reference voltage from 0.6 V to 1.87 V (see Table 2). The default value is 0.6 V. If FB is connected to VCC, the default value is 0.9 V.

Table 2—Output reference voltage chart

D[6:0]	VOUT	D[6:0]	VOUT	D[6:0]	VOUT	D[6:0]	VOUT
000 0000	0.60	010 0000	0.92	100 0000	1.24	110 0000	1.56
000 0001	0.61	010 0001	0.93	100 0001	1.25	110 0001	1.57
000 0010	0.62	010 0010	0.94	100 0010	1.26	110 0010	1.58
000 0011	0.63	010 0011	0.95	100 0011	1.27	110 0011	1.59
000 0100	0.64	010 0100	0.96	100 0100	1.28	110 0100	1.60
000 0101	0.65	010 0101	0.97	100 0101	1.29	110 0101	1.61
000 0110	0.66	010 0110	0.98	100 0110	1.30	110 0110	1.62
000 0111	0.67	010 0111	0.99	100 0111	1.31	110 0111	1.63
000 1000	0.68	010 1000	1.00	100 1000	1.32	110 1000	1.64
000 1001	0.69	010 1001	1.01	100 1001	1.33	110 1001	1.65
000 1010	0.70	010 1010	1.02	100 1010	1.34	110 1010	1.66
000 1011	0.71	010 1011	1.03	100 1011	1.35	110 1011	1.67
000 1100	0.72	010 1100	1.04	100 1100	1.36	110 1100	1.68
000 1101	0.73	010 1101	1.05	100 1101	1.37	110 1101	1.69
000 1110	0.74	010 1110	1.06	100 1110	1.38	110 1110	1.70
000 1111	0.75	010 1111	1.07	100 1111	1.39	110 1111	1.71
001 0000	0.76	011 0000	1.08	101 0000	1.40	111 0000	1.72
001 0001	0.77	011 0001	1.09	101 0001	1.41	111 0001	1.73
001 0010	0.78	011 0010	1.10	101 0010	1.42	111 0010	1.74
001 0011	0.79	011 0011	1.11	101 0011	1.43	111 0011	1.75
001 0100	0.80	011 0100	1.12	101 0100	1.44	111 0100	1.76
001 0101	0.81	011 0101	1.13	101 0101	1.45	111 0101	1.77
001 0110	0.82	011 0110	1.14	101 0110	1.46	111 0110	1.78
001 0111	0.83	011 0111	1.15	101 0111	1.47	111 0111	1.79
001 1000	0.84	011 1000	1.16	101 1000	1.48	111 1000	1.80
001 1001	0.85	011 1001	1.17	101 1001	1.49	111 1001	1.81
001 1010	0.86	011 1010	1.18	101 1010	1.50	111 1010	1.82
001 1011	0.87	011 1011	1.19	101 1011	1.51	111 1011	1.83
001 1100	0.88	011 1100	1.20	101 1100	1.52	111 1100	1.84

Table 2—Output reference voltage chart (*continued*)

D[6:0]	VOUT	D[6:0]	VOUT	D[6:0]	VOUT	D[6:0]	VOUT
001 1101	0.89	011 1101	1.21	101 1101	1.53	111 1101	1.85
001 1110	0.90	011 1110	1.22	101 1110	1.54	111 1110	1.86
001 1111	0.91	011 1111	1.23	101 1111	1.55	111 1111	1.87

2. Reg01 SysCntlreg1

<table>
<tr><th>NAME</th><th>BITS</th><th>DEFAULT</th><th colspan="4">DESCRIPTION</th></tr>
<tr><td>EN</td><td>D[7]</td><td>1</td><td colspan="4">**I^{2}C controlled turn-on or turn-off the part.** When the external EN is low, the converter is off, and the I^{2}C is in shutdown. When EN is high, the EN bit will take over. The default EN bit is “1.”</td></tr>
<tr><td>GO_BIT</td><td>D[6]</td><td>0</td><td colspan="4">**Switch bit of I^{2}C writing authority for output reference command only**. Set GO_BIT=“1” to enable the I^{2}C authority of the writing output reference. When the command is finished, GO_BIT is auto re-set to “0” to prevent false operation of VOUT scaling. If the reference is adjusted within 50 mV, GO_BIT will NOT be auto re-set to “0.” If this is the case, manually set GO_BIT to “0.” Writing GO_BIT=“1” first is recommended, then write the output reference voltage.</td></tr>
<tr><td rowspan="5">Slew rate</td><td rowspan="5">D[5:3]</td><td rowspan="5">100</td><td>D[5:3]</td><td>SLEW RATE</td><td>D[5:3]</td><td>SLEW RATE</td></tr>
<tr><td>000</td><td>64 mV/us</td><td>100</td><td>4 mV/us</td></tr>
<tr><td>001</td><td>32 mV/us</td><td>101</td><td>2 mV/us</td></tr>
<tr><td>010</td><td>16 mV/us</td><td>110</td><td>1 mV/us</td></tr>
<tr><td>011</td><td>8 mV/us</td><td>111</td><td>0.5 mV/us</td></tr>
<tr><td rowspan="5">Switching frequency</td><td rowspan="5">D[2:1]</td><td rowspan="5">00</td><td>D[2:1]</td><td>Fs</td><td></td><td></td></tr>
<tr><td>00</td><td>600 kHz</td><td></td><td></td></tr>
<tr><td>01</td><td>850 kHz</td><td></td><td></td></tr>
<tr><td>10</td><td>1.1 MHz</td><td></td><td></td></tr>
<tr><td>11</td><td>1.6 MHz</td><td></td><td></td></tr>
<tr><td>Mode</td><td>D0</td><td>0</td><td colspan="4">A “0” enables PFM mode, a high disables PFM mode.</td></tr>
</table>

3. Reg02 ID1

NAME	BITS	DESCRIPTION
Vendor ID	D[7:4]	1000
IC revision	D[3:0]	IC revision

4. Reg03 Status

NAME	BITS	DESCRIPTION
Reserved	D[7:5]	**Reserved for future use.** Always set at “0.”
VID_OK	D[4]	**I^{2}C controlled voltage adjustment is complete.** The internal circuit compares the DAC output with the VOUT voltage. If VOUT is in the 90%-110% range of the DAC output, the VID_OK bit is high (which means the voltage scaling is complete). Otherwise, VID_OK=“0.”
OC	D[3]	**Output over-current indication.** When the bit is high, the IC is in hiccup mode.
OTEW	D[2]	**Die temperature early warning bit.** When the bit is high, the die temperature is above 120˚C.
OT	D[1]	**Over-temperature indication**. When the bit is high, the IC is in thermal shutdown.
PG	D[0]	**Output power good indication.** When the bit is high, the VOUT power is good. This means the VOUT is higher than 90% of the designed regulation voltage. For additional details, please refer to the “Power Good Indicator” section on page 15.

APPLICATION INFORMATION

Setting the Output Voltage in the FB Control Loop

The reference voltage and the external resistor divider set the output voltage through FB. The feedback resistors R1 and R_T set the feedback-loop bandwidth with the internal compensation capacitor. Choose the value for R1 first, R2 is then given by Equation (3) [11]:

$$R2 = \frac{R1}{\frac{V_{OUT}}{V_{REF}} - 1} \qquad (3)$$

NOTES:

11) V_{REF} is 0.6 V when powering up or EN is on. After the MP8864 is enabled, V_{REF} can be programmed through the I^2C. Set V_BOOT="1" to enable the FB control loop.

The T-type network (see Figure 10) is recommended highly when V_{OUT} is low.

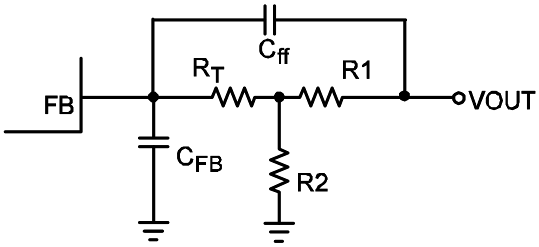


Figure 10—T-type network

Table 3 lists the recommended T-type resistor values for common output voltages.

Table 3—Resistor selection for common output voltages with default 0.6V V_{REF}(12)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R_T (kΩ)	C_{ff} (pF)	C_{FB} (pF)	L (uH)
0.9	Connect FB to VCC					1
1	34(1%)	51(1%)	33(1%)	15	10	1
1.2	34(1%)	34(1%)	33(1%)	10	10	1
1.8	34(1%)	16.5(1%)	15(1%)	10	15	1.5
2.5	34(1%)	10.7(1%)	15(1%)	15	22	1.8
3.3	34(1%)	7.5(1%)	15(1%)	15	33	2.7
5	34(1%)	4.64(1%)	7.5(1%)	15	47	2.7

NOTE:

12) The recommended parameters are based on a 12 V input voltage and a 22µF x 2 output capacitor. Different input voltage and output capacitor values may affect the selection of R1, R2, R_T, C_{ff}, and C_{FB}. For additional component parameters, please refer to the "Typical Application Circuits" section on page 26.

Setting the Output Voltage in the I^2C Control Loop

In addition to setting the output voltage through the FB loop, the I^2C loop can set the output voltage through VOUT by setting V_Boot="0". In this case, the output voltage is the set reference voltage. Please refer to Table 2 on page 20 for additional details about the output voltage setting.

Output Voltage Dynamic Scale

To dynamic scale the output voltage during normal operation, refer to Figure 11 and following the steps below:

Step 1: Write GO_Bit (reg01[6]) to "1."

Step 2: Write reg00 to select the feedback loop by setting V_BOOT(reg00[7]) and set the reference voltage by the output reference (reg00[0:6]) simultaneously. If the reference adjustment is within 50 mV, GO_BIT will not auto re-set to "0." If this is the case, manually set GO_BIT to "0." Repeat steps to dynamic scale to another voltage.

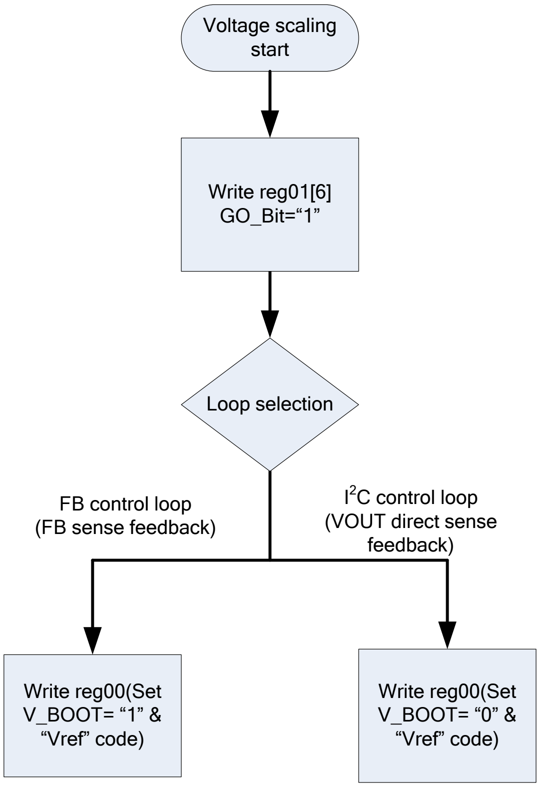


Figure 11—Output voltage dynamic scale flow chart

Selecting the Inductor

For most applications, use a 1 µH to 10 µH inductor with a DC current rating at least 25% higher than the maximum load current. For highest efficiency, use an inductor with a DC resistance less than 15 mΩ. For most designs, the inductance value can be derived from Equation (4):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \qquad (4)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be determined using Equation (5):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \qquad (5)$$

Use a larger inductor for improved efficiency under light-load conditions—below 100 mA.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore it requires a capacitor to supply the AC current while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Use ceramic capacitors with X5R or X7R dielectrics for best results because of their low ESR and small temperature coefficients. For most applications, use a 22µF x 2 capacitor.

Since C2 absorbs the input switching current, it requires an adequate ripple-current rating. The RMS current in the input capacitor can be estimated using Equation (6):

$$I_{C2} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \qquad (6)$$

The worse case condition occurs at $V_{IN} = 2V_{OUT}$. See Equation (7).

$$I_{C2} = \frac{I_{LOAD}}{2} \qquad (7)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current. The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1 µF) placed as close to the IC as possible. Ensure ceramic capacitors have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by capacitance can be estimated using equation (8):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C2} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \qquad (8)$$

Selecting the Output Capacitor

The output capacitor (C5) maintains the DC output voltage. Use ceramic, tantalum, or low ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated using Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times (R_{ESR} + \frac{1}{8 \times f_S \times C5}) \qquad (9)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated using Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C5} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \qquad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated using Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \qquad (11)$$

The output capacitor affects the stability of the regulation system. The MP8864 can be optimized for a wide range of capacitance and ESR values.

External Bootstrap Diode (BST)

BST voltage may become insufficient at particular conditions. If any of these conditions occur, an external bootstrap diode can enhance the efficiency of the regulator and avoid insufficient BST voltage at light-load PFM operation.

Insufficient BST voltage is more likely to occur at the following conditions:

- V_{IN} is low.
- The duty cycle is large: $D=\frac{V_{OUT}}{V_{IN}}>65\%$

If insufficient BST voltage occurs during these conditions, the output voltage ripple may become extremely large during light-load conditions, or there may be bad efficiency during heavy-load conditions. Add an external BST diode from VCC to BST (see Figure 12).

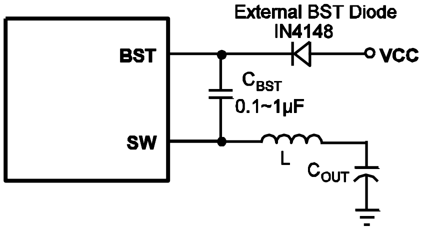


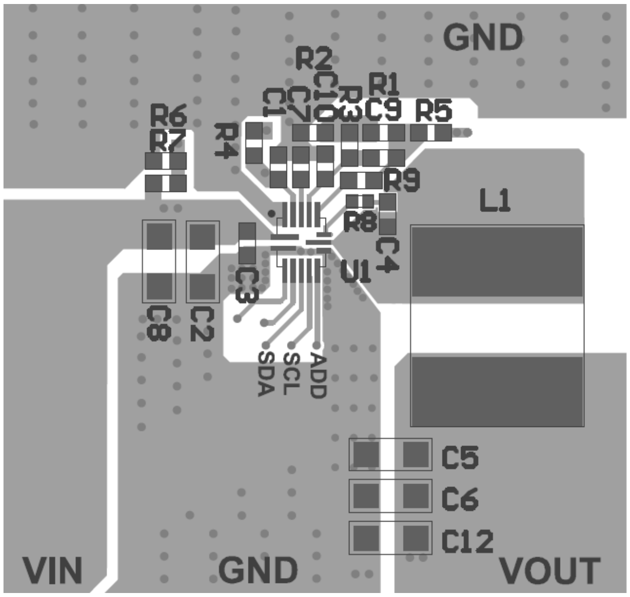
Figure 12—Optional external bootstrap diode to enhance efficiency

The recommended external BST diode is 1N4148, and the BST capacitor value is 0.1 µF to 1 µF.

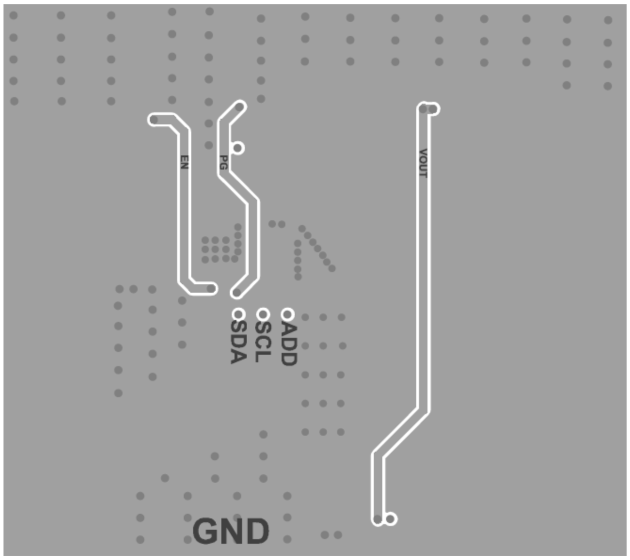
PCB Layout Guidelines (13)

Efficient PCB layout is critical to achieve stable operation, especially for VCC capacitor and input capacitor placement. For best results, refer to Figure 13 and follow the guidelines below:

1) Use a large ground plane to connect directly to GND. Add vias near GND if the bottom layer is ground plane.
2) Place the VCC capacitor as close as possible to VCC and GND. Make the trace length of VCC to the VCC capacitor anode to the VCC capacitor cathode chip to GND as short as possible.
3) Place the ceramic input capacitor close to IN and GND. Keep the connection of the input capacitor and IN as short and wide as possible.
4) Route SW and BST away from sensitive analog areas such as FB. It is NOT recommended to route a SW and BST trace under the chip's bottom layer.
5) Place the T-type feedback resistor R3 close to the chip to ensure the trace (which connects to FB) is as short as possible.



Top Layer



Bottom Layer

Figure 13—Recommended PCB layout

NOTE:

13) The recommended layout is based on Figure15 and the Typical Application circuit on page 26.

Design Example

Table 4 shows a design example following the application guidelines for the following specifications:

Table 4—Design example

V_{IN}	12 V
V_{OUT}	1.2 V
I_O	4 A

The detailed application schematics are shown in Figure 16. The typical performance and circuit waveforms have been shown in the “Typical Performance Characteristics” section. For additional device applications, please refer to the related evaluation board datasheets.

TYPICAL APPLICATION CIRCUITS (14)

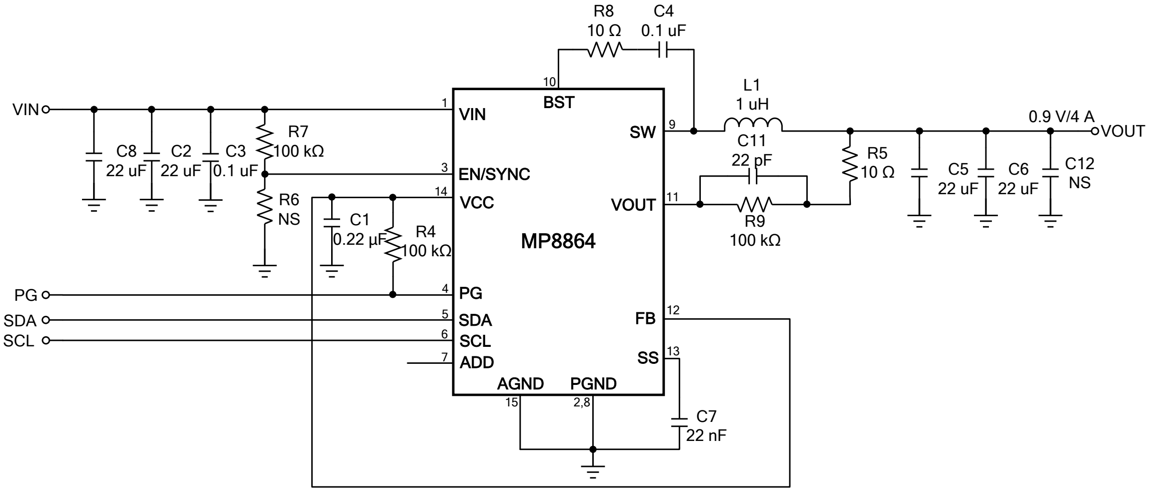


Figure 14—12 V Input-0.9 V/4 A Output (15)

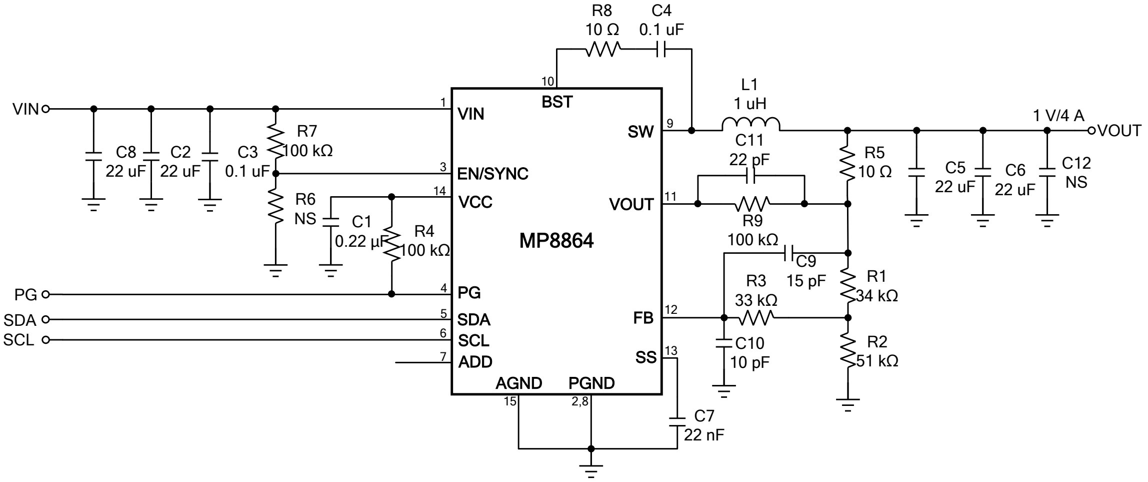


Figure 15—12 V Input-1 V/4 A Output

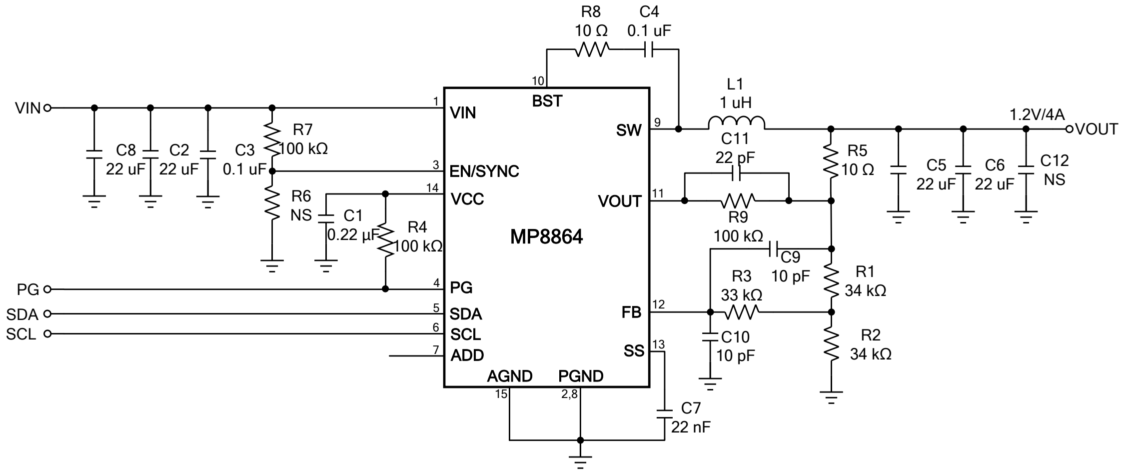


Figure 16---12 V Input-1.2 V/4 A Output

Notes:

14) Excluding Figure 13, the circuits are based on a 0.6 V default reference voltage.
15) R5 is used for loop test purposes. It is NOT needed if the test loop signal is small.

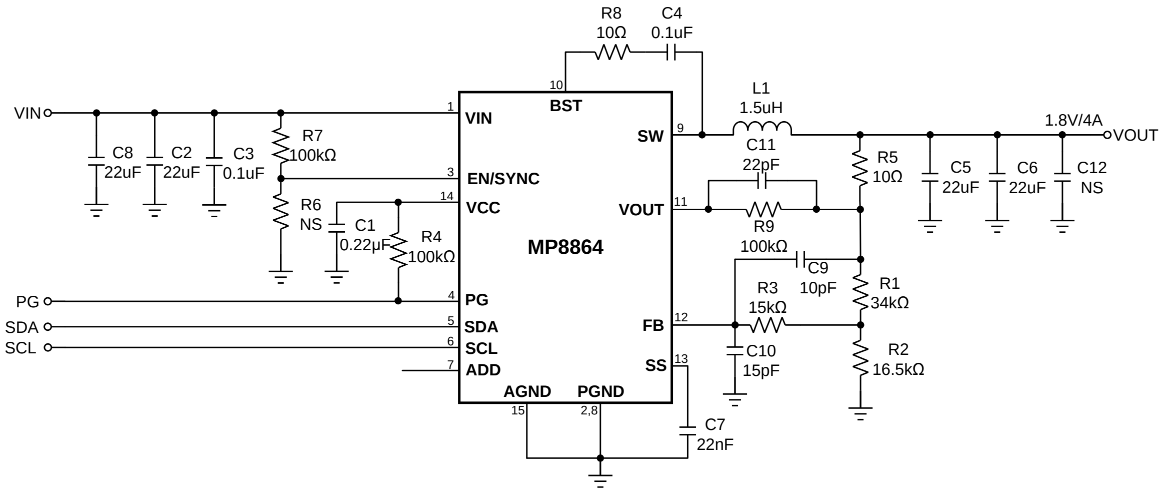


Figure 17—12 V Input-1.8 V/4 A Output

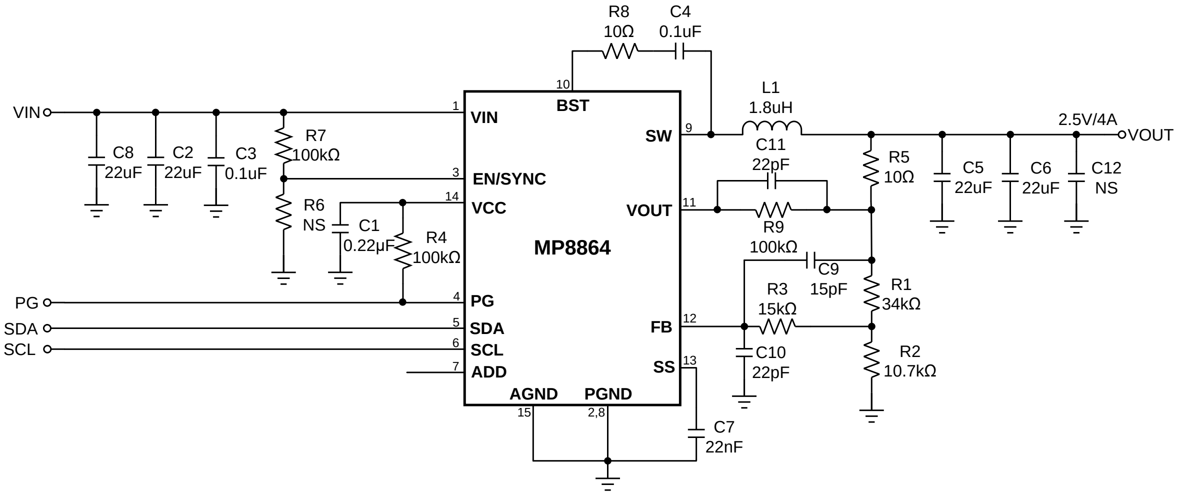


Figure 18—12V Input-2.5 V/4 A Output

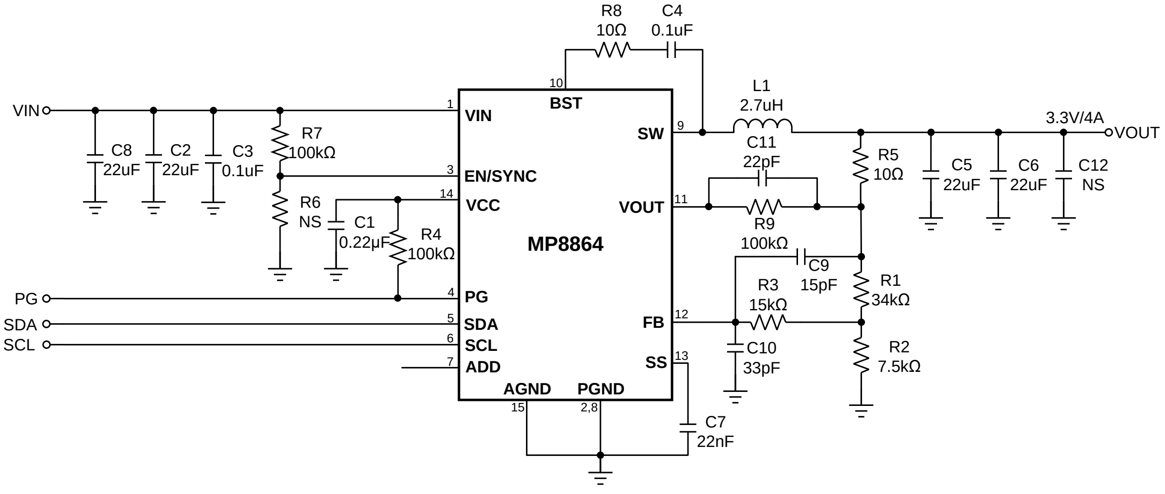


Figure 19—12 V Input-3.3 V/4 A Output

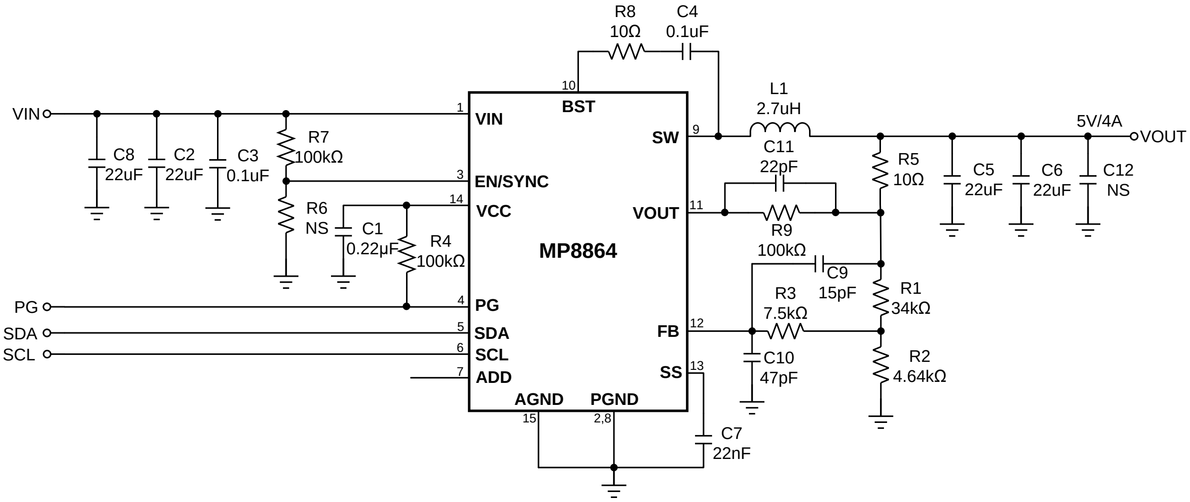
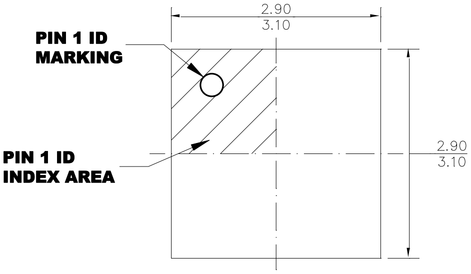


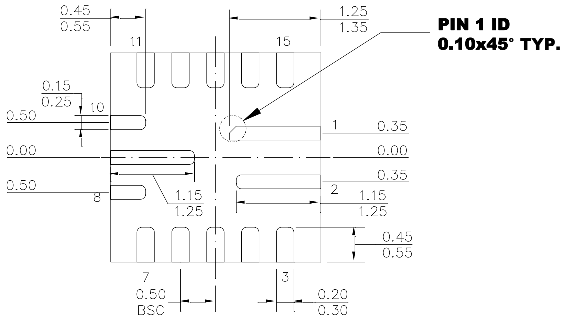
Figure 20—12 V Input-5 V/4 A Output

PACKAGE INFORMATION

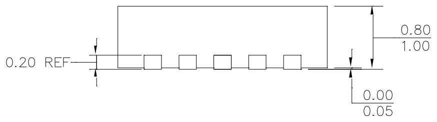
QFN-15 (3mm X 3mm)



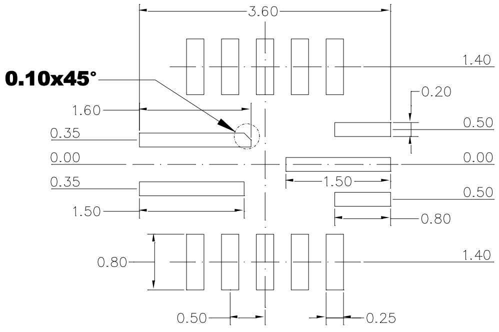
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.