



Product Change Notification - LIAL-30DTSS543

Date:

03 Feb 2020

Product Category:

Memory

Affected CPNs:**Notification subject:**

Memo # ML01202000QB: Final Notice: New silicon mask set with design and layout changes for selected Microchip products of the AT24C16D device family.

Notification text:**PCN Status:**

Final notification.

PCN Type:

Manufacturing Change

Microchip Parts Affected:

Please open one of the icons found in the Affected CPNs section above.

NOTE: For your convenience Microchip includes identical files in two formats (.pdf and .xls)

Description of Change:

New silicon mask set with design and layout changes for selected Microchip products of the AT24C16D device family

Pre Change:

Manufactured using 36316 Rev A0 mask on 36.3K wafer technology fabricated at Microchip fabrication sites FAB 5 (Colorado Springs, CO, USA) using 6 inch wafers.

Post Change:

Manufactured using 363V4 rev A2 mask on 36.3K wafer technology fabricated at Microchip fabrication site FAB 5 (Colorado Springs, CO, USA) using 6 inch wafers or manufactured using 36316 Rev A0 mask on 36.3K wafer technology fabricated at Microchip fabrication site FAB 5 (Colorado Springs, CO, USA) using 6 inch wafers.

Pre and Post Change Summary:

	Pre Change	Post Change	
Wafer Mask	36316 Rev A0	363V4 Rev A2	36316 Rev A0
Wafer Technology	36.3K wafer technology	36.3K wafer technology	
Fabrication Location	FAB 5 (Colorado Springs, CO USA)	FAB 5 (Colorado Springs, CO USA)	
Wafer Diameter	6 inches (150 mm)	6 inches (150 mm)	
Quality certification	ISO/TS16949	ISO9001/TS16949	



Impacts to Data Sheet:

None

Change Impact:

None

Reason for Change:

to improve manufacturability by qualifying a new silicon mask set with design and layout changes.

Change Implementation Status:

In Progress

Estimated First Ship Date:

April 15, 2020 (date code: 2016)

NOTE: Please be advised that after the estimated first ship date customers may receive pre and post change parts

Time Table Summary:

	February 2020				->	April 2020				
Workweek	06	07	08	09		14	15	16	17	18
Final PCN Issue Date	x									
Qual Report Availability	x									
Estimated Implementation Date								X		

Method to Identify Change:

Traceability code

Qualification Report:

Please open the attachments included with this PCN labeled as PCN_#_Qual Report.

Revision History:

February 3, 2020: Issued final notification. Attached the qualification report. Provided estimated first ship date to be on April 15, 2020

The change described in this PCN does not alter Microchip's current regulatory compliance regarding the material content of the applicable products

Attachment(s):

[PCN_LIAL-30DTSS543_QUAL REPORT.pdf](#)

Please contact your local [Microchip sales office](#) with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

AT24C16D-MAHM-E

AT24C16D-MAHM-T

AT24C16D-PUM

AT24C16D-SSHM-B

AT24C16D-SSHM-T

AT24C16D-STUM-T

AT24C16D-XHM-B

AT24C16D-XHM-T



MICROCHIP

**QUALIFICATION REPORT SUMMARY
RELIABILITY LABORATORY**

PCN#: LIAL-30DTSS543

**Date
December 3, 2019**

**New silicon mask set with design and layout changes for
selected Microchip products of the AT24C16D device family**



MICROCHIP

SUMMARY QUALIFICATION REPORT

Purpose: New silicon mask set with design and layout changes for selected Microchip products of the AT24C16D device family

Document Control #: ML122019000C

Document Revision: A

Device(s): AT24x08/AT24x16/24xx08x/24xx16x

Product: 5V 2W 16K serial EEPROM

Mask Identification #: 363V4

Process 0.25um, 6" wafer

MSL: 3301



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SUMMARY QUALIFICATION REPORT

Qualification Material:

LOT	LOT 1
DEVICE	24AA16-E/P
MASK, REV	363V4 (A2)
WAFER FAB	Fab 5
WAFER PROCESS	0.25um, 6"
WAFER LOT	MCSO520188047.000
ASSEMBLY LOT	MMT-202100278.000
PACKAGE	8LD PDIP
ASSEMBLY SITE	MMT
FINAL TEST	MTAI
QUAL #	ESD: ML0920190079 LU: ML092019007A CDM: ML102019003B
QUAL TEST	HTOL / ELFR / HTDR / ESD / LU / CDM

Conclusion:

Pass Fail

Based on the results, the 363V4 mask has meet the reliability guidelines implemented in the qualification plan.

Qualification Data:

Early Life Failure Rate (ELFR):

Test Method	AEC Q100-008
Test Condition	125°C / 24 hours
Sample Size (800 ea. min)	(Fail/Pass)
Lot 1	0 / 815

Pre & Post Testing was done @ +25°C, -40°C, +85°C, and 125°C.

High Temperature Operating Life (HTOL)

Test Method	AEC Q100-005
Test Condition	125°C / 408 hours
Sample Size (77 ea. min)	(Fail/Pass)
Lot 1	0 / 615

Pre & Post Testing was done @ +25°C, -40°C, +85°C, and 125°C.

High Temperature Data Retention (HTDR)

Test Method	AEC Q100-005
Test Condition	125°C / 504 hours
Sample Size (231 ea. min)	(Fail/Pass)
Lot 1	0 / 246

Pre & Post Testing was done @ +25°C, -40°C, +85°C, and 125°C.

ESD and Latch Up

Test	Reference Method	Sample	Highest Passing Voltage
ESD – HBM	AEC Q100-002 JS-001-2017	18/Lot 1	+/- 4500V
ESD – CDM	AEC Q100-11 (ANSI/ESD S5.3.1)	18/Lot 1	+/- 2000V on all pins
Latch Up	AEC Q100-004 JEDEC JESD78	6/Lot 1 6/Lot 1 6/Lot 1	6 Pass @ +25°C ^a 6 Pass @ +125°C ^a 6 Pass @ +25°C ^b

All Pre & Post Testing done @ +25°C, +85°C, and 125°C.

^a +/-105mA Pulse / +Overvoltage stress

^b +/-200mA Pulse / +Overvoltage stress

MTBF/FIT Data:

These calculations only consider ELFR and DLT data from this Qualification	
Activation Energy	0.7 eV
Application Temperature	55 degrees C

	Infant Mortality	Total Life	MTBF (Hours)
Device Hours	19,560	270,480	N/A
Fit Rate - 50% Confidence	136	10	101,595,911
Fit Rate - 60% Confidence	180	13	76,854,340
Fit Rate - 90% Confidence	452	33	30,583,417

Note: One FIT is one fail in 10⁹ device hours

	Best Estimated Failure Rate (%KHR)
Infant Mortality	0.0136
Total Life	0.0010